Sādhanā (2019) 44:137
https://doi.org/10.1007/s12046-019-1121-1

A compact 4-to-8-bit nonbinary SAR ADC based on 2 bits per cycle DAC architecture

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MS received 10 March 2018; revised 13 July 2018; accepted 7 March 2019; published online 7 May 2019

Abstract. A compact programmable-resolution successive approximation register (SAR) analog to digital converter (ADC) for biosignal acquisition system is presented. The ADC features a programmable 4-to-8-bit DAC that makes the ADC programmable with 2 bits evaluated in each clock cycle. At low resolution with relaxed noise and linearity requirements, use of an increased clock speed improves energy efficiency. A single DAC architecture is used to generate references for 2 bits per cycle evaluation for all resolutions. Nonbinary switched capacitor circuits, least sensitive to parasitics, are proposed for the use in DAC for reference generation. The choice of architecture and circuit design are presented with mathematical analysis. The post-layout simulation of designed ADC in 90 nm CMOS process has 1.2 MS/s sampling rate at 8-bit mode with a power consumption of 185 μW achieving an ENOB of 7.6. The active area of designed ADC is 0.06 mm^2. The DAC resolution scaling and the use of variable sampling rate maximize efficiency at lower resolutions. Therefore, figure of merit (FOM) is degraded only by a factor of 4.7 for resolution scaling from 8 to 4 bits. This is a significant improvement over 16× degradation expected from 8-bit to 4-bit resolution scaling by truncating the bits.

Keywords. Analog to digital converter (ADC); successive approximation register (SAR); parasitic insensitive; programmable resolution; low power; charge recycling; 2-bit per cycle; nonbinary.

1. Introduction

Biomedical monitoring systems, used to record various physiological parameters, are required to process vital signals having varying bandwidth as well as dynamic range requirements. For example, in applications such as ECG monitoring, low resolution is desirable to detect the heart rate and high resolution to observe ST pattern changes [1, 2]. In neuroprosthetic applications, each electrode senses signals from multiple neurons, which need to be distinguished. Therefore, the resolution required in digitizing the signal from each electrode is not uniform across all electrodes [4]. The analog-to-digital converters (ADCs) in the analog front-end of such systems should have resolution and sampling rate necessary to cater to the requirements of signals being processed. Successive approximation register (SAR) ADCs with capacitive DACs are popular for biomedical signal digitization due to their low-power requirements. However, conventional SAR ADCs with a fixed resolution and sampling rate are not able to adapt to multiple signals demanding different resolutions. ADCs having programmable resolution and sampling rate are appropriate for these applications. They reduce the design time since the ADCs can be reproduced for use in different channels. In addition, they can also effectively reduce the silicon real-estate if re-used through time-multiplexing.

Many of the SAR ADCs found in the literature incorporate variability of resolution into a conventional charge redistribution ADC, even though this approach leads to low power but at the expense of area and speed. The ADC [3] has 12-bit and 8-bit resolution options with scalable sample rate by purging DAC capacitors so that they can be used to generate suitable auto-zero reference for comparator offset calibration. This leads to the separation of sampling phase and auto-zeroing but trading off the conversion time. A resolution-reconfigurable DAC architecture [2] uses two DACs (main DAC and sub-DAC) to facilitate scalability. Voltage scaling at lower resolution improves energy efficiency. In adaptive resolution charge redistribution SAR ADC [4], described for neural sensor application, larger capacitors used in a DAC are switched out for lower resolution. Also, SAR logic is reconfigured for lower resolution operations. Therefore power scales linearly with resolution over a small range, whereas sampling rate remains constant in all resolution modes.

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SAR architectures [5, 6] that resolve 2 bits in a cycle are also popular since they can effectively double the conversion speed but at the expense of power and area. Among the diversity of available topologies, choosing a right architecture that is power efficient over the range of bandwidth and resolution, as well as configurable, is fundamental to this work. In this work, a 2-bit-per-cycle DAC architecture is proposed based on a DAC [8] architecture, and modified suitably for 2-bit-per-cycle operation as well as resolution programmability. DAC architecture locally utilizes a flash converter concept to enhance the speed of operation by resolving 2 bits in one successive approximation conversion cycle. The DAC architecture uses a reference generation circuit based on switched capacitor (SC) for the flash that is least sensitive to parasitics. A mathematical analysis also has been carried out to justify the parasitic-insensitive nature of reference generation scheme. The proposed idea has been validated by designing an 8-bit ADC [7] in 90 nm CMOS technology for operations on 1 V supply. Since this DAC architecture has fixed components and is independent of resolution, programmable-resolution feature is trivial. The proposed resolution-programmable ADC has resolution modes varying from 4 to 8 bits with 1-bit increment. In addition, for a given resolution, variation in the sampling rate is achieved over a range of frequencies by suitably varying the system clock period.

The remaining paper is organized as follows. Section 2 explains 2-bit-per-cycle DAC algorithm and timing. Section 3 includes programmable ADC with 2 bits per cycle DAC architecture. Section 4 contains details of parasitic insensitive reference generation circuit used for the DAC and section 5 presents resolution programmability feature of ADC. Section 6 includes details regarding various building blocks of ADC such as buffer, comparator and gate boosted sample and hold. Sections 7 and 8 give the post layout simulation results of ADC and conclusion respectively.

2. Two bits per cycle DAC algorithm and timing

A DAC architecture has been proposed for 2 bits per cycle operation. The proposed architecture uses fixed number of capacitors for resolution from 4 to 8 bits. The variable resolution architecture proposed is an extended version of the architecture proposed in [8] and [9]. The proposed architecture is also made parasitic independent when compared with [9]. The algorithm followed for extracting a 2 bits per cycle can be explained with the help of figure 1.

- In the beginning of each clock cycle, two voltages V_{TOP} and V_{BOT} are generated based on the bits evaluated in the previous cycle.
- V_{TOP} and V_{BOT} are divided into four equal parts (quadrants), each of value $(V_{TOP} - V_{BOT})/4$. The resulting three levels between V_{TOP} and V_{BOT} are denoted as V_{TH1}, V_{MID} and V_{TH2} (in the decreasing order of voltage).

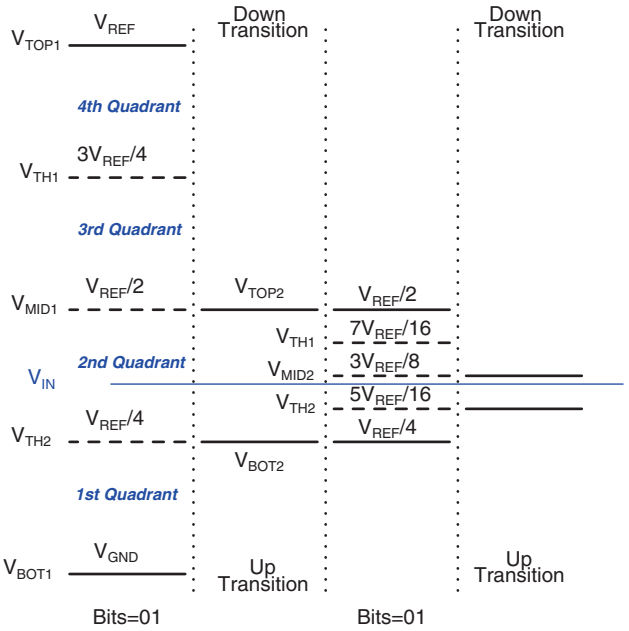

Figure 1. Pictorial representation of the algorithm followed in DAC for reference generation.

- These three voltage levels are compared to the input V_{IN} to evaluate the two bits in each cycle.

In the first clock cycle, $V_{TOP} - V_{BOT}$ is equal to the full scale voltage V_{REF}. In the second cycle, V_{TOP} and V_{BOT} are updated based on the quadrant in which the input is present. This process is repeated until all the bits are evaluated. As can be seen in figure 1, both V_{TOP} and V_{BOT} converge towards the input. All the desired voltage levels are generated using SC circuit (DAC). Timing diagram of the conversion process is shown in figure 2. Each conversion cycle has a sampling phase and a hold phase. In the sampling phase, the input is sampled and in the hold phase the conversion takes place. The clk_H = HIGH is the recycling phase except for the first cycle, which is a sampling phase. In recycling phase, V_{TOP} and V_{BOT} required for the bit evaluation in the current cycle are generated by recycling two of the voltages V_{TOP}, V_{TH1}, V_{MID}, V_{TH2} and V_{BOT} from

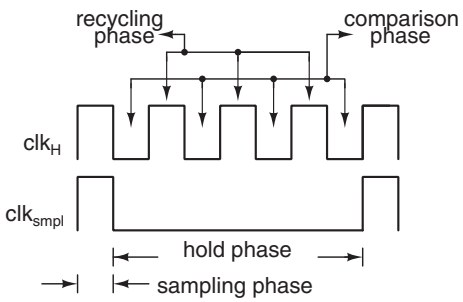

Figure 2. Timing details of one conversion cycle.

the previous cycle based on the bits evaluated in the previous cycle. During clk_H = LOW (comparison phase), V_{TH1}, V_{MID} and V_{TH2} are generated for the current cycle from V_{TOP} and V_{BOT}. Also, the 2 bits are evaluated by comparing V_{IN} to V_{TH1}, V_{MID} and V_{TH2}. In the sampling phase, the input is sampled and simultaneously V_{TOP} and V_{BOT} are set such that $V_{TOP} - V_{BOT} = V_{REF}$ and $(V_{TOP} - V_{BOT})/2 = V_{CM}$, the common mode voltage. The input V_{IN} also resides on the same common mode voltage.

3. Programmable ADC with 2-bit-per-cycle DAC architecture

A simplified block diagram of the proposed programmable-resolution ADC is shown in figure 3. The SAR controller controls the DAC to generate threshold voltages for the 2-bit flash. A Finite-State Machine (FSM) generates clocks necessary to generate control signals to turn ON/OFF the switches in the DAC as well as switches at the inputs of the three comparators.

The DAC architecture for 2 bits per cycle evaluation is shown in figure 4. There are a total of four SC blocks that are used to generate the three reference voltages (V_{TH1}, V_{MID} and V_{TH2}) for the flash. They are named LEFT, RIGHT, UP and DOWN. The SC blocks LEFT and RIGHT are identical circuits that generate V_{MID} in tandem. In one cycle, LEFT generates V_{MID} and RIGHT holds the two voltages (V_{TOP}, V_{BOT}) that are being processed. These two SC blocks interchange this task in subsequent comparison cycles. UP and DOWN SC blocks are used to generate V_{TH1} and V_{TH2}, respectively, for every comparison cycle. Outputs of the comparators are encoded at each comparison phase

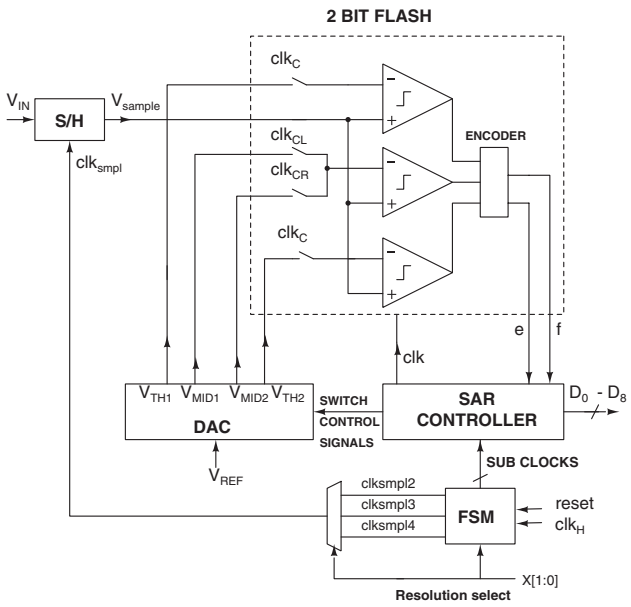

Figure 3. Block diagram of programmable-resolution, fixed voltage SAR ADC.

and based on the pair of bits generated during comparison phase, charge recycling is done by switching ON the appropriate switches in the DAC. This process continues until all pairs of bits are evaluated. DAC uses a fixed number of unit sized capacitors for reference generation that is independent of resolution, and reference generation is parasitic insensitive to a large extent. In each of the recycling phase, only two split buffer sets out of the four are active. The conventional binary search algorithm can be carried out at no extra clock cycles and comparison steps. The control logic block is developed using a minimum number of custom-designed basic gates. Most of the logic realized are two level NAND–NAND circuits so that delay in the generation of control signals is minimum.

4. Parasitic-insensitive reference generation circuit for V_{TH1}, V_{MID} and V_{TH2}

The four SC blocks LEFT/RIGHT, UP and DOWN generating the three reference voltages V_{MID}, V_{TH1} and V_{TH2} must be free of parasitic effects. The proposed scheme makes the threshold generation parasitic insensitive to a large extent. The proposed scheme is analysed with respect to the scheme proposed in [9]. The three threshold voltages to be generated from V_{TOP} and V_{BOT} are given in (1)–(3):

$$V_{MID} = \frac{1}{2}(V_{TOP} + V_{BOT}), \tag{1}$$

$$V_{TH1} = \frac{3}{4}V_{TOP} + \frac{1}{4}V_{BOT}, \tag{2}$$

$$V_{TH2} = \frac{1}{4}V_{TOP} + \frac{3}{4}V_{BOT}. \tag{3}$$

In [9] V_{MID}, V_{TH1} and V_{TH2} are generated using SC networks and buffers using circuits shown in figures 5 and 6 [9]. These circuits are susceptible to parasitics. The junction parasitic capacitors from the switches and buffer input capacitors are the dominant contributors to parasitics. For the same reason, the unit capacitors used were on the order of a few pico-farads. This demands a large power for the recycling buffers, thus degrading the efficiency. With the technology scaling (90 nm), the issue can aggravate, when the ADC is to be built for low-voltage operation (1 V). The voltage-dependent nature of their capacitances is one of the major contributors to ADC non-linearity. Schemes have been proposed to generate reference voltages that are least sensitive to parasitics and are explained as follows.

4.1 V_{MID} generation

Consider the V_{MID} [9] generating circuit in figure 5. The nodes 1, 2 have parasitic capacitance to ground due to

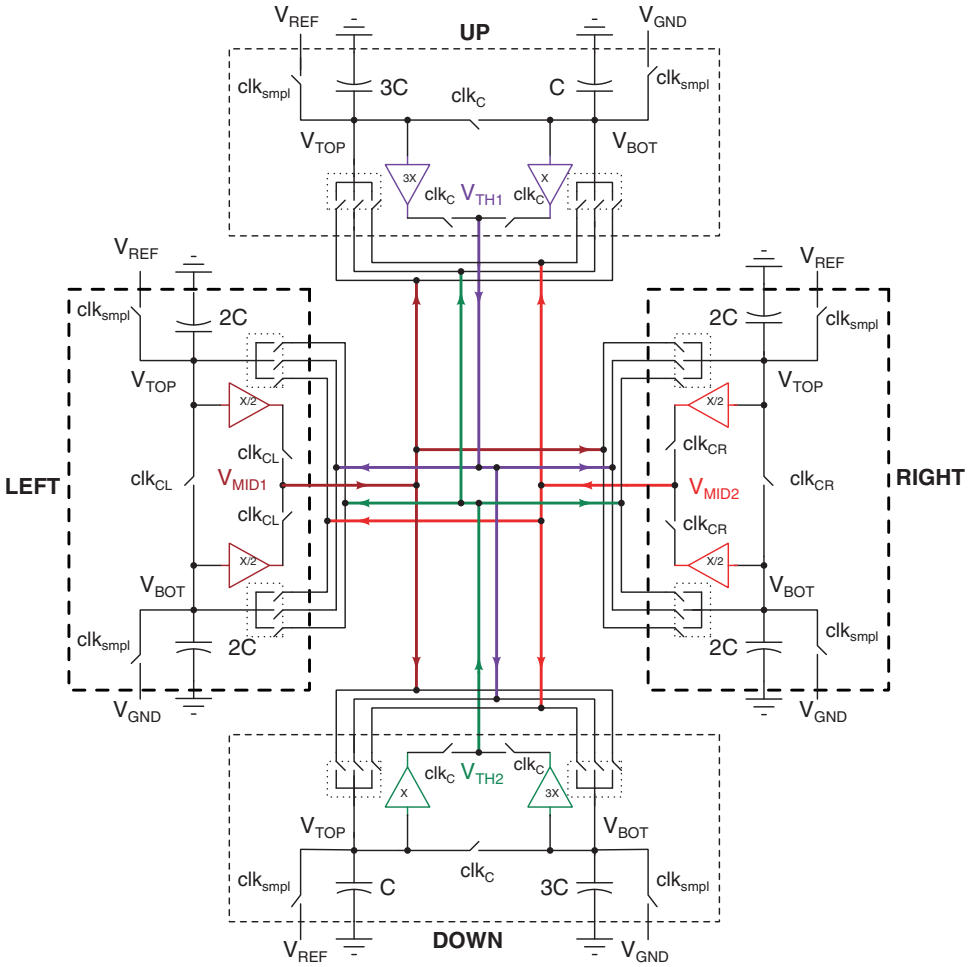

Figure 4. Proposed DAC architecture to evaluate 2 bits per cycle.

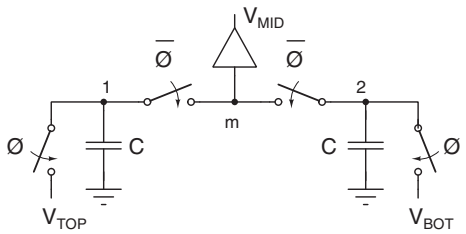

Figure 5. Switched capacitive network for V_{MID} generation.

switches, say C_{p1} and C_{p2}, respectively. The node m will have a parasitic capacitance (C_{pm}) due to switches and the buffer. During the phase ϕ, nodes 1 and 2 are connected to V_{TOP} and V_{BOT}, respectively, while the node m will be at a potential equal to V_{MID} corresponding to the previous cycle. This state is shown in figure 7 for the n^{th} cycle, along with the parasitic capacitance. In $\overline{\phi}$, voltages sampled at nodes 1 and 2 are shared to generate V_{MID}. This state is shown in figure 8. Note that here, C'_{pm} shows the equivalent parasitic

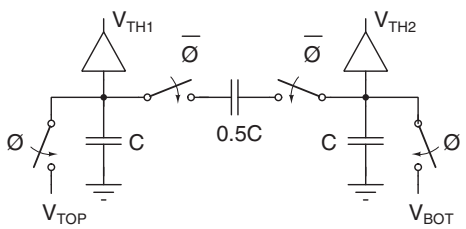

Figure 6. Switched capacitive network generating V_{TH1} and V_{TH2}.

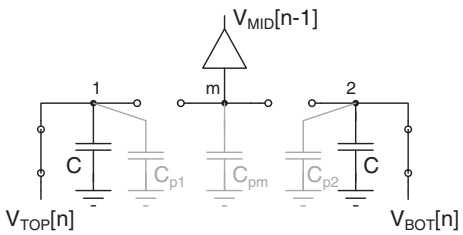

Figure 7. V_{MID} generation circuit of figure 5 in the presence of parasitics during ϕ phase.

at node m. The voltage at node m at the end of n^{th} cycle is given by

$$V_{MID}[n] = \frac{2CV_{MID,ideal[n]}}{C_{tot}} + \frac{C_{p1}V_{TOP}[n]}{C_{tot}} + \frac{C_{p2}V_{BOT}[n]}{C_{tot}} + \frac{C_{pm}V_{MID}[n-1]}{C_{tot}} \tag{4}$$

where $V_{MID,ideal}[n] = \frac{V_{TOP}[n]+V_{BOT}[n]}{2}$ is the ideal voltage expected at node m and $C_{tot} = 2C + C'_{pm}$ is the equivalent capacitance at node m during $\overline{\phi}$. It can be observed that V_{MID} generated at the end of each cycle is in error and more seriously, the error accumulates from the previous cycle.

The error $\Delta V[n] = V_{MID,ideal}[n] - V_{MID}[n]$ is given in (5):

$$\Delta V[n] = \frac{V_{TOP}[n](C'_{pm} - 2C_{p1})}{2C_{tot}} + \frac{V_{BOT}[n](C'_{pm} - 2C_{p2})}{2C_{tot}} - \frac{C_{pm}V_{MID}[n-1]}{C_{tot}}. \tag{5}$$

If the circuit is symmetric and the parasitic capacitances are assumed to be voltage independent; then $C_{p1} = C_{p2}$ and $C'_{pm} = C_{p1} + C_{p2} + C_{pm}$. In such a case, $\Delta V[n]$ simplifies to

$$\Delta V[n] = \frac{C_{pm}}{C_{tot}}(V_{MID,ideal}[n] - V_{MID}[n-1]). \tag{6}$$

From (6), the worst case error occurs at the first cycle assuming $V_{MID}[n-1] = 0$ and is given by $\Delta V_{max} = \frac{C_{pm}}{C_{tot}}\frac{V_{REF}}{2}$. Minimization of this error demands a large value of C at least on the order of a few pico-farads. A careful look at the results given earlier reveals that the parasitic capacitance at node m is responsible for the error and its accumulation. A modification to the circuit in figure 5 is proposed that can make the V_{MID} generation insensitive to parasitics if the parasitics are voltage independent. The proposed circuit is shown in figure 9. Here, the buffer is split into two and they are directly driven by nodes 1 and 2, thereby eliminating node m. Both the nodes 1 and 2 see equal parasitics. The effect is that the error in V_{MID} generated is zero. With the voltage-dependent parasitics, V_{MID} is bound to have an error and is given in (7). It can be seen that the error is proportional to the difference in parasitic capacitances between the nodes 1 and 2. The result is that the requirement on C is relaxed to a large extent. Another point to note is that the error does not accumulate.

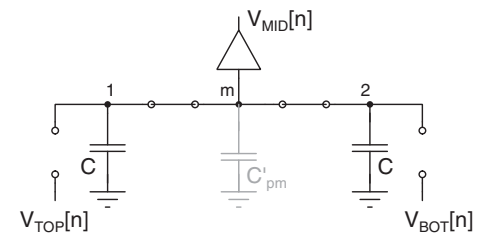

Figure 8. V_{MID} generation circuit of figure 5 in the presence of parasitics during $\overline{\phi}$ phase.

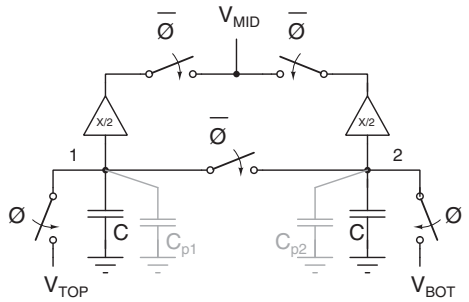

Figure 9. Proposed V_{MID} generation circuit.

$$\Delta V[n] = \frac{(C_{p1} - C_{p2})}{2C_{tot}}(V_{TOP} - V_{BOT}). \tag{7}$$

The value of unit capacitor C in LEFT/RIGHT block not only decides error in V_{MID} generation but also the noise contribution from the DAC.

Firstly, to minimize the error in V_{MID} generation due to parasitic capacitances at charge sharing nodes of SC circuit, the difference in parasitic capacitances at charge sharing nodes must be as low as possible as seen in (7). To limit this error within $0.1V_{LSB}$,

$$C/(C_{p1} - C_{p2}) > 640. \tag{8}$$

Secondly, the thermal noise due to ON state resistance of switches at charge sharing node at the end of N_c clock cycles is

$$N_c\sqrt{KT/C} \tag{9}$$

where N_c is the number of clock cycles for N bit resolution.

To limit this noise voltage within αV_{LSB} where α is a fraction,

$$C > (N_c/\alpha)^2 KT/(V_{LSB})^2. \tag{10}$$

If α is considered as 0.1 as before,

$$C > 17.36\,\text{fF}. \tag{11}$$

To limit these errors to a safe value, we decided to use C = 200 fF, to which permissible parasitic variation is less than 0.312 fF. Figure 10 shows the error in V_{MID} normalized to LSB of an 8-bit ADC with V_{REF} = 0.5 V for input in 1st and 4th quadrants of the first cycle. The unit capacitor C used in the DAC is 200 fF. With the scheme shown in figure 5, the error is found to be as high as 1.55LSB. However, with the proposed scheme, the error is limited to less than 0.1LSB even with a small capacitance of C = 200 fF. It is to be

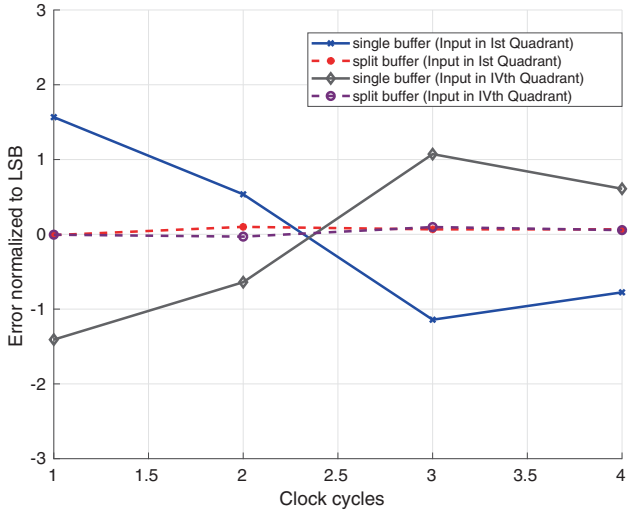

Figure 10. Simulated error in V_{MID} generation with single buffer and split buffer.

noted that the 0.1LSB error is due to the combined effect of the complete DAC circuit, which includes error due to buffer settling, charge injection, clock feed-through and voltage-dependent parasitics.

4.2 V_{TH1} and V_{TH2} generation

The flash references V_{TH1} and V_{TH2} generated using the circuit shown in figure 6 are also prone to errors in the presence of switch and buffer parasitics. This can be mitigated by the circuit shown in figure 11. The buffers for recycling V_{TH1} and V_{TH2} can be driven by either of the nodes of the respective circuits, i.e. the buffer recycling V_{TH1} can be driven by either node X or Y. Note that the buffers are split in the ratio 1:3 such that the ratio of parasitics introduced at the nodes remains the same. Dummy switches have been added to make the switch parasitic capacitances also to appear in the same 1:3 ratio. The switch connected to V_{TOP} also needs to be sized three times that connected to V_{BOT}. A similar arrangement can be used for generating V_{TH2}. The scheme presented earlier makes the threshold generation insensitive to parasitic capacitance

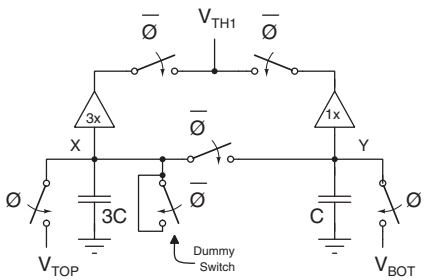

Figure 11. Proposed parasitic-insensitive circuit to generate V_{TH1}.

if the parasitics are voltage independent. Considering voltage-dependent parasitic capacitance, the error in the voltage V_{TH1} generated at the end of n^{th} cycle can be written as in (12):

$$\Delta V_{TH1} = \frac{3}{4}\frac{V_{TOP}}{C_{tot,XY}}\left(C_{p,XY} - \frac{4}{3}C_{p,X}\right) + \frac{1}{4}\frac{V_{BOT}}{C_{tot,XY}}\left(C_{p,XY} - 4C_{p,Y}\right). \tag{12}$$

Here, V_{TOP} and V_{BOT} correspond to n^{th} cycle, $C_{p,X}$ and $C_{p,Y}$ are the parasitic capacitance at node X and Y, respectively, during ϕ phase, $C_{p,XY}$ is the total parasitic capacitance at nodes X and Y during $\overline{\phi}$ phase and $C_{tot,XY} = 4C + C_{p,XY}$. Figure 12 shows the error in V_{TH1} and V_{TH2} voltages normalized to LSB of an 8-bit ADC with V_{REF} = 0.5 V, for a few cases of input voltages in three different quadrants. Simulation results show that the error is limited to less than 0.125LSB even with a small capacitance of C = 100 fF.

5. Resolution programmability

In conventional SAR ADC using capacitor array DAC, there are two approaches to program the resolution. First [3], start the bit recycling from MSB capacitor and stop at the desired resolution. Because of large MSB capacitor, the energy required is higher. The second approach [4] is to start recycling from the middle of the array towards the LSB capacitor. This method requires the MSB capacitor to be isolated, which otherwise would offer attenuation, demanding higher accuracy for the comparator.

The proposed DAC architecture supports resolution reconfigurability with ease, since the hardware used in the DAC (capacitors, switches or analog blocks) are independent of resolution. The S/H, comparator and DAC are to be

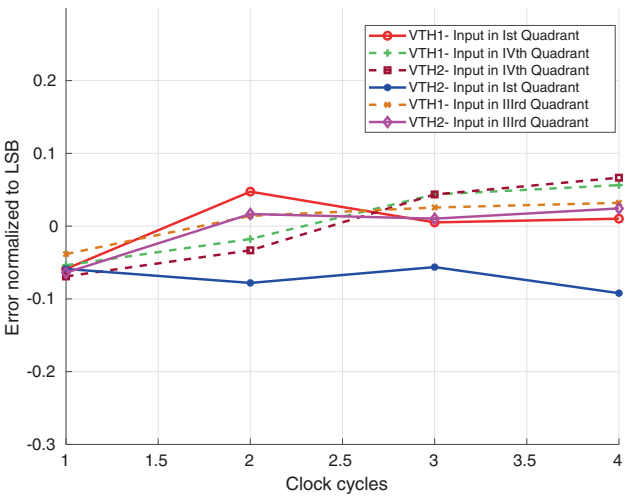

Figure 12. Simulated error in threshold generation with the proposed method, for V_{IN} in in three different quadrants.

designed for the accuracy demanded by the highest resolution, a requirement similar to that for the conventional approach. Since comparator resolution and buffering accuracy are designed to support ADC resolution up to 8 bits in this work, clocking scheme and control logic are modified to suit programmable resolution. Using FSM circuit, a sampling clock is generated to sample signal after every 2, 3 and 4 cycles of the system clock as shown in figure 3 (clksmpl2, clksmpl3 and clksmpl4) to achieve a programmability of 4–8 bits. Resolution is selected digitally by resolution select bits X[1:0]. Accordingly, the FSM block generates clk_{smpl} for the S/H block. Therefore sampling rate increases as the ADC resolution decreases. Resolution is variable from 4 to 8 bits in 1-bit increment. In each of these resolution modes, sampling rate can be lowered down to 60% from its peak sampling rate. The leakage at nodes V_{TOP} and V_{BOT} in each of the SC block poses lower limit on the sampling rate.

6. Building blocks of 2 bits per cycle SAR ADC

6.1 *Buffer*

The buffers required to recycle the charges for generating 2-bit flash references are realized by connecting an OTA in unity feedback configuration. To limit the buffer error to less than 1/8th of an LSB at 8-bit resolution for a full-scale voltage of 0.5 V, it is desirable to have a gain in excess of 70 dB for the OTA. A two-stage OTA with a folded cascode first stage has been designed, whose circuit is shown in figure 13. Transistor sizes are decided to maximize the voltage gain as well as to meet the signal swing requirement. Transistors M_1–M_9 form the first-stage folded cascode amplifier and M_{13}–M_{16} form the second stage. Approximate gain of first stage (Av_1) and the second stage (Av_2) is given by (13) and (14), respectively:

$$Av_1 \cong g_{m2} r_{o9}, \tag{13}$$

$$Av_2 \cong g_{m13}[g_{m14} r_{o13} r_{o14} || g_{m15} r_{o15} r_{o16}]. \tag{14}$$

Transistors M_{10}–M_{12} form a part of biasing circuit of first and second stage of the op-amp. In order to extend the input range of the amplifier and hence the DAC, the bias current through the folded cascode stage is made to depend on input voltage instead of fixed bias scheme. Here the bias current through M_6 and M_7 is made to track the variations in the current of M_3 (the tail transistor) occurring due to channel length modulation at large input signals. When used as unity gain buffer, this is important since for large signals, common mode rejection is degraded [10], affecting the input range. The use of M_{11} with its gate driven by the V_{ip} input will force the current of M_{10} to follow that of M_3, thus improving the common mode rejection and the input range. The loop is compensated by adding capacitor between output node to the folding node. The drain to source resistance of M_5 acts as resistance in series with the capacitor, and thus helps in compensating for the right half plane zero appearing at $(g_{m13})/C$. The offset correction scheme shown in figure 14 has been used to minimize buffering error due to offset voltage. The offset is stored on to C during sample phase (ϕ) of clk_{smpl} and corrected during hold phase ($\overline{\phi}$). Figure 15 shows frequency response of two-stage OTA. The overall DC gain obtained is 76.9 dB for typical process corner, which includes first-stage gain of 28.7 dB and the second-stage gain is 48.2 dB. The unity gain bandwidth of OTA is 70 MHz. The gain margin and phase margin are found to be 15 dB and 55°, respectively. The maximum error in buffer output voltage for the intended input range of 0.5 V over an equal common-mode voltage is found to be less than 120 μV (< 0.1LSB). The total input-referred noise of buffer is found to be 6.17 nV^2. The response of buffer for a square wave input with a capacitive load of 600 fF is shown in figure 16. Slew rates of 4.78 and 48.5 V/μs with settling time of 110 and 30 ns, respectively, have been achieved with this load. The overall performance parameters of OTA are listed in table 1.

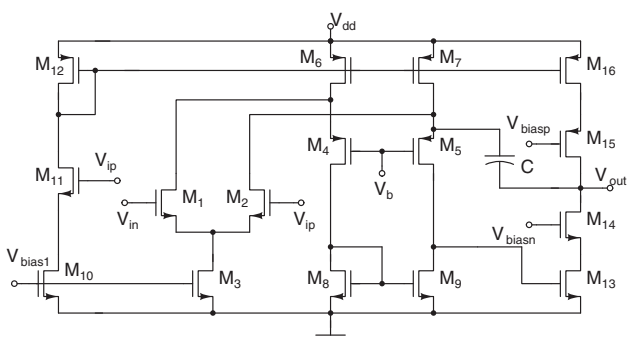

Figure 13. Schematic of the two-stage OTA for the buffer.

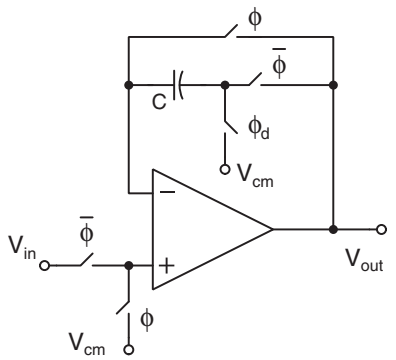

Figure 14. Buffer with offset correction circuit.

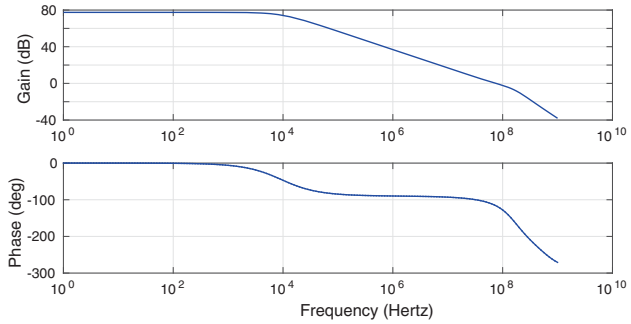

Figure 15. Frequency response of low-power OTA with compensation.

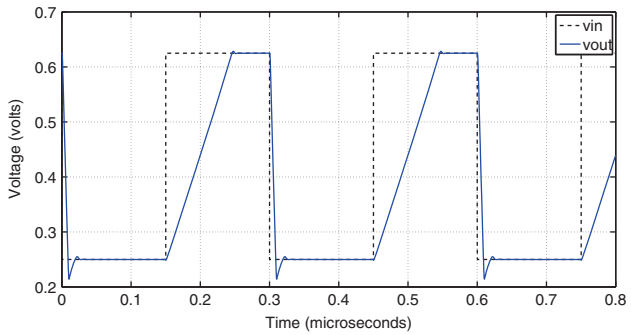

Figure 16. Transient response of the buffer.

Table 1. Performance summary of low-power OTA.

Performance metric	*Value*
DC gain [dB]	76.98
Gain margin [dB]	15
Phase margin [deg]	55
Power dissipation [μW]	16
Load capacitance [fF]	600
PSRR [dB]	54.7
CMRR [dB]	80

6.2 *Comparator*

The comparator used for two-bit flash is realized by cascading two pre-amplifier stages followed by a latch. Schematics of the comparator pre-amplifier and dynamic latch used in this work are shown in figure 17. The pre-amplifier is realized using a simple nMOS differential amplifier with pMOS resistor loads. One of the input comes from input sample and hold circuit and the other from the DAC. Both of these inputs reside on a DC of 0.5 V, resulting in an input common mode voltage of 0.5 V, for the pre-amplifier. Each pre-amplifier has been designed to offer a gain of 6 dB. The operation of dynamic latch is

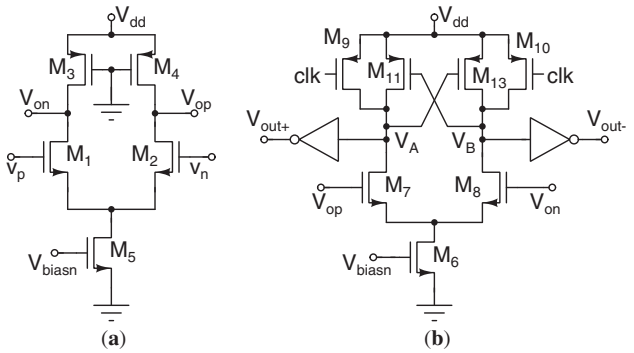

Figure 17. Comparator: (a) pre-amplifier stage and (b) dynamic latch stage.

explained as follows: during *clk* low phase, nodes V_A and V_B are forced to V_{dd} by M_9 and M_{10}. When clk goes high, these nodes slew towards ground at unequal rates decided by the input differential voltage. When the node voltages are low enough, pMOS positive feedback load devices M_{11} and M_{12} turn on and latch the comparator. The output inverters restore the comparator outputs to logic levels. The power consumption of the comparator is 8.4 μW with resolution of ±100 μV. Two pre-amplifier stages followed by a latch stage help not only in minimizing offset of latch stage but also in achieving overall resolution of 10 bits for the comparator. Dynamic offset voltage of overall comparator is found to be 80 μV, which is well within $0.1V_{LSB}$. By careful device matching during layout as well as slightly over-designing overall resolution of the comparator, the offset calibration technique is avoided in this work.

6.3 *Switch bootstrapping sample and hold*

To improve dynamic performance of the ADC, a switch bootstrapping [11] sample and hold, shown in figure 18(a), has been used. The circuit uses a charged capacitor to sustain the gate to source voltage of M_1 during ON phase. The switch M_6 grounds the gate of the switch M_1 during OFF phase and, at the same time, switches M_3 and M_4 charge the boot strapping capacitor to the supply voltage. Switch M_5 and transmission gate (TG) switch connect the gate and drain of M_1 during ON state with boosted gate

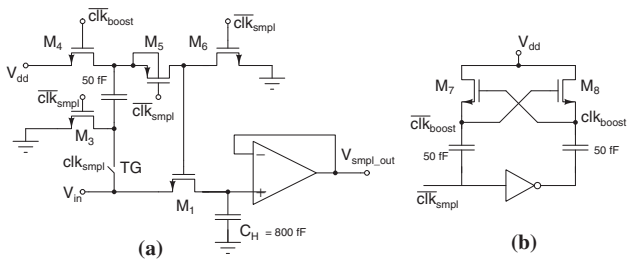

Figure 18. (**a**) Switch bootstrapping sample and hold. (**b**) Clock booster.

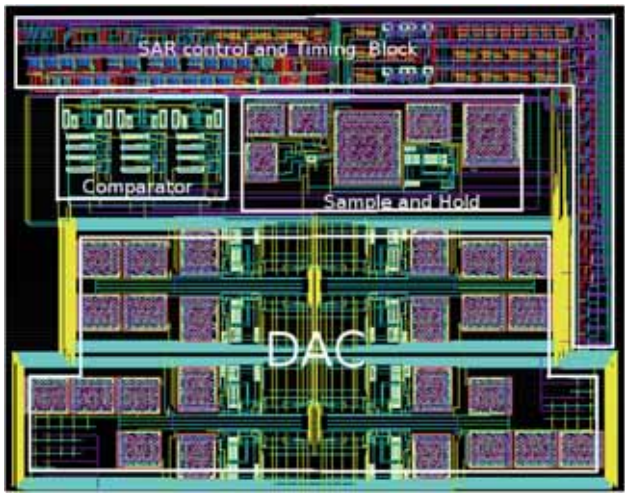

Figure 19. Layout of the ADC.

voltage. Each of the switches used must have appropriate gate drive in order to ensure proper switching and suitable protection for the drains that undergo large voltage swings. Since switch M_4 is an NMOS transistor, its gate requires a voltage higher than V_{dd} for it to turn ON. Therefore a voltage doubler made by a cross-coupled pair M_7–M_8 with charge pumping capacitors as shown in figure 18(b) is used. The gates of M_7 and M_8 are driven by the clock and complemented clock signal.

7. Simulation results

The proposed programmable-resolution 2-bit-per-step SAR ADC has been designed in UMC 90 nm CMOS process to operate on 1 V supply. The layout of the ADC is shown in figure 19 and the area occupied is 0.06182 mm^2 (281 µm × 220 µm). The post-layout simulation results show that ADC achieves a conversion speed of 1.2 MS/s in 7/8-bit mode and 2.4 MS/s in 4-bit mode. The total capacitors used in the DAC are 16C where C is the unit capacitor of value 100 fF, thanks to the parasitic-insensitive reference generation scheme, which otherwise would have demanded a C of at least a couple of pico-farads. Also, 100 fF has been used for unit capacitors only to minimize the effect of voltage-dependent parasitics. Compared with conventional charge redistribution DAC architecture, which requires 256C for 8-bit resolution, this DAC offers large savings in terms of area, headroom on capacitor mismatch and parasitic requirements. From static performance of ADC (code density test) in 8-bit mode, DNL and INL of the ADC at 1.2 MS/s sampling speed are found to be within 0.7LSB/–0.5LSB and 0.3LSB/–0.8LSB, respectively, and are shown in figures 20 and 21, respectively.

The output spectra of the ADC for an input full-scale sine wave at 13.95 kHz (near DC) and 525.48 kHz (at Nyquist)

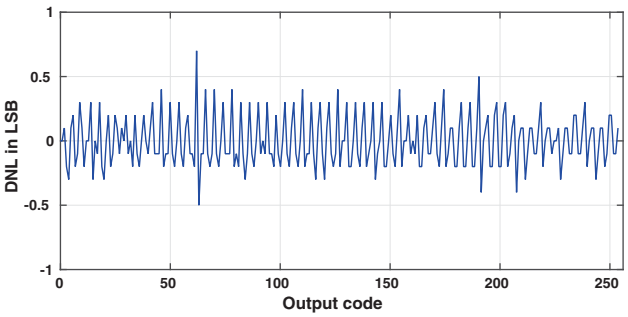

Figure 20. DNL error in 8-b mode.

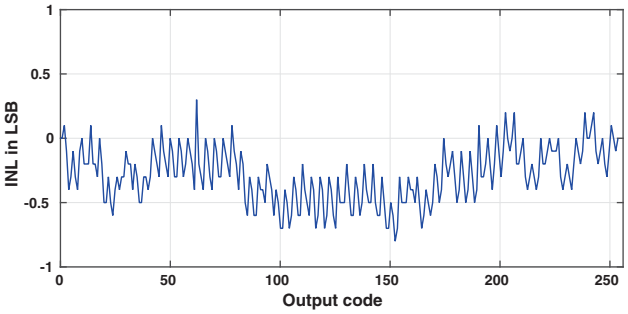

Figure 21. INL error in 8-b mode.

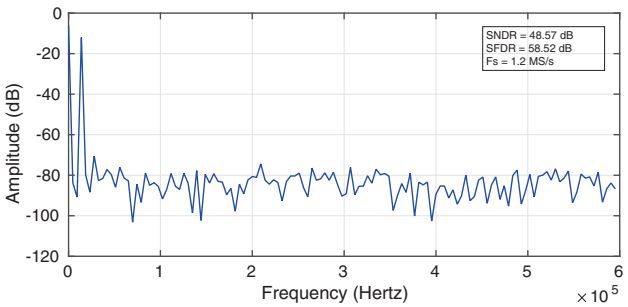

Figure 22. FFT spectrum of 8-b ADC for an input frequency of 13.95 kHz.

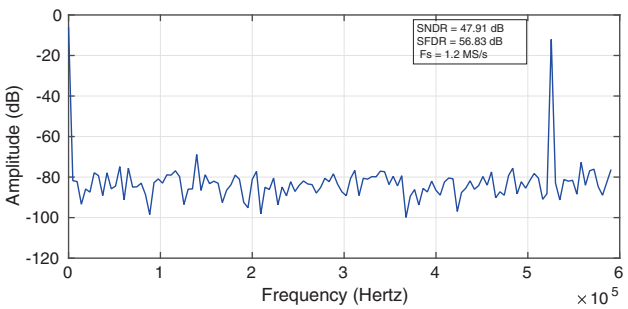

Figure 23. FFT spectrum of 8-b ADC for an input frequency of 525.48 kHz.

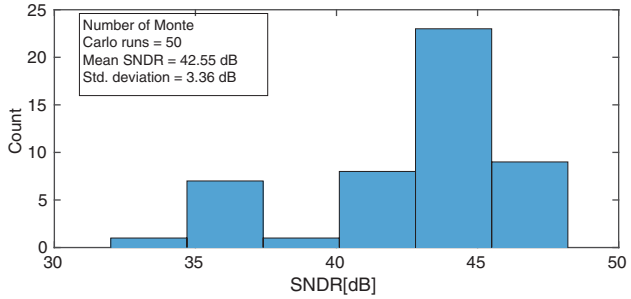

Figure 24. Mean and sigma SNDR against mismatch in buffers.

Table 2. Performance of ADC at different process corners.

Parameter	tt	ff	ss	snfp	fnsp
SNDR(dB)@DC	48.6	46.3	49.9	41.8	47.6
SNDR(dB)@Nyq.	47.9	46.0	49.3	41.3	48.6

Table 3. Performance of ADC at different supply voltages.

Parameter	0.9 V	1 V	1.1 V
SNDR(dB)@DC	48.9	48.57	47.15
SNDR (dB)@Nyquist	47.43	47.9	46.89
Power (μW)	178.5	185	190.4

Table 4. Performance of ADC at different temperatures.

Parameter	0°C	27°C	70°C
SNDR(dB)@DC	48.82	48.57	48.14
SNDR (dB)@Nyquist	47.91	46.02	48.1

are shown in figures 22 and 23, for which the SNDRs of 48.57 dB (ENOB = 7.77) and 47.9 dB (ENOB = 7.66) are obtained, respectively. The total power consumption of ADC is 185 μW. Further reduction in power is possible by turning the two split buffers off during recycling phase. This is possible since only two of the four buffers in the DAC are used during the recycle phase. This would result in a power of 130 μW. To verify ADC performance against mismatch in buffers used in the DAC, Monte Carlo simulations of 50 runs are carried on the extracted netlist. Figure 24 shows the histogram plot of SNDR variations. The mean and sigma values of SNDR are 42.55 and 3.36 dB, respectively. The plot shows that the proposed ADC architecture is mismatch tolerated to a large extent.

ADC performance for various process corners is given in table 2. ADC is found to offer consistent performance across corners at nominal temperature and 1 V supply.

The power consumption of ADC and the dynamic performance are recorded in table 3 for supply voltage variation by ±10%.

The ADC performance for temperature variation from 0 to 70°C is tabulated in table 4. The designed programmable-resolution SAR ADC performance is compared to those of some of the SAR ADCs in the literature as shown in table 5. The FOM used for the comparison is computed using formula (15) [8]:

$$\text{FOM} = \frac{P_{diss}}{2^{ENOB} \times 2f_{in}} \tag{15}$$

where P_{diss} is the power dissipation, f_{in} is the input frequency and ENOB is the effective number of bits. It can be seen that the proposed SAR ADC has FOM comparable to those of some of the SAR ADCs found in the literature. A lower FOM indicates higher power efficiency. Moreover, the designed programmable-resolution ADC occupies small area compared with a few state-of-art designs. The performance of ADC at different resolutions is shown in table 6. The sampling rate at 4-bit resolution setting is 2.38 MS/s and consumes 132 μW. At low resolution with relaxed noise and linearity requirements, use of an increased clock speed improves energy efficiency. Hence, FOM is degraded by only 4.7× from 8-bit to 4-bit operation. This is a significant improvement over 16× degradation expected from 8-bit to 4-bit resolution scaling by

Table 5. Comparison with available low-power, low-voltage, SAR ADCs in the literature.

Ref.	Tech. (μm)	V_{dd} (V)	F_s (MS/s)	ENOB (@fin)	P_{diss} (μW)	FOM (fJ/conv.)	Area (mm^2)	AE (μm^2)	C_u (fF)	C_{tot} (pF)
[2][1]	0.065	0.55	0.02	8.84	0.206	22.4	0.22	480.08	65	6.24
[4][1]	0.13	1	0.1	7.55	0.9	48	0.09	480.24	20	5.12
[12]	0.13	1.2	1	8.39	150	2213	0.18	536.37	15	15
[13][1]	0.13	1	1	7.7	8.8	42.3	0.16	769.46	15	3.84
[14]	0.09	1.8	50	7.2	6000	816	0.4	2720	15	1.4
[15]	0.18	0.9	1	8.38	7.16	8007	0.48	1440.82	–	–
[16][2]	0.13	1.2	1250	5.6	32000	800	0.09	1855.55	5	0.24
[17][2]	0.045	1.25	1000	6.48	73000	80	0.16	179.24	5	0.6
This work[1, 2]	*0.09*	*1*	*1.2*	*7.66*	*185*	*762*	*0.06*	*305.66*	*100*	*1.6*

[1] Variable-resolution SAR ADC.

[2] 2 b/step SAR ADC

Table 6. Performance summary of ADC at different resolutions.

Resolution mode	4-b	6-b	8-b
Maximum sampling frequency [MS/s]	2.38	1.6	1.2
SNDR@dc [dB]	25.49	37.64	48.57
SFDR@dc [dB]	35.53	50.36	60.96
ENOB@dc	3.94	5.96	7.77
SNDR@Nyquist [dB]	25.58	37.5	48.2
SFDR@Nyquist [dB]	34.76	50.13	54.2
ENOB@Nyquist	3.95	5.9	7.66
Power [μW]	132	161	185
FOM [fJ/conversion-step]	3588	1685	762
FOM [variable-resolution DAC]↑	4.7×	2.2×	1×
FOM [fixed-resolution DAC] ↑	16×	4×	1×

truncating the bits in conventional SAR ADC for variable-resolution mode.

8. Conclusion

A 4-to-8-bit programmable-resolution, 2-bit-per-cycle SAR ADC has been presented. The ADC uses a DAC whose architecture is resolution independent, which makes the ADC programmability almost trivial. The proposed DAC architecture uses a few non-binary capacitors, and therefore there is an area advantage over the conventional binary weighted capacitor array architecture. Though the buffers required for the DAC demand a higher power, with a careful design of buffers, the overall efficiency is maintained on par with the existing 8-bit architectures. The DAC architecture proposed is made parasitic independent to a large extent. Post-layout simulation results of the ADC designed in 90 nm CMOS process operating on 1 V supply offered an ENOB of 7.77 near DC for an 8-bit setting while it was 3.94 in 4-b mode at DC. Degradation in FOM is only 4.7× for a resolution change from 8 to 4 bits when compared with 16× offered by truncating the bits. The proposed ADC is suitable for modern instrumentation systems and data acquisition systems.

Acknowledgements

Authors would like to thank Ministry of Electronics and Information Technology (MeitY), Government of India, for providing EDA tools through SMDP-VLSI Project.

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