# One Cycle Controlled Bridge-less SEPIC Converter Fed BLDC Motor Drive

Sonu Jayachandran, Pavana and Vinatha U
Department of Electrical & Electronics Engineering
National Institute of Technology, Karnataka, Surathkal

***Abstract*—This paper presents a One Cycle Controlled (OCC) Bridge-less (BL) SEPIC converter fed Brush-Less DC (BLDC) motor drive for air conditioning application. The speed control of proposed drive is obtained by Pulse Amplitude Modulation (PAM) of three-phase Voltage Source Inverter (VSI). The Pulse Amplitude Modulation is facilitated by the DC bus voltage variation via duty ratio modulation of BL-SEPIC converter switches. A non-linear technique called One Cycle Control (OCC) is used to accomplish the duty ratio control of BL-SEPIC converter. Autoshaping of supply current is achieved by designing BL-SEPIC converter to ensure Discontinuous Inductor Current Mode (DICM) operation. The Total Harmonic Distortion (THD) of supply current is maintained within the limits as specified by IEC-61000-3-2. The proposed system is designed and simulated in MATLAB/Simulink environment and its performance is analyzed for speed control over a wide range.**

**Index terms—Bridge-less SEPIC, BLDC motor, DICM, One Cycle Control.**

## I. Introduction

The rising living standards and urbanization have lead to the global upsurge in demand for air conditioning systems. This resulted in air conditioning load being one of the major part of global electricity demand. Conventionally, compressors for air-conditioners utilize single phase Induction Motors with ON/OFF type control. That is, either it will deliver rated power or it will be turned OFF based on thermostat output. Advances in power electronics and semiconductor devices have enabled the use of adjustable speed drives in air-conditioning systems which employ inverters in conjunction with embedded electronics/DSP systems for speed control. Even though this inverter technology is costlier, it is superior to conventional ON/OFF control owing to its advantages like high energy saving capability, ozone friendly, comfortability and low noise. Recent developments in this area are focused on achieving improved motor efficiency, high power density and superior performance at a lower cost. Considering this scenario, BLDC motors are replacing conventional motors in air conditioning applications by virtue of their advantages such as high torque/inertia ratio, high energy efficiency, low maintenance, ruggedness etc. [1]. A BLDC motor comprises of permanent magnets in the rotor and three-phase winding in the stator. BLDC motor is also mentioned as electronically commutated motors since stator windings are energized via a three phase voltage source inverter (VSI) based on rotor position information [2].

The conventional BLDC drive involves a single-phase AC supply feeding the motor-inverter assembly via a Diode Bridge Rectifier (DBR). In this scheme, generally the speed control of BLDC motor is attained by pulse width modulation (PWM) of inverter switches. This method is characterized by disadvantages such as high switching losses in VSI, increased sensor requirement, poor power factor and increased distortion in the input current etc. In order to resolve issues related to power quality at AC mains, a Power Factor Correction (PFC) converter is used in between DBR and three-phase VSI. Another method to attain BLDC motor speed control is Pulse Amplitude Modulation of VSI. PAM based speed control allows VSI to be operated in low frequency, thus reducing switching losses and eliminates the current sensor requisite which is needed in PWM scheme of control. Therefore, a PFC converter with wide voltage modulation ratio will enable the PAM based speed control of BLDC motor, thus reducing switching losses and improving power quality of AC mains [2].

State-of-the-art of PFC converters has been described in various works of literature [3], [4]. Among this, the Bridge-less topologies have gained popularity since they reduce conduction loss at the front end. The buck and boost configurations amidst this can provide only either step-up or step-down operation. Thus, the wide variation of DC bus voltage is not possible in these configurations [5]. Since PAM based speed control requires a wide range of voltage variation, bridge-less buck-boost configurations such as Cuk, SEPIC, Zeta etc. are commonly used. However, the buck-boost and Cuk converter provide negative output voltage polarity that produces complexity in gate driver design [6] and Zeta converter is affected by higher EMI issues due to the series connected switch [7]. Among the buck-boost configurations, SEPIC provides a good alternative with lesser EMI issues and simple gate driver designs [8], [9].

The PFC converter has two modes of operation termed as 1) Continuous Inductor Current Mode (CICM) and 2) Discontinuous Inductor Current Mode (DICM). In comparison, latter has reduced sensor requirement and achieves power factor correction inherently while former has low stresses on converter switches [10]. Thus, a trade-off must be done to choose the operating mode based on the power requirement.

978-1-5386-3864-4/17/$31.00 

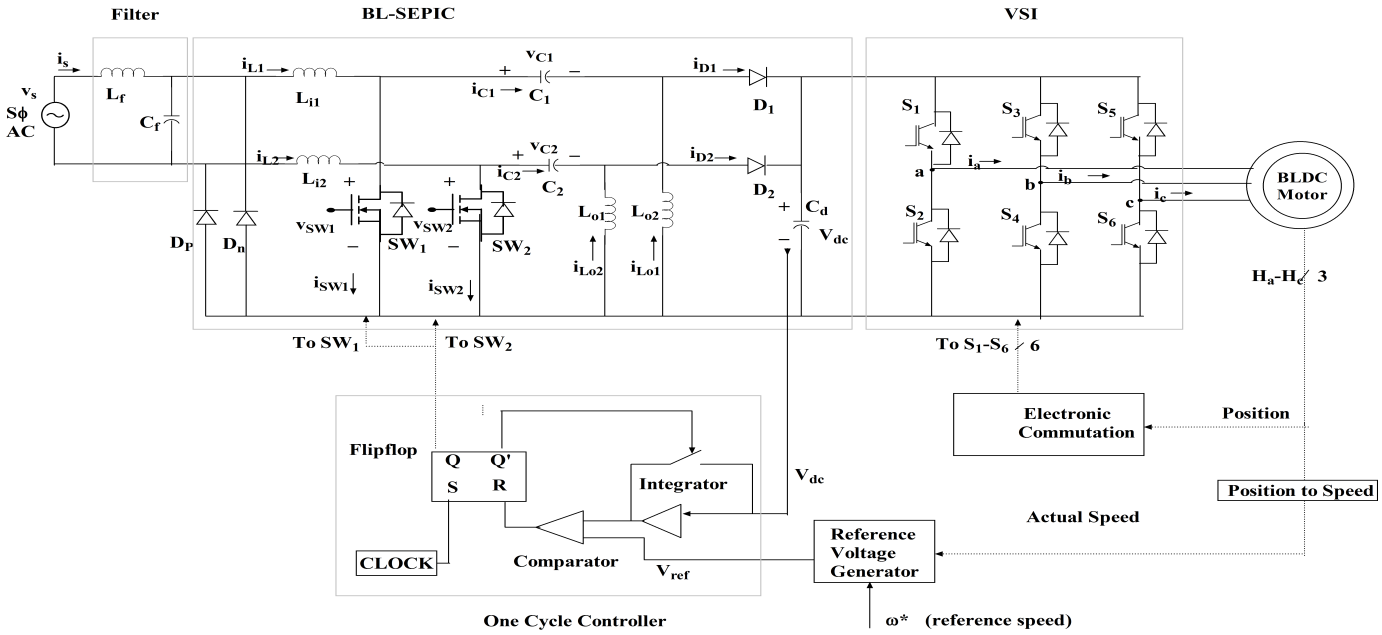



Figure 1: Proposed One Cycle Controlled BL-SEPIC fed BLDC drive

This paper put forward a BLDC motor drive for air conditioning application fed from AC mains via a DICM Bridgeless SEPIC PFC converter. The PAM method enables the speed control of BLDC drive and three-phase VSI is operated at fundamental frequency with 120° conduction. The PAM control requires wide variation of DC bus voltage of the three-phase VSI. Voltage variation at DC bus is realized by duty ratio control of BL-SEPIC switches. A non linear technique termed as One Cycle Control is employed to achieve the duty ratio modulation [11]. The objective of this paper is to implement the proposed One Cycle Controlled BL-SEPIC fed BLDC motor drive in MATLAB/Simulink environment and to analyze the performance during steady state and dynamic conditions.

## II. Proposed Adjustable Speed Drive System

Figure1 represents the schematic for proposed One Cycle Controlled BL-SEPIC fed BLDC motor drive. Partial elimination of DBR reduces conduction losses at the front end. A single-phase AC supply feeds the BL-SEPIC converter via an LC filter. The BL-SEPIC converter is designed such that DICM operation is ensured to achieve inherent current shaping at the input. The converter output is used to feed BLDC motor via a three-phase VSI. The BLDC motor is electronically commutated based on position information from hall sensor signals. The BLDC motor speed is controlled by modulation of DC bus voltage. A non-linear technique called One cycle control is used to obtain modulation of DC bus voltage.

### *A. Operation Of BL-SEPIC Fed BLDC motor Drive*

The Bridge-less SEPIC AC-DC converter consists of two SEPIC arms. Diode $D_p$, Inductor $L_{i1}$, Switch $S_{W1}$, Capacitor $C_1$, inductor $L_{01}$, diode $D_1$, operates for the positive half cycle. Similarly, $D_n$, $L_{i2}$, $S_{W2}$, $C_2$, $L_{02}$, $D_2$ operates for the negative half cycle of the AC mains voltage. The operation of BL-SEPIC during positive half cycle of AC input is shown in Figure 2. Waveforms corresponding to an entire line cycle operation and a full switching cycle operation is represented in Figure 3a and 3b respectively.

A SEPIC converter operating in DICM has three stages of operation. Considering positive half cycle, these three stages are explained as follows

*Stage I: Switch ON, Diode OFF:-* At the instant when the switch turns ON, the supply starts charging the input inductor. The energy transferring capacitor discharges through output inductor via the switch. The diode $D_1$ is in reverse biased state and the DC bus capacitor $C_d$ feeds the BLDC load. Therefore, in this mode the inductor currents increase and capacitor voltage decreases which is illustrated in Figure 3b.

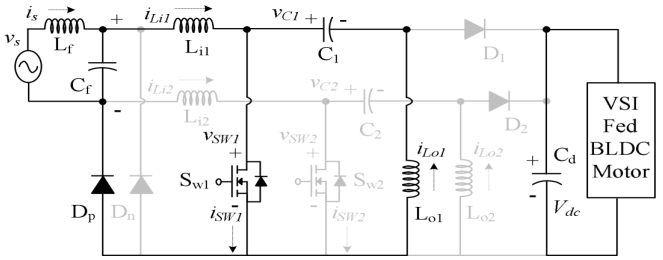
*Stage II: Switch OFF, Diode ON:-* At the instant when the switch turns OFF, both input and output inductors discharge through the load. Diode $D_1$ is ON during this mode. The energy transferring capacitor $C_1$ and DC bus capacitor $C_d$ charges during this mode. Therefore, in this mode $I_{l1}$ and $I_{l2}$ decreases and $V_{C1}$ and $V_{dc}$ increases.

*Stage III: Switch OFF, Diode OFF:-* At the end of stage II, the output inductor enters DICM as it is completely discharged. Now the input inductor discharges through output inductor via $C_1$ making both inductor currents same but opposite in magnitude. Both switch and Diode $D_1$ is off during this mode. The DC bus capacitor feeds the motor load.

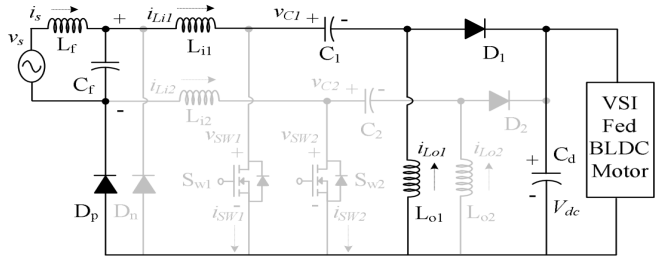
Similarly, in negative half cycle same operation happens with lower SEPIC arm.

### *B. Design of BL-SEPIC Converter*

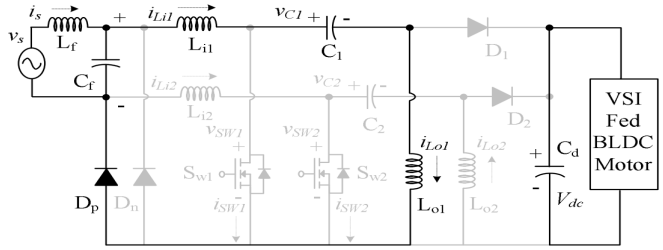
A 0.5 hp BLDC motor is selected for the experiment (Complete parameters given in Appendix). The BL-SEPIC converter




(a)




(b)




(c)

Figure 2: BL-SEPIC converter operation in positive half cycle

is designed for a rated power of 500 W. The converter is designed to accomplish a voltage variation from 70 V - 310 V at DC bus. The output inductors are designed to ensure DICM operation even at lower DC bus voltages.

The DC bus voltage $V_{dc}$, which is the output voltage of BL-SEPIC is a function of duty ratio (D) [12], which can be expressed as (1)

$$V_{dc} = \frac{D}{(1-D)} V_{in} \tag{1}$$

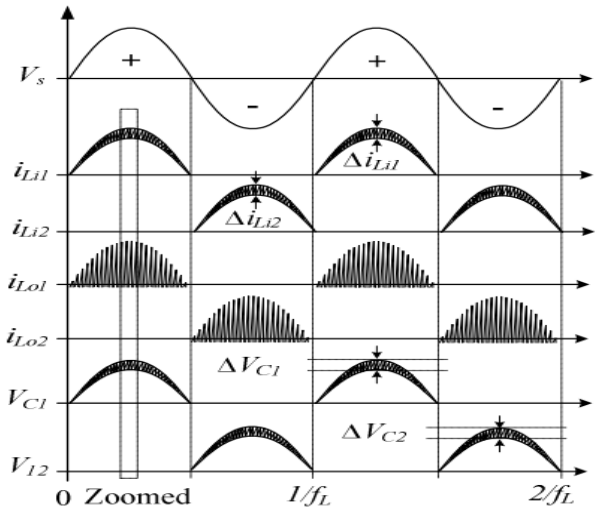
where $V_{in} = \frac{2V_m}{\pi}$, is the average voltage at the input of BL-SEPIC converter. $V_m$ is the peak value of supply voltage. The instantaneous power $P_i$ at SEPIC output for any DC bus voltage can be expressed as a linear function of $V_{dc}$ as (2)

$$P_i = \frac{P_{max}}{V_{dcmax}} V_{dc} \tag{2}$$

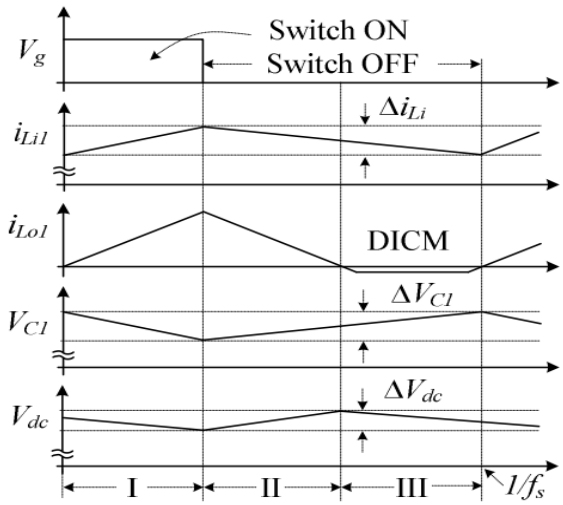
The input side inductors with a permitted ripple current of $\Delta I_{Li}$ is designed according to (3)

$$L_{i1} = L_{i2} = \frac{V_{in} D}{\Delta I_{Li} I_{in} f_s} \tag{3}$$

The design of input side inductor is done for peak value of minimum input voltage (i.e. $V_s = \sqrt{2} V_{smin}$) and rated DC




(a)




(b)

Figure 3: BL-SEPIC converter operation for an entire a)line cycle b) switching cycle

bus voltage ($V_{dc}$ = 310 V) where inductor current ripple is maximum. A current ripple as 30 % of $I_{in}$ is selected.

The output inductors is designed to ensure DICM operation even at minimum DC bus voltage. The design equation is given by (4)

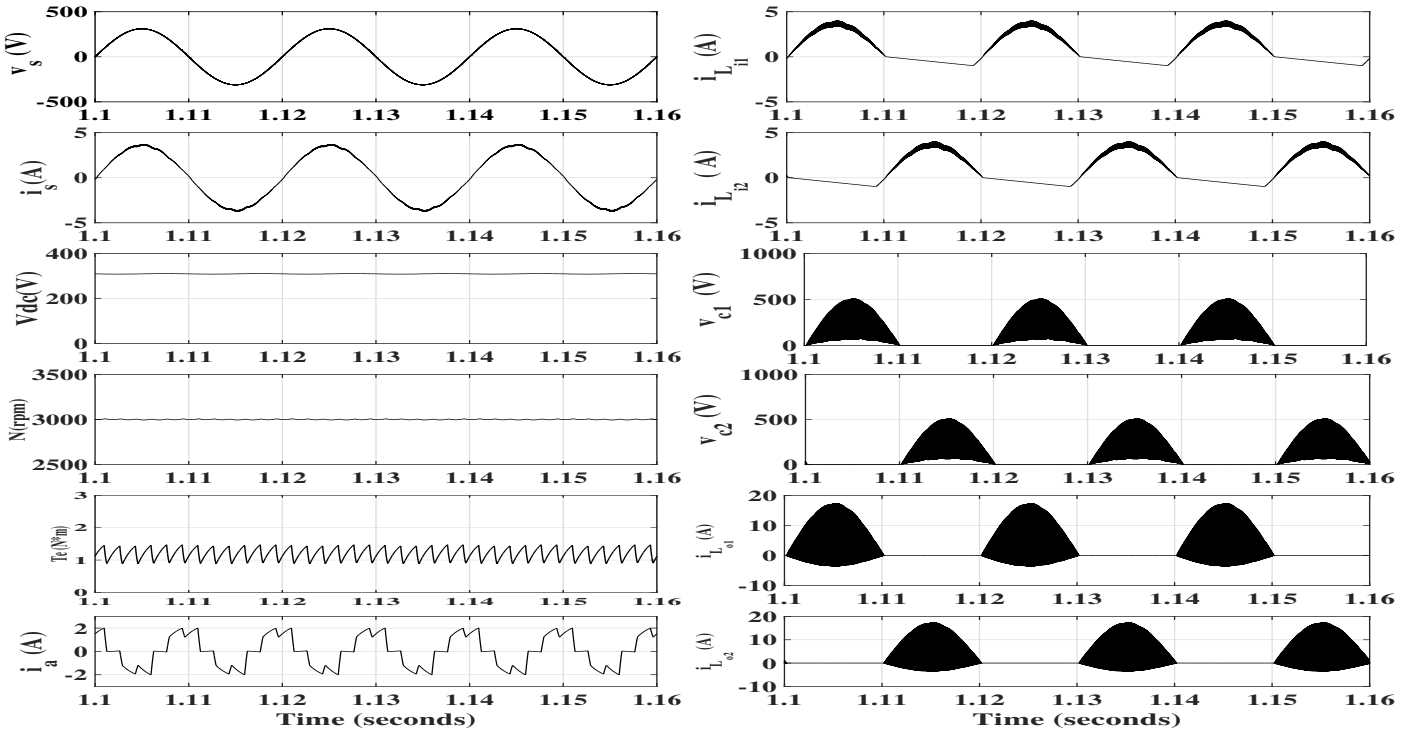
$$L_{o1} = L_{o2} = \frac{V_s^2 V_{dc} D}{2 P_i V_{in} f_s} \tag{4}$$

The energy transferring capacitor $C_{1,2}$ is designed for a permitted ripple voltage of $\Delta V_{in}$=30% at maximum DC bus voltage and maximum supply voltage as (5)

$$C_{1,2} = \frac{P_i}{\Delta V_{c1} f_s (V_{in} + V_{dc})^2} \tag{5}$$

The DC bus capacitor $C_d$ is calculated by (6)

$$C_d = \frac{P_i}{2\omega\delta V_{dc}^2} \tag{6}$$




(a) (b)

Figure 4: Steady state performance of proposed One Cycle Controlled BL-SEPIC fed BLDC motor drive

where $\delta$ is the percentage ripple of DC bus Voltage. The DC bus capacitor is calculated to ensure minimum ripple even at lower DC bus voltages.

The maximum filter capacitance required is calculated as (7)

$$C_{fmax} = \frac{I_m}{\omega V_m} \tan\theta \tag{7}$$

where $\theta$ is the angular displacement between filter output current and voltage.

The design criteria for filter inductance for a selected cut off frequency of $f_c$=$f_s$/10 such that $f_L \leq f_c \leq f_s$ is given by (8)

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} \tag{8}$$

## III. Control Of Proposed Adjustable Speed Drive

The proposed BLDC motor drive speed control is achieved by Pulse Amplitude Modulation of three phase VSI. The VSI switches are operated at fundamental frequency based on position signals from hall sensors. The DC bus voltage modulation to achieve PAM is done by One Cycle Control of BL-SEPIC converter. The actual speed is obtained from the position signals given by hall sensors. A PI controller is used to process the error between actual speed and reference speed to generate the reference DC bus voltage. This reference voltage and actual DC bus voltage is fed to One Cycle Controller to generate the required gate pulses for BL-SEPIC switches. This non linear control will offer more robustness, input-perturbation rejection and faster dynamic response.

### A. Principle of One Cycle Control technique

The concept of One cycle was introduced by Smedley and Cuk in 1991 [11]. The general concept for one cycle control is as follows:

Switching function $d(t)$ at a frequency $f_s = \frac{1}{T_s}$ determines the switch operation in each cycle.

$$d(t) = \begin{cases} 1 & 0 \leq t \leq T_{ON} \\ 0 & T_{ON} \leq t \leq T_s \end{cases} \tag{9}$$

Suppose $x(t)$ is the input at switch, then the signal transfered at the output of switch is equal to

$$\begin{aligned} y(t) =& x(t) * d(t) \\ i.e., y(t) =& \frac{1}{T_s} \int_0^{T_{ON}} x(t)dt \end{aligned} \tag{10}$$

If the duty cycle of switch is modulated such that integration of the switched waveform in each cycle is exactly equal to the integration of control reference,i.e.,

$$\int_0^{T_{ON}} x(t)dt = \int_0^{T_s} v_{ref}(t), \tag{11}$$

then the mean of switched waveform is precisely equal to the mean value of control reference in each cycle.

$$y(t) = \frac{1}{T_s} \int_0^{T_{ON}} x(t)dt = \frac{1}{T_s} \int_0^{T_s} v_{ref}(t) = V_{ref}(t) \tag{12}$$

The schematic diagram for implementation of One Cycle Control for BL-SEPIC converter is illustrated in Figure 1. The

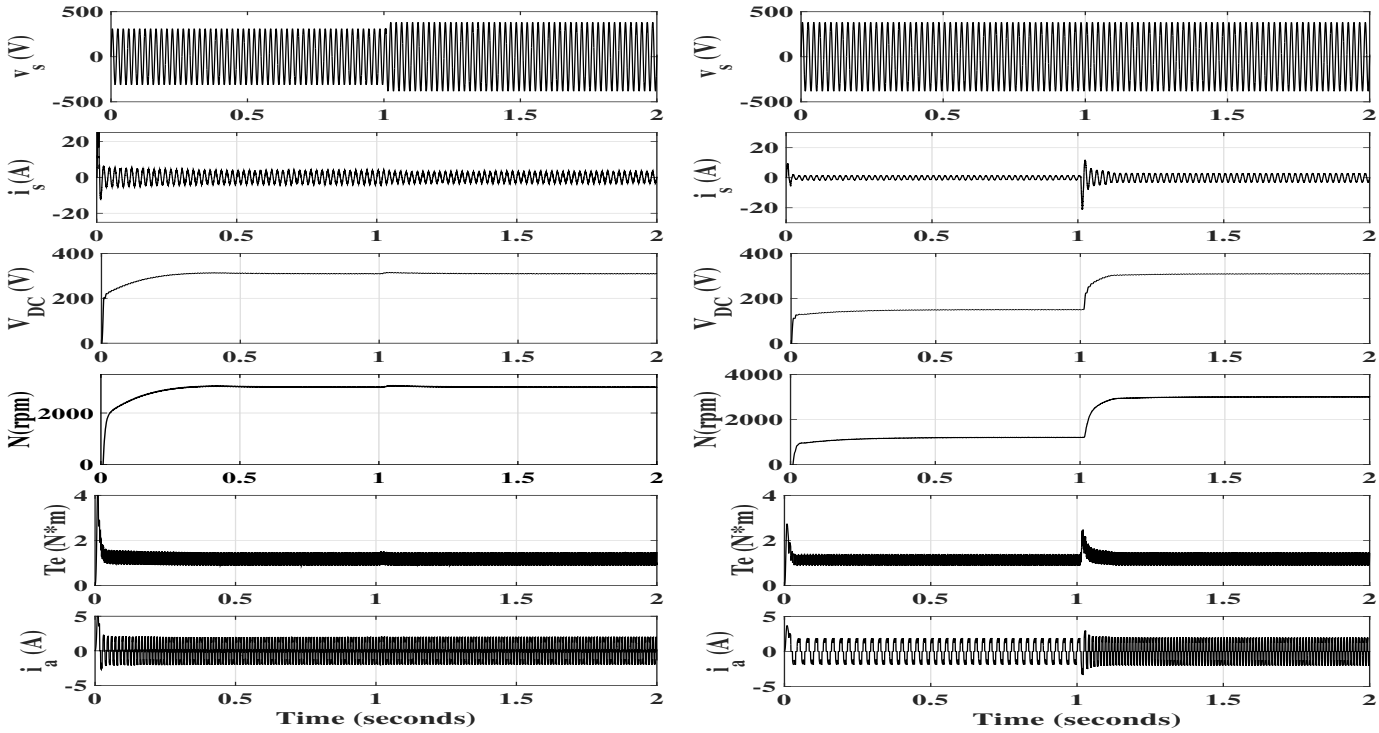



Figure 5: Dynamic Performance of proposed One Cycle Controlled BL-SEPIC converter fed BLDC motor drive under a) Step change in supply voltage b) Step change in Reference Speed

main components are a real time integrator with a reset switch, a comparator, and an S-R flipflop. A constant frequency ($f_s = \frac{1}{T_s}$) clock at the S input of flipflop determines the switch turn ON. The integrator operation is initiated instantly when the switch is turned ON. The output voltage is sensed and integrated by the integrator. A comparator compares the integrator output with the reference signal $V_{ref}$. The moment when the integrator output becomes equal to the control reference, the comparator produces a high pulse and resets the flipflop. Instantly the switch gets turned OFF and integrator resets to zero. Thus, the average of the switched waveform is assured to be equal to control reference.

$$y(t) = \frac{1}{T_s}\int_0^{dT_s} x(t)dt = V_{ref}(t) \tag{13}$$

This operation happens for every switching cycle and the output voltage is maintained to be equal to the reference signal.

## IV. Results and Discussions

The proposed BLDC drive is simulated using MATLAB/Simulink environment and performance is evaluated for steady state and dynamic conditions. The parameters such as speed (N), torque ($T_e$), DC bus voltage ($V_{dc}$), stator current ($i_a$), supply current ($i_s$), supply voltage ($v_s$), input and output inductor currents ($i_{Li1}$, $i_{Li2}$ and $i_{Lo1}$,$i_{Lo2}$) are evaluated for analysis of the proposed One Cycle Controlled BL-SEPIC fed BLDC motor drive. The power factor and Total Harmonic Distortion of input current for different speeds are tabulated.

Table I: Steady state performance of One Cycle Controlled BL-SEPIC fed BLDC motor drive at different speeds.

| Reference Speed (rpm) | Actual Speed (rpm) | Vdc* | Vdc | THD(%) | PF | Is(A) |
|---|---|---|---|---|---|---|
| 300 | 300 | 72.5 | 72.5 | 5.69 | 0.9982 | 0.6266 |
| 600 | 600 | 98.2 | 98.2 | 5.4 | 0.9991 | 0.8287 |
| 900 | 900 | 124.5 | 124.5 | 5.17 | 0.9995 | 1.0330 |
| 1200 | 1200 | 150.5 | 150.5 | 3.40 | 0.9999 | 1.2395 |
| 1500 | 1500 | 176.8 | 176.8 | 3.38 | 0.9999 | 1.4495 |
| 1800 | 1800 | 203 | 203 | 2.96 | 0.9999 | 1.6630 |
| 2100 | 2100 | 230 | 230 | 2.61 | 0.9999 | 1.879 |
| 2400 | 2400 | 257 | 257 | 2.4 | 0.9999 | 2.0986 |
| 2700 | 2700 | 283 | 283 | 2.3 | 0.9998 | 2.32 |
| 3000 | 3000 | 310 | 310 | 2.1 | 0.9997 | 2.547 |

### *A. Steady state performance of One Cycle Controlled BL-SEPIC fed BLDC motor drive*

The performance during steady state of the proposed BLDC drive is analyzed for rated load torque. The steady state waveforms of speed, torque and motor current for rated DC bus voltage and rated supply voltage is shown in Figure 4a. The corresponding currents through input and output inductors and voltages across energy transferring capacitors at steady state for rated conditions are illustrated in Figure 4b. Table I shows the simulation results obtained for speed control over a wide range. The results from table I convey that the BLDC motor drive with One Cycle Controlled BL-SEPIC converter operating in DICM has ensured inherent input current shaping

and maintained THD of input current below the limits as specified by IEC 61000-3-2.

### *B. Dynamic Performance of Proposed One Cycle Controlled BL-SEPIC fed BLDC motor Drive*

Dynamic performance analysis of proposed BLDC motor drive is done for:

1) step change in supply voltage
2) step change in speed

*1) Dynamic performance under step change in supply Voltage:* For the BLDC drive operating at rated speed and torque conditions, a step change in supply voltage from nominal 220 V to 270 V is given at 1 sec. The dynamic performance waveforms depicting this scenario are shown in Fig 5a. It is evident from the waveforms that OCC is able to reject the supply voltage perturbations.

*2) Dynamic performance under Step change in reference Speed:* The BLDC drive performance for a dynamic change in reference speed is analyzed by applying a step change in reference speed from 1200 rpm to 3000 rpm at 1 sec. Corresponding step change in DC bus voltage from 150 V to 310 V can be seen from the waveforms shown in Figure 5b. The controller is able to achieve faster dynamic response with zero percent overshoot and minimal settling time (0.1 sec).

## V. Conclusion

A One Cycle Controlled BL-SEPIC converter fed BLDC motor drive has been presented for air conditioning application. A BL-SEPIC converter operating in DICM mode ensures near unity power factor at AC mains. Speed control of BLDC motor is obtained by Pulse Amplitude Modulation of VSI. PAM method for speed control reduces the switching losses and current sensor requirements. A simple nonlinear One Cycle control technique is used to facilitate Pulse Amplitude Modulation by duty ratio control of BL-SEPIC converter switches. The performance of the proposed system during steady state and dynamic conditions is analyzed in MATLAB/Simulink environment. The results obtained show that the proposed BLDC motor drive has near unity power factor and supply current THD conforming to IEC 61000-3-2 standard. The One Cycle Control technique effectively rejects supply voltage perturbations. It also obtains a faster dynamic response for speed variations with zero percent overshoot and minimal settling time (0.1 sec).

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## Appendix

BLDC Motor Rating:

| **Parameters** | **Value** |
|---|---|
| Poles | 4 |
| $P_{rated}$ | 375 W |
| $V_{rated}$ | 310 V |
| $T_{rated}$ | 1.2 Nm |
| $N_{rated}$ | 3000 RPM |
| Stator resistance/phase, $R_s$ | 14.56Ω |
| Stator inductance/phase, $L_s$ | 25.71$mH$ |
| $K_e$ | 78 V/krpm |
| $K_t$ | 0.74 Nm/A |