# On-Chip 1.8 V Step Down DC/DC Converter with 94% Power Efficiency

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***Abstract*—We present a DC to DC Converter to step down an unregulated DC voltage source of 2.7 - 3.6 V to a regulated 1.8 V DC with peak power efficiency of 94%. The DC to DC Converter, constituted here, is designed for the load current range of 0 to 100 mA. The converter uses a variable switching frequency control method to adjust the power efficiency as well as the ripple to the optimum value as per the load conditions. This control mechanism is implemented by a delta modulator which makes the switching frequency load dependent. The simplicity of the delta modulator causes the silicon real estate as well as the power salvage. It makes the design highly power proficient enabling it to achieve the efficiency greater than the conventional PWM based DC to DC converter. The design, proposed here, procures efficiency of approximately 90% at and above 20% of the full load, and thereby maintains the flat efficiency curve almost over the entire load range.**

***Keywords*-DC to DC Converter, Delta modulator, High power efficiency**

## I. Introduction

With an ever-increasing demand for compact and portable electronics, an integrated Step down DC to DC converter is emerging out as an efficient interface between portable electronics and Li-Ion batteries. A negative feedback control loop employing a Pulse Width Modulation (PWM) technique is a conventional design methodology for the Step down DC to DC (Buck) converter[1]. It benefits the designer with low output ripple content and the fast transient response.

A block diagram of the PWM based buck converter is shown in Figure 1. The PWM feedback loop consists of a compensator, an error amplifier and a comparator. The compensated error is compared with a sawtooth waveform of constant frequency $f_s$ by the comparator. Thus in the PWM based buck converters, the loop is switched at the frequency, $f_s$, and the duty cycle is varied as per the load conditions to keep the output constant against supply and load variations.

The size of the LC filter used in such a design depends on the switching frequency and the acceptable ripple content. To make the design compact as well as to have less ripple in the output, it is necessary to have high switching frequency. One of the critical bottlenecks in using the high switching frequency is the drastic reduction in the light load power efficiency owing to the significant switching loss. To

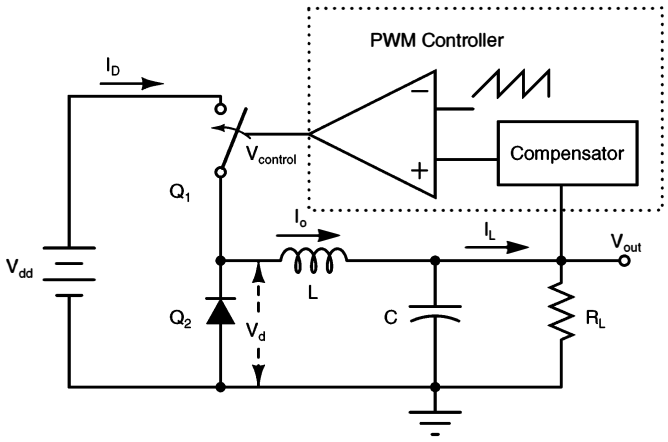


Figure 1. A block diagram of PWM based buck converter

mitigate this problem, most of the designers are introducing Pulse Frequency Modulation switching (PFM) along with PWM switching for example[2][3]. In the PFM technique, the switching frequency is adjusted, as per the load, to a lower value keeping the duty cycle constant to alleviate the switching loss. In such a system, PWM switching is used at the heavy load to limit the output ripple to a very low value while PFM is used at the light load to make the system efficient with the increased but acceptable output ripple. Integrating the PWM and PFM mode of switching as well as selecting an appropriate mode demands a load sensing logic, which makes the design quite intricate. It also results in increased silicon area and reduced power efficiency.

This paper presents a variable frequency control method which uses delta modulator in place of PWM/PFM. In this approach, the switching frequency gets automatically tuned to its optimum value as per the load conditions. At the heavy load the switching frequency is few MHz while at the light load it trickles down to few kHz. High switching frequency at the heavy load helps to keep the ripple content in the output to the low value while the reduction in the switching frequency improves the light load power efficiency. The control logic is simple to design and takes less silicon area and the power.

The rest of the paper is organized as follows. Section II describes delta modulation based buck converter in detail. Section III deals with results and observations. The conclusion is given in the last section.

## II. Delta Modulation based Buck converter

The delta modulators are typically used in data converters to achieve very high resolutions. A block diagram of a classical first order delta modulator is as shown in Figure 2[4]

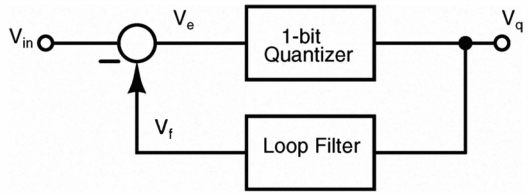


Figure 2. A block diagram of delta Modulator

The input voltage, $V_{in}$, is compared with a feedback voltage, $V_f$, by an error amplifier. The output of the error amplifier, $V_e$, is quantized using a 1-bit quantizer. The quantized signal, $V_q$, is filtered by a loop filter (typically integrator) which predicts input. The loop, therefore, tracks the input signal by making the average value of the quantized signal same as that of input. Hence the frequency as well as the duty cycle of the quantized signal gets adjusted automatically as per the input voltage. This feature is exploited in this design to step down the output from 2.7-3.6 V to 1.8 V as well as to make it independent of load and line variations.

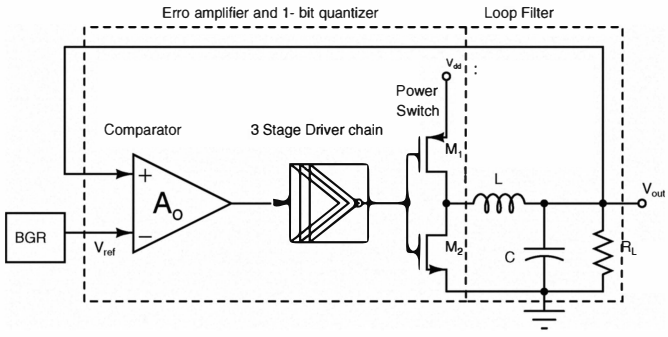


Figure 3. Schematic of a delta modulation based buck converter

A circuit diagram of a delta modulation (DM) based buck converter is shown in Figure 3. Here $M_1$ and $M_2$ form an inverter which constitute a power switch. A loop filter formed by an inductor (L) and a capacitor (C) removes switching harmonics and delivers smooth DC at the output. A feedback is taken from the output and given to a low power comparator which is acting here as an error amplifier and 1-bit quantizer. Another input of the comparator is a reference signal, $V_{ref}$, i.e desired load voltage. The loop adjusts the duty cycle of the quantized output to make its average value equal to $V_{ref}$. At the same time switching frequency also gets adjusted automatically as per the load conditions. A 3-stage driver is used to drive a huge capacitive load offered by the power switch with smaller rise and fall time.

### A. Operation

The buck converter operates in two phases. In the first phase, when $M_1$ is ON, the supply voltage, $V_{dd}$, gets connected to inductor and capacitor. During this phase of operation, the inductor stores the energy. When $M_1$ turns OFF, $M_2$ turns ON and the energy trapped in the inductor is transferred to load and capacitor. Therefore, by adjusting the duty cycle (D), the output DC can be adjusted[5]. The output will not be a pure DC signal but a small switching ripple will be overriding the DC. The amplitude of the ripple depends on the switching frequency, $f_s$, and can be given by (1)[5].

$$V_{ripple} = \frac{V_{out} \times (1-D)}{8LCf_s^2} \quad (1)$$

The Q-factor of a parallel RLC circuit, formed by LC filter and the load resistance, also play an important role in deciding the ripple content. The Q-factor can be given by (2).

$$Q = R_L \times \sqrt{\frac{L}{C}} \quad (2)$$

The Q-factor is, therefore, a direct function of the load resistance which makes the attenuation offered by the LCR circuit load dependent. Hence, with the increase in the load resistance the attenuation reduces and the ripple increases. As the load voltage is compared with the $V_{ref}$, ripple becomes a decisive factor and determines the switching frequency. In other words, the switching frequency and the output ripple are interdependent and negative feedback loop tunes itself to adjust the switching frequency and the ripple to the optimum value for a given load.

### B. Implementation Details

The design of a power switch is the most critical task as the power switch is a main source of power loss. Hence to improve the efficiency it is mandatory to keep power losses in the power switch as small as possible. The power switch is modeled in terms of *n* number of unit switches, which are connected in parallel [6]. The unit switch is designed to offer $R_{unit}$ of 6 Ω and $C_{unit}$ of 60 pF. The optimum value of *n* can be given by (3)[6].

$$n = \frac{I_L}{V_{dd}} \sqrt{\frac{R_{unit}}{f_s \times C_{unit}}} \quad (3)$$

For given specifications, under the full load condition, $n$ is found to be approximately 7. This ensures not only silicon salvage but also the maximum power efficiency.

The ripple in the output is a high frequency power line noise for loading devices. Hence it's necessary to keep it as small as possible. At the full load, the output ripple content should be few mV (typically less than 0.56% of full load value) while under no load conditions increased ripple is tolerable[2][3]. In this work the ripple under no load is limited to approximately 12% of the nominal output voltage. The cut off frequency of the LC filter is kept 1 Mrad/sec to meet these specifications. The values of L and C are chosen to limit the overshoot, under sudden load change, below 1 V.

The maximum switching frequency also depends on how fast the loop responds which in turn depends on the bandwidth of the comparator. Therefore, the comparator should have sufficiently large gain and bandwidth. The comparator, substantiated here, is a CMOS based 2-stage differential input single ended output OTA. It offers the gain of 61 dB and has bandwidth of 50 MHz while the power consumption is limited to approximately 2 mW.

The output of the converter is regulated by continuously comparing it with the reference voltage. This demands a reference voltage which is independent of supply and temperature variations. Thus a Band Gap Reference (BGR) circuit is designed to provide an accurate and stable reference. It is designed to have % variation in the reference voltage, due to the temperature as well as the supply, less than 0.1%.

## III. Results and Observation

The delta modulation (DM) based buck converter is designed using 0.18 $\mu$m CMOS Technology from UMC library. Transient response of the converter under full load is as shown in Figure 4. It has the peak to peak ripple of 8 mV (0.44%)and settling time of 50 $\mu$s while the switching frequency is automatically adjusted to 1.5 MHz.

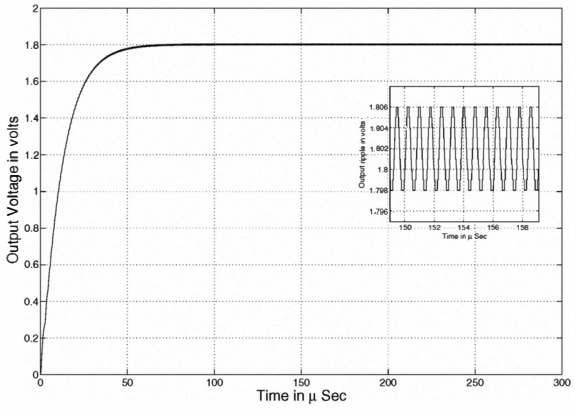


Figure 4. Transient response of the converter under the full load

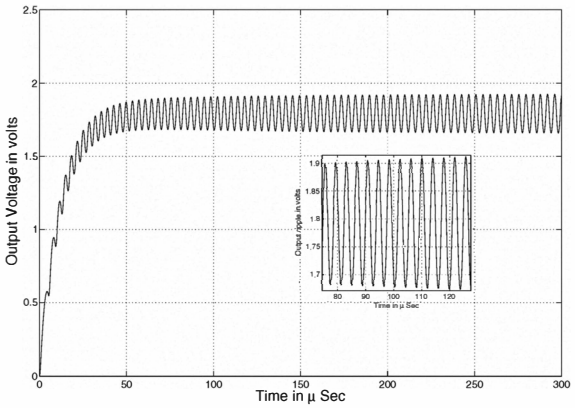


Figure 5. Transient response of the converter under no load

Transient response of the converter under no load condition is shown in Figure 5. It can be observed that the settling time remains the same as that of the full load condition but the peak to peak ripple increases to 0.2 V (12%). The switching frequency gets adjusted to approximately 200 kHz thereby improves the power efficiency.

The system was tested for sudden load change by exposing it from no load to full load value and vice versa. When foisted to no load to full load transition, the DM based buck converter incurs an undershoot of 0.8 V and takes 10 $\mu$s to return to the steady state. When the load changes suddenly from full load to no load, it exhibits an overshoot of 1 V and takes 100 $\mu$s to resume to the steady state. The waveform is shown in Figure 6

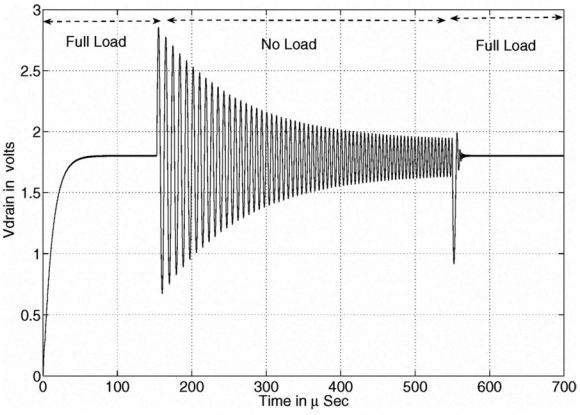


Figure 6. Transient response of the converter when load changes from full to no and vice versa

Most of the loading devices, nowadays, draw huge switching current with the nominal constant current. Thus to check the robustness of the system it has been subjected to the same scenario. The system was tested for a nominal load

of 30 mA and a switching current of 200 mA was drawn simultaneously at the rate of 5 MHz. The resulting transient response of the system is shown in Figure 7. It can be observed that the ripple content is less than 40 mV.

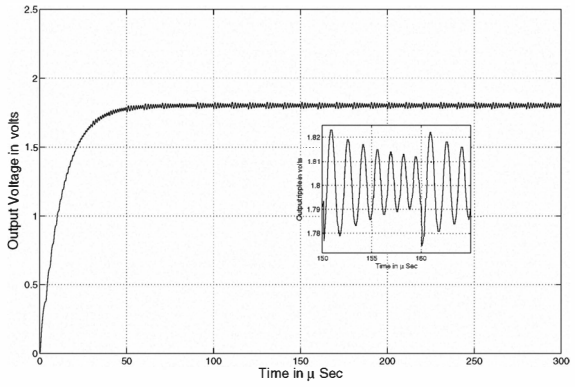


Figure 7. The transient response of the converter when subjected to the switching load

The DM based buck converter is very proficient when it comes to power efficiency. The power efficiency for the entire load range is shown in Figure 8. It has the peak power efficiency of 94% at half load while the efficiency is more than 90% at and above 20% of the full load.

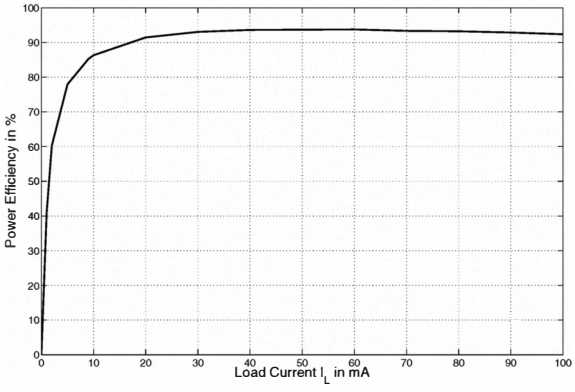


Figure 8. The power efficiency curve of the converter

The behavior of the system under varying input conditions has been analyzed. The line regulation of the system is minimum i.e 0.016% at half load and it is below 1% at and above 20% of the full load. At no load, however, it increases upto 3.356%.

## IV. Conclusion

The buck converter is designed to use delta modulation for adjusting the switching frequency dynamically as per the load. The system performance is analyzed and the effects of subsequent design issues were examined. The system endeavors the full load efficiency of 93% and manages to operate with the peak efficiency of 94% at half load. The efficiency procured by the system at 10% of the full load is almost 87%. The power efficiency curve is flat almost over the entire range of the load current. The full load ripple is 8 mV (0.44%), whereas at 10% of the full load the ripple is almost 60 mV (3.33%). The DM based buck converter uses a simple control mechanism and therefore, in toto, it is a highly power efficient approach which restricts the output ripple to the acceptable value with the significant reduction in silicon area.

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