Library Characterization: Noise and Delay Modeling

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***Abstract*—In this paper, we propose new models for noise and delay of gates, which are two significant p arameters for characterizing a cell library. Supply noise and coupling noise contribute greatly to overall noise in a circuit. With scaling down of technology, coupling noise has been very significant. Hence, it is necessary to model this noise for analysis purposes. Modeling involves characterization of significant n oise parameters such as Noise propagation characteristics and Noise Immune Characteristics. Noise Immunity curve characterized using Noise bump height only method leads to fast modeling. We propose a novel method for delay modeling using FFT spectrum of output signal. The cell delay characterization is done by extracting the relationship between delay and the width of the main lobe of FFT spectrum of the response of the system for a narrow input pulse.**

***Index Terms*-Noise propagation characteristics, Noise Immunity curve (NIC), Fast Fourier Transform (FFT).**

I. Introduction

There exists different design flows i n V LSI D esign, semi-custom flow i s o ne o f t hem. S emi-custom d esign fl ow makes use of the already designed standard cell libraries. The most optimal performance can be obtained only by a full custom design flow w herein t he d esigner g ets t o c hoose t he transistor sizes exactly as per requirement. In such a situation, the designer has to build his own library. The library has to be characterized well to aid the process of synthesis and to get a reasonable idea of the post layout performance after synthesis.

As the technology shrinks, the effect of coupling capacitance between nets becomes too dominant leading to the need of crosstalk analysis for better timing analysis of the library cells. Accurate modeling of noise parameters could reduce the problems. For accurate results, parameters like noise propagation and noise immunity are to be characterized.

The demand for timing analysis has increased because of the erroneous outputs due to noise glitches at the input side. Delay models are very essential for timing analysis. Non Linear Delay based modeling (NLDM) technique is widely used in industry standard tools [1]. NLDM is based on Look Up Table (LUT) approach. For various values of input slews and output loads, the delay is calculated by running spice simulations and storing the results in the form of LUTs. Then, interpolation is performed on the available data table in order to obtain the delay at any arbitrary input slew and output load which is not present in the table.

The objective of this work is to provide a general approach for noise characterization as well as a new approach for finding out delay from the FFT spectrum of output signal. Section 2 explains the noise modeling techniques. Proposed delay modeling method is discussed in section 3. Section 4 concludes the paper.

II. Noise Modeling

Noise is any unwanted signal (voltage or current) in a net which is expected to have an arbitrary amplitude and frequency value. Noise in CMOS can be power supply noise, substrate noise etc. But as we move to lower technologies, the issue of signal integrity keeps getting more critical due to coupling noise. Owing to this, accurate noise characterization of the library becomes essential. Noise can be in the form of ripples, bumps, random noise etc. Real coupled waveform requires parameters such as amount of coupling, ground capacitance, driver size etc. However, these parameters are less efficiently controllable for exact characterization. Hence triangular waveform as shown in Fig.1, which is approximately similar to real coupled waveform, is commonly used for analysis. Parameters to specify the characteristics of a noise bump are height (in volts) and width (in seconds) [2], [3]. Isosceles triangles are used in order to reduce inaccuracies.

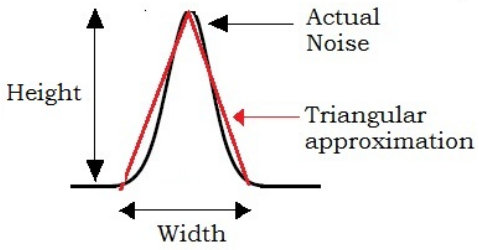

Fig. 1. Additive Input signal for noise bump characterization

The parameters to characterize noise in the library are noise propagation and Noise Immunity Curves (NIC) [2], [3], [4].

A. Noise Propagation Characteristics

Propagation characteristics of noise bump from victim net to output is very important. After propagating to the output net, the noise bump can either get attenuated or amplified.

Noise propagation information is stored in a multi dimensional table called noise propagation table. The table provides information about the characteristics of noise bump obtained. Simulation is performed for different values of input noise height and width. The height and width of the ouput noise bump obtained are saved in table. The input noise height is varied from 0 to Vdd.

Figure 2 shows noise propagation characteristic of a buffer for different values of input noise width. The height of input noise width is fixed at 1.3 V. The characterization should be performed for falling as well as rising noise. In this simulation, we have considered falling noise bump. Presence of noise bump at input leads to invalid transition at the output. As the input noise bump width varies, so does the period of false transition at the output. As width increases, output transition shifts to right side of axis and the period of false transition increases.

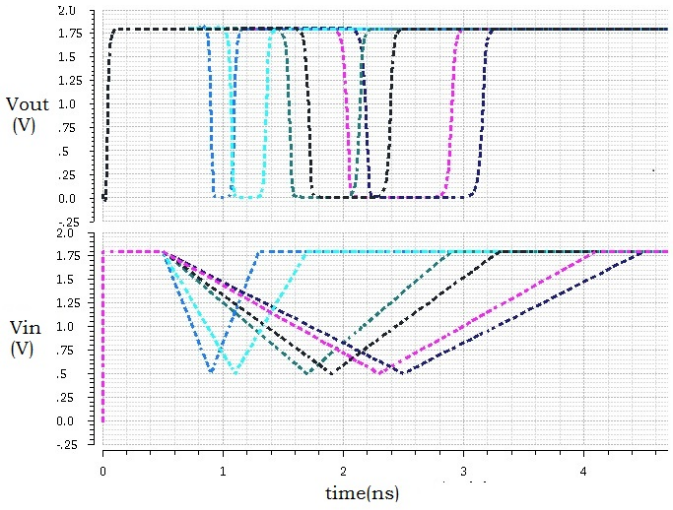

Fig. 2. Noise propagation characteristics of a buffer for different values of input noise width and constant height.

Figure 3 shows noise propagation characteristic of a buffer for different values of input noise height. Input noise width is fixed at 800 ps. Output is immune to noise till a certain height value. Despite the presence of input noise, output remains free from logic failures. However, after a certain height value, invalid transitions occur at output. As height of input noise bump increases, period of false transition increases. Noise propagation table contains the characteristics of output for varying ranges of input noise width and height.

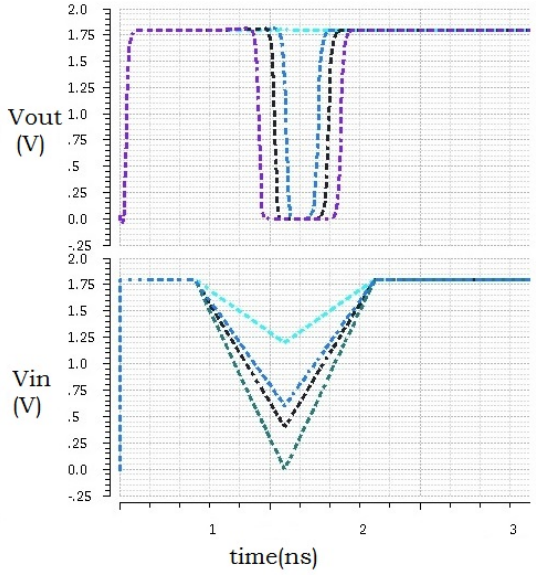

Fig. 3. Noise propagation characteristics of a buffer for different values of input noise height and constant width.

B. Noise Immunity Curve (NIC)

Each cell can tolerate a certain level of noise glitch at input without causing noise at the output. This characteristic of the cell is called noise immunity characteristic. Noise immunity characteristics are represented using Noise Immunity Curves. Noise immunity curves are plotted to find out the regions of output logic failures. There are different methods to characterize noise immunity curves. These include *Hyperbolic Noise Immunity curves*, *Noise Immunity lookup tables*, *Noise Margins* etc. In this work, we used the method of *Noise Margins* based on noise bump height.

Height based method is simple and fast. In this method, the height of output noise bump determines whether the output is a logic failure or not. Noise margin is the minimum value of output noise bump height (in Volts) which makes a logic change at output. Most of the EDA tools consider 0.2 $*V_{DD}$ as noise margin. If output noise bump height is more than 0.2 $*V_{DD}$, then it is in logic failure region. Input noise bump is varied with different values of height and width. The values of output noise bump height is observed. The pairs of input noise bump height and width causing an output bump of height more than noise margin is plotted to obtain noise immune curve.

Noise immunity of a single cell is characterized twice, once for rising noise bump and then for falling noise bump. Noise bump could change output transitions from high logic to low logic as well as from low logic to high logic. Figure 4 shows the noise immunity curve of a buffer. Area below the curve is immune to noise. Area above the curve is less tolerable to noise. For a set of noise height and width, the output logic might fail in this case.

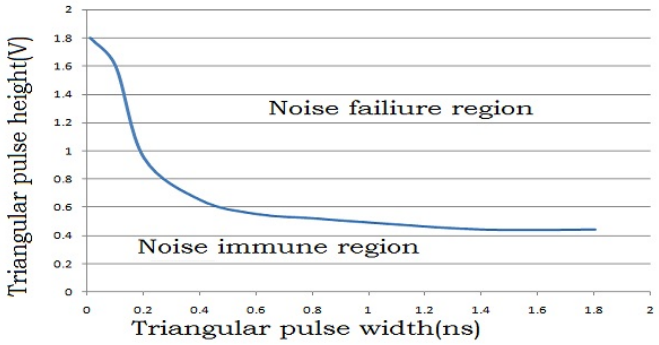

Fig. 4. Noise Immunity Curve (NIC) of a buffer

Noise slack analysis can be performed using Noise Immunity Curve. Noise slack is the amount of noise height that needs to be added to the noise bump to cause a failure [2]. When the noise slack is negative, it means that the noise bump has exceeded the noise immunity parameters for the cell and can be considered a failure. When the noise slack is positive, the noise bump is within the noise immunity parameters. After the noise characterization, EDA tools give noise report of each cell. Noise slack is an important parameter obtained from NIC. Noise slack is determined from the area of the noise bump and by checking whether the noise constraint is met. Slack area is the product of noise bump height (in Voltage) and width (in nano second). Figure 5 shows the noise slack analysis in the NIC of a buffer at points A, B and C. Point C shows a negative noise slack. Slack is said to be positive if the point is below the threshold value [2], [3].

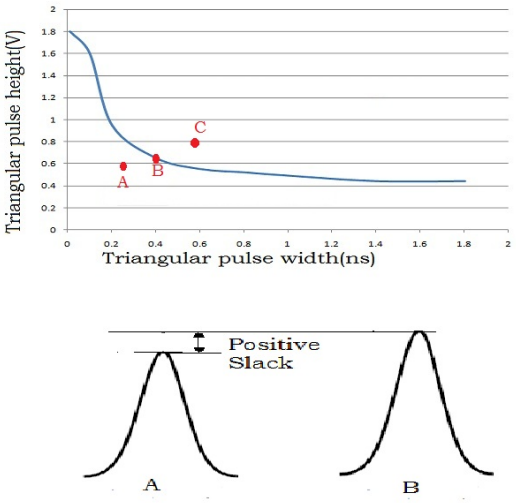

Fig. 5. Noise slack area calculation from NIC

III. Delay Modeling

EDA tools use the conventional method of Non Linear Delay Modeling (NLDM) for delay analysis. LUTs are multidimensional tables containing the delay values obtained by SPICE simulations for different pairs of input slew and output load. Tool does the interpolation on the available data in case of a new pair of input slew and output load capacitance. This method is complex and consumes more time.

The delay model proposed in this work is an approach that relates to Fast Fourier Transform (FFT) spectrum of output and delay of cell. FFT is an algorithm to calculate Discrete Fourier Transform (DFT). DFT converts a signal from time domain to frequency domain. Let $X_0, X_1, ..., X_n$ are complex numbers then DFT is calculated by the equation [5]:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-\frac{2\pi i}{N} kn}, \quad k = 0, 1, \ldots, N-1 \tag{1}$$

Evaluation using the above equation takes an algorithm complexity of O(N^2). FFT algorithms compute DFT by the same approach but with a complexity of O(NlogN), consequently saving time. The principal idea here is to determine the half width of the main lobe of the FFT spectrum of the system output for a narrow input signal pulse. The width of the input pulse is carefully chosen so that the FFT spectrum has a characteristic as shown in fig. 6. From this FFT response, the gate delay can be expressed as,

$$T_d = \frac{1}{Main\ lobe\ half\ width} \tag{2}$$

A. Experiment

Simulations are carried out at the block level to model the block delay. All the simulations are performed on gpdk 180 nm library.

1) Simulation setup: Figure 6 shows the simulation setup for delay modeling. This experiment is performed on gates such as Inverter and Buffer of different sizes. The method can be extended to any combinational block. To perform the simulation, ideally one has to apply an impulse at the input of the combinational block and find the DFT of the output signal and estimate the delay. In this work, the impulse is approximated by a rectangular pulse of very narrow width and small duty cycle. Input pulse widths of 10 ps to few nano seconds are applied at the input of the gate. A 1024-point FFT spectrum of output signal is analyzed.

2) Simulation Results: Simulation results show difference in the nature of FFT spectrum for low frequencies (starting at 0 Hz) when input pulse width is changed from a value less than the gate delay to a value more than the gate delay. Fig 7 shows typical results of simulation performed on an inverter (INV3

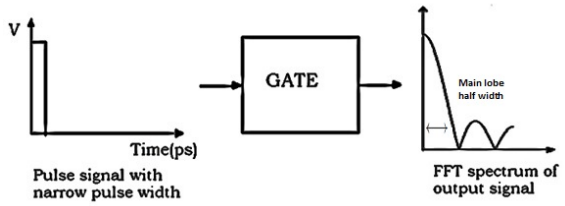

Fig. 6. The delay modeling approach

in Table 1) with 33.8 ps delay. When the input pulse width is less than the gate delay, the magnitude of the FFT spectrum increases initially, reaches a peak and then decreases. On the other hand, when the input pulse width is equal to or greater than the gate delay, the magnitude of the FFT spectrum starts decreasing right from 0 Hz. The spectrum shows similar traits for all the input pulses with pulse width greater than the delay value. This change in spectrum occurs when the input pulse width value exceeds the gate delay.

Figures 7(a-c) show the FFT spectra of the output of the inverter (INV3 in Table I) for input pulse widths of 30, 34 and 100 ps respectively. When the main lobes of the three spectra are compared, differences are visible. In figures 7(b) and 7(c), the main lobe peak occurs at 0 Hz and the main lobe amplitude decrease as the frequency is increased, while in Fig. 7(a), the magnitude of the output spectrum initially increases beyond 0 Hz, attains a peak value at about 10 GHz and then starts decreasing.

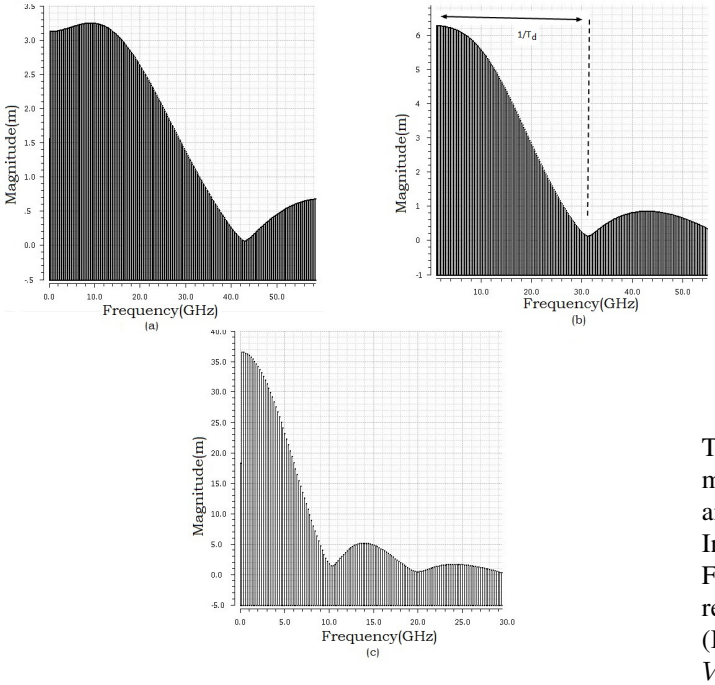

Fig. 7. FFT spectra of output of the inverter with a delay of 33.80 ps for input pulse widths of 30, 34 and 100 ps.

The change in spectrum occurs when input pulse width exceeds the gate delay and we derive the delay value from the respective spectrum. It is observed that the inverse of half the width of the main lobe of FFT spectrum is equal to the gate delay. This is found to be true for all blocks, both analog and digital.

The experiment is performed on Inverters and Buffers of different sizes. Table 1 compares the delay of gate obtained using Cadence tool and inverse of the main lobe width of FFT spectrum. Comparing the results, delay obtained using the proposed approach is found to be closer to the delay calculated by the tool. Maximum error observed is only $\pm$ 13 %.

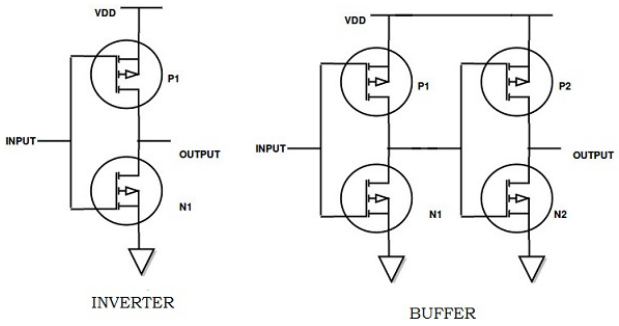

Fig. 8. Basic Inverter and Buffer circuits.

TABLE I
COMPARISON OF DELAY CALCULATED BY CADENCE TOOL AND PROPOSED APPROACH

Gate	Size of Transistors	Delay calculated by the tool (ps)	Inverse of half the width of main lobe of FFT (ps)
BUF1	$\frac{P1}{N1} = \frac{580n}{400n}, \frac{P2}{N2} = \frac{820n}{550n}$	87	95
BUF2	$\frac{P1}{N1} = \frac{1u}{400n}, \frac{P2}{N2} = \frac{1.2u}{600n}$	99.3	113
BUF3	$\frac{P1}{N1} = \frac{6.3u}{2.52u}, \frac{P2}{N2} = \frac{12u}{4u}$	113	125
INV1	$\frac{P1}{N1} = \frac{1u}{400n}$	24	22
INV2	$\frac{P1}{N1} = \frac{4.86u}{2.16u}$	34.8	33.3
INV3	$\frac{P1}{N1} = \frac{6.3u}{2.52u}$	33.6	30.7

To find the effect of supply voltage on gate delay, the experiment is repeated by changing the supply voltages of the gates and recording the output FFT spectra. Supply voltage of the Inverter is varied from 0.9 V to 1.8 V. Figure 9 shows the FFT spectrum of output for an input pulse width less than its respective gate delay. Fig. 9(a) shows the spectrum of Inverter (INV3) at V_{dd} of 0.9 V and Fig. 9(b) shows the spectrum at V_{dd} of 1.2 V. The FFT spectrum shows similar pattern in the main lobe.

Figure 10 shows the FFT spectrum of the Inverter output signal when the applied input pulse width is more than the gate delay

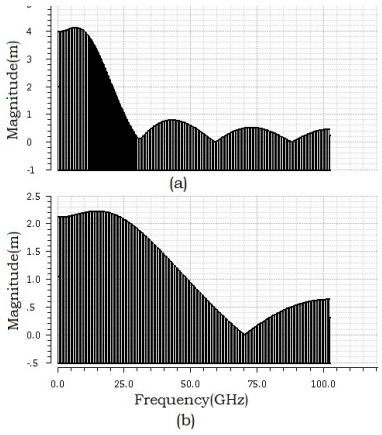

Fig. 9. FFT spectrum of output for input pulse width less than gate delay for (a) $V_{dd} = 0.9V$ (b) $V_{dd} = 1.2V$

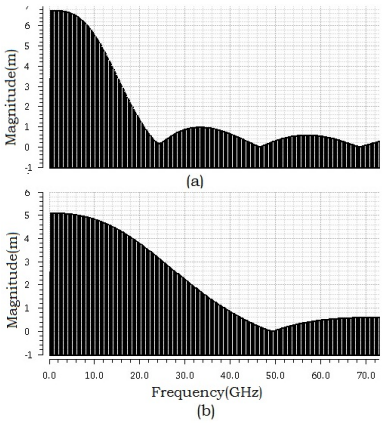

Fig. 10. FFT spectrum of output for input pulse width more than gate delay for (a) $V_{dd} = 0.9V$ (b) $V_{dd} = 1.2V$

values. Figures 10(a) and 10(b) are spectra of Inverter (INV3) at input voltage supply of 0.9 V and 1.2 V respectively. As supply voltage increases, the gate delay decreases as expected and the spectrum becomes more flat. In other words, even when the input pulse width is less than the gate delay at lower supply voltages, as the supply voltage is increased, the output spectrum begins to follow the expected trait and the gate delay can be fairly accurately determined. In general, the gate delay can therefore be determined for different supply voltages by applying input pulses of appropriate widths. The analysis can be extended to any digital gate or any combinational logic. This is significant because, the technique can be applied to determine the minimum clock period as in static timing analysis.

IV. Conclusion

In this work, library characterization is attempted by modeling noise and delay of library cells. Noise modeling requires to record noise propagation characteristics and noise immune characteristics. Noise Immunity Curve (NIC) characterization using noise bump height only method [2] reduces the simulation time considerably. The region of failure of cell can be directly observed from the NIC and hence modeling is simplified.

A new method based on FFT of the output signal for a narrow input pulse is proposed for delay modeling of the library cell. A simple relationship between the delay and the FFT spectrum of output signal is derived. Since the approach is performed using FFT algorithm, time complexity of computation is less. Delay modeling using FFT approach gives near accurate results in a short time.

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