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# A 500 kS/s 8-bit Charge Recycle Based 2-bit per Step SAR-ADC

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***Abstract*—This paper presents a low power 3.3 V, 500 kS/s 8-bit successive approximation register ADC in 0.18 $\mu$m technology. The DAC architecture employs charge recycling to produce 2-bits in one cycle i.e, it takes N/2 clock cycles to generate N-bits. The DAC architecture uses four rail to rail unity gain buffers and seven unit size capacitors in which one is half of the unit size to design ADC. Three comparators have been used to decide the 2-bits in each cycle. The simulated SNDR, at the input frequency of 56.64 kHz, is 48.14 dB and at 232.42 kHz is 47.03 dB. The simulated maximum INL as well as DNL is 0.5 LSB. The design consumes a low power of 1.8 mW from the power supply of 3.3 V.**

***Keywords*-SAR ADC, Unity Gain Buffer, Latch based comparator, Low power, Charge Recycling, 2-bit per step .**

## I. INTRODUCTION

Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC) are essential building blocks of many portable systems. These analog interfacing circuits provide connection between the physical world and the digital computing signal processing systems. In order to bring the interface between analog and digital world as close as possible there is great demand for low power ADCs.

Among different ADC architectures the SAR-ADC represents a common solution for applications demanding medium speed, medium resolution and low power. The conventional SAR-ADCs, as shown in Fig. 1, use charge redistribution DAC [1]-[2]. Speed of conversion is limited as it requires N-clock cycles to convert N-bits. The bulky binary weighted capacitor arrays employed in above architectures require large silicon area.

Recently presented ADC in [3] is a charge recycle based 1-bit per step SAR-ADC. This architecture is area efficient compared to other previous DAC architectures because it uses two buffers and four unit sized capacitors to generate 1-bit per cycle. In this architecture, speed is limited by the slew rate and the output impedance of unity gain buffer.

The ADC presented in [4] uses split capacitor and dual sampling technique to evaluate 2-bit per step. Due to split capacitor arrays and complex control logic, this architecture may demand for advanced process technology.

The ADC presented in [5] uses 2-bit per step approach. The architecture uses kelvin divider and the segmented voltage again subdivided through kelvin divider. This circuit uses large number of resistors and the controlling switches, which leads to large power and area overhead.

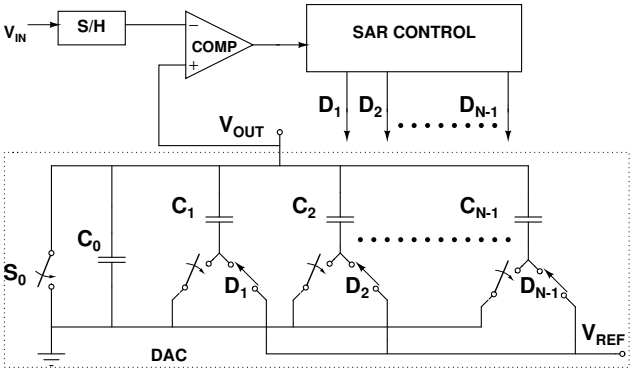


Fig. 1. Conventional SAR ADC

In this paper a multiple value approach to the DAC architecture is presented which takes N/2 clock cycles to convert N-bits. This architecture uses four buffers and seven unit sized capacitors in which one is half of the unit size. Every clock cycle 2 bits are to be generated. This requires three reference voltages to be generated for comparison from DAC. Out of seven unit sized capacitors, four capacitors are used to generate one reference voltage and remaining three capacitors are used to generate other two reference voltages. In one clock cycle only two buffers are in use to generate the 2 bits and the other two buffers are turned off, thus saving the power.

The remaining paper is organized as follows. Section II presents the DAC architecture, section III presents the buffer and the comparator architecture, section IV presents the sample and hold circuit, section V gives the simulation results and section VI conclusion.

## II. DAC ARCHITECTURE

The proposed DAC architecture schematic is as shown in Fig. 2(a). This architecture has been derived on the basis of the DAC architecture proposed in [3].

DAC architecture uses four buffers and seven capacitors. The capacitors are chosen such that $C_{TOP1}$ = $C_{TOP2}$ = $C_{BOT1}$ = $C_{BOT2}$ = $C_{TH1}$ = $C_{TH2}$ = C and $C_{TH3}$ = C/2. $V_{REF1}$ and $V_{REF2}$ are taken as $V_{REF}$ and zero respectively.

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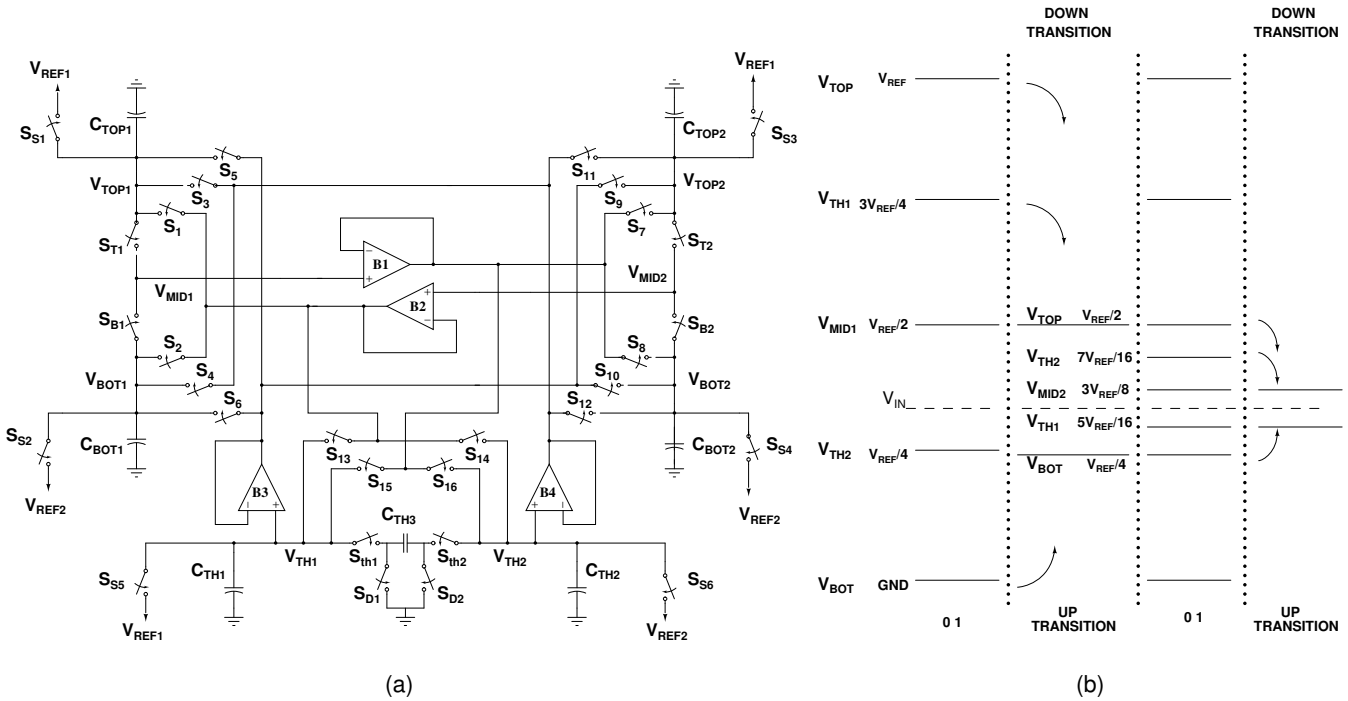


Fig. 2. Proposed DAC (a) Schematic (b) Algorithm

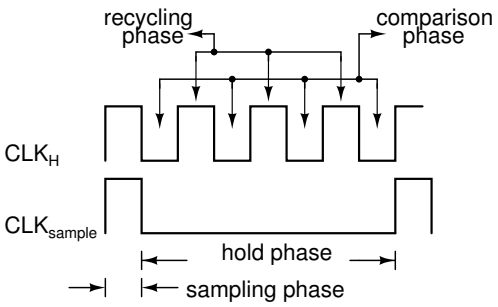


Fig. 3. Timing diagram showing sampling phase, comparison cycle and recycling phase

The Algorithm used for the DAC operation is shown in Fig. 2(b). The DAC is operated as follows : In the sampling phase, the switches $S_{S1}$-$S_{S6}$, $S_{D1}$ and $S_{D2}$ are closed. The capacitors $C_{TOP1}$, $C_{TOP2}$ and $C_{TH1}$ will get charged to $V_{REF1}$ while the bottom capacitors $C_{BOT1}$, $C_{BOT2}$ and $C_{TH2}$ will get charged to $V_{REF2}$. At this time all other switches will be open and the voltage across $C_{TH3}$ will be zero. Fig. 3 shows the timing diagram for the DAC operation where $CLK_{sample}$ is the clock applied to the sample and hold circuit, $CLK_H$ is the clock applied to the DAC.

The comparison cycle follows the sampling phase. In this phase switches $S_{S1}$-$S_{S6}$, $S_{D1}$ and $S_{D2}$ are open and the switches $S_{T1}$, $S_{B1}$, $S_{th1}$ and $S_{th2}$ are closed. The capacitors $C_{TOP1}$ and $C_{BOT1}$ generate voltage $V_{MID1}$, i.e, $V_{MID1}$ = ($V_{TOP1}$+$V_{BOT1}$)/2 = $V_{REF}$/2. The capacitors $C_{TOP2}$ and $C_{BOT2}$ retain the previous voltage levels i.e, $V_{TOP2}$ = $V_{REF}$ and $V_{BOT2}$ = 0. The capacitors $C_{TH1}$, $C_{TH2}$ and $C_{TH3}$ together will generate the voltages $V_{TH1}$ and $V_{TH2}$. This is explained as follows: In the sampling phase, the switches $S_{th1}$, $S_{th2}$ are open and $S_{D1}$, $S_{D2}$ are closed. The node A is charged to $V_{REF}$ and node B is connected to zero so that the voltage across $C_{TH1}$ is $V_{REF}$ and voltage across $C_{TH2}$, $C_{TH3}$ is zero as shown in the Fig. 4. The charge on $C_{TH1}$ is $C_{TH1} \times V_{REF}$ which is $C \times V_{REF}$. The equivalent circuit during comparison

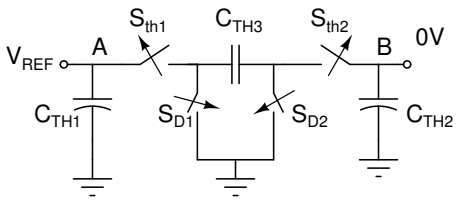


Fig. 4. Threshold voltage generation circuit in sampling and recycling phase

phase is as shown in Fig. 5. In the first comparison cycle the switches $S_{th1}$, $S_{th2}$ are closed. The charge on $C_{TH1}$ and $C_{TH2}$ will now get redistributed. Therefore according to the charge conservation principle,

$$CV_{REF} = CV_{TH1} + \frac{CV_{TH1}}{3}$$

$$V_{TH1} = \frac{3V_{REF}}{4} \tag{1}$$

$$V_{TH2} = \frac{\frac{C}{2} \times V_{TH1}}{C + \frac{C}{2}}$$

$$V_{TH2} = \frac{V_{REF}}{4} \tag{2}$$

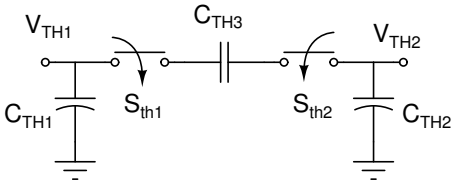


Fig. 5. Threshold voltage generation circuit in comparison phase

These three node voltages i.e, $V_{MID1}$, $V_{TH1}$ and $V_{TH2}$ are now compared with $V_{IN}$ simultaneously. The result of the comparison is fed to one hot code generator and then to encoder. According to the $V_{IN}$'s value as shown in Fig. 2(b) the bits generated is 01. Since the $V_{IN}$ lies in between $V_{REF}$/2 and $V_{REF}$/4 the bits produced will trigger the logic circuit to close the switches $S_{T1}$, $S_4$ $S_7$, $S_{12}$ and $S_{15}$. In effect the voltages $V_{TOP2}$ and $V_{TH1}$ will recycle to $V_{REF}$/2 during recycling phase and is called a down transition. The nodes $V_{BOT1}$ and $V_{BOT2}$ will recycle to $V_{REF}$/4 and is called as up transition. Now new voltages are such that $V_{TOP1}$ = $V_{TOP2}$ = $V_{TH1}$ = $V_{REF}$/2 and $V_{BOT1}$ = $V_{BOT2}$ = $V_{TH2}$ = $V_{REF}$/4. The capacitor $C_{TH3}$ will be discharged to ground. For the next two bit generation in the next comparison phase, only the switches $S_{T2}$, $S_{B2}$, $S_{th1}$ and $S_{th2}$ have to be closed so that the capacitors $C_{TOP2}$ and $C_{BOT2}$ will produce the voltage $V_{MID2}$ = ($V_{TOP2}$ + $V_{BOT2}$)/2 = 3$V_{REF}$/8. The bottom capacitors $C_{TH1}$, $C_{TH2}$ and $C_{TH3}$ altogether produce 7$V_{REF}$/16 and 5$V_{REF}$/16 as reference voltages at the nodes $V_{TH1}$ and $V_{TH2}$ respectively. Nodes $V_{TOP1}$ and $V_{BOT1}$ will hold previous voltage levels $V_{REF}$/2 and $V_{REF}$/4 respectively. Now the switches $S_{th1}$ and $S_{th2}$ are open and the switches $S_{D1}$ and $S_{D2}$ closed so as to discharge the capacitor $C_{TH3}$ to ground.

Again in the next comparison cycle $V_{IN}$ is compared with $V_{MID2}$, $V_{TH1}$, $V_{TH2}$ and with the presence of $V_{IN}$ in between 3$V_{REF}$/8 and 5$V_{REF}$/16, the bits generated will be 01. Next recycling period the switches $S_{T2}$, $S_1$, $S_6$, $S_{10}$ and $S_{14}$ are closed. The nodes $V_{TOP1}$ and $V_{TH2}$ will recycle to 3$V_{REF}$/8, a down transition and the nodes $V_{BOT1}$ and $V_{BOT2}$ will recycle to 5$V_{REF}$/16, an up transition.

In this algorithm in each charge recycling period only two buffers out of four buffers is turned on to charge the capacitors.

## III. Comparator And Buffer

### A. Buffer architecture

The buffer schematic is shown in Fig. 6 [6]. The buffer output impedance and the slew rate determines the speed of the above DAC. Here a buffer architecture with high slew rate is presented. The circuit consists of two complementary differential stages with transistors $M_1$-$M_5$ and $M_{10}$-$M_{14}$ are connected in parallel. In which each of them drive one half of the output common source push pull stage. The transistors $M_6$-$M_9$ generate bias. In the proposed DAC architecture, only two buffers are turned on in recycling phase. Switches $S_1$, $S_2$, $S_3$ and $S_4$ are provided in buffer (Fig. 6) to turn on/off the required buffer.

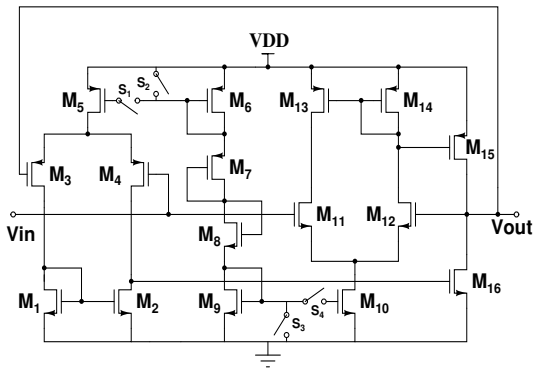


Fig. 6. Schematic of buffer

### B. Comparator

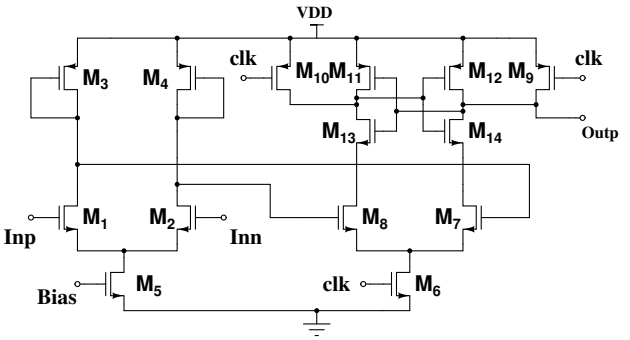


Fig. 7. Schematic of comparator

Schematic of the comparator used in this work is shown in Fig. 7. It is a dynamic latch based comparator as in [7]. The dynamic latch consists of pre-charge transistors $M_9$ and $M_{10}$, cross-coupled inverter $M_{11}$-$M_{14}$, differential pair $M_7$, $M_8$ and switch $M_6$ which prevent the static current flow when the clk is low. When the clk signal is low, the drain voltages of $M_7$

and $M_8$ are $V_{DD}$-$V_T$ and their source voltage is $V_T$ below the latch input common mode voltage. Therefore, once the clk signal goes high, the n-channel transistors $M_7$, $M_8$, $M_{13}$ and $M_{14}$ immediately go into the active region. Because one of the transistors from each cross coupled inverters is off in steady state, there is no static power dissipation. The bias voltage generated for buffer is also used to bias the comparator.

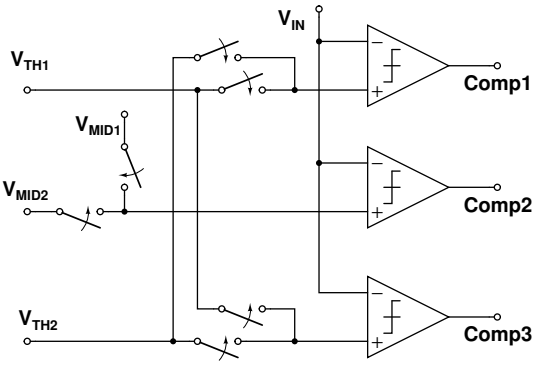


Fig. 8. Switch configuration at input of comparators

Three comparators followed by one hot code generator and encoder are used for two bit generation. $V_{TOP1}$ and $V_{TOP2}$ will always hold voltages higher than $V_{BOT1}$ and $V_{BOT2}$. But $V_{TH1}$, $V_{TH2}$ may hold values above and below $V_{MID1}$ / $V_{MID2}$. Therefore input to the comparator Comp1 and Comp3 are connected to both $V_{TH1}$ and $V_{TH2}$ through switches as shown in Fig. 8. The control logic will take care of the switching, based on the value of $V_{IN}$, $V_{TH1}$ and $V_{TH2}$. The $V_{MID1}$ and $V_{MID2}$ are connected to the input of Comp2.

## IV. Sample and Hold Architecture

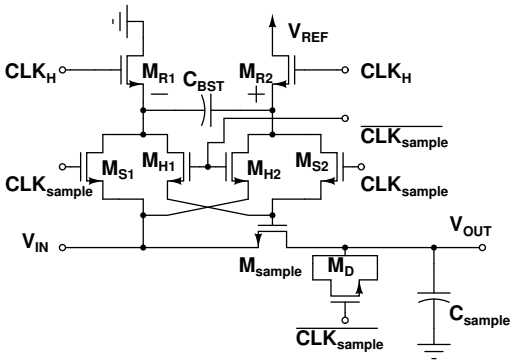


Fig. 9. Sample and Hold circuit

A switched-capacitor clock-boosted architecture is used for the sample-and-hold circuit due to its rail-to-rail capability and low-power operation. Schematic is as shown in Fig. 9 [3]. After a few clock periods, $C_{BST}$ is charged to $V_{DD}$ and subsequently acts as a floating voltage source. At each sampling phase ($CLK_{sample}$), $C_{BST}$ connects the gate-source terminals of $M_{sample}$ in such a way that $V_{GS}$ = $V_{DD}$. Therefore in sampling phase, the gate source voltage of $M_{sample}$ will be held at $V_{DD}$ higher than its source voltage regardless of the value of $V_{IN}$ making the switch resistance input independent. On the other hand, in the hold phase, $M_{H1}$ and $M_{H2}$ turn on and $M_{S1}$ and $M_{S2}$ turn off, providing a negative voltage between the gate-source terminals of $M_{sample}$. This results in $V_{GS}$ = -$V_{DD}$ during hold phase to avoid leakage problem. $M_D$ is employed to cancel the charge-injection effect. The voltage on $C_{BST}$ may degrade due to leakage, so a high frequency clock $CLK_H$ (same as applied in DAC) is applied through transistors $M_{R1}$ and $M_{R2}$ to refresh it to $V_{DD}$.

## V. Simulation Results

The proposed ADC is an 8-bit 500 kS/s SAR-ADC and is implemented in 0.18$\mu$m technology. The DAC capacitor used is 2 pF and the sampling capacitor is 500 fF.

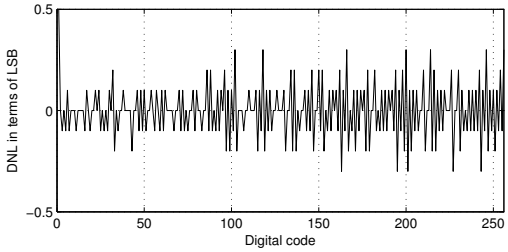


Fig. 10. DNL plot of the ADC

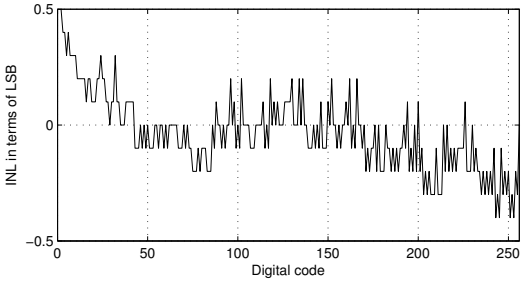


Fig. 11. INL plot of the ADC

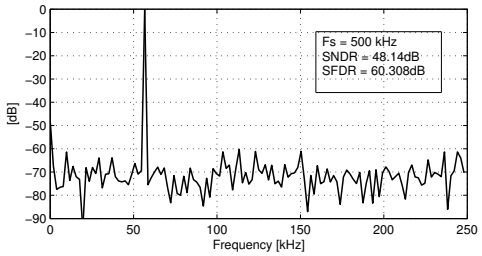


Fig. 12. Output spectrum at input frequency 56.64 kHz

As shown in Fig. 10 and Fig. 11, at 500 kS/s, the simulated DNL and INL are within 0.5 LSB. The spectra for an input full scale sine wave at 56.64 kHz and 232.42 kHz are as shown in Fig. 12 and Fig. 13 respectively for which the SNDR of

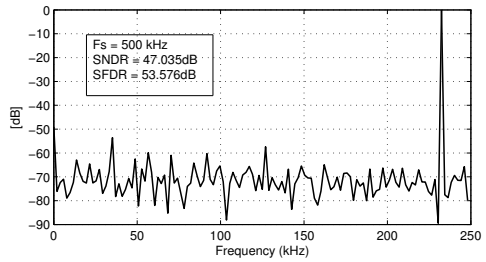


Fig. 13. Output spectrum at input frequency 232.42 kHz

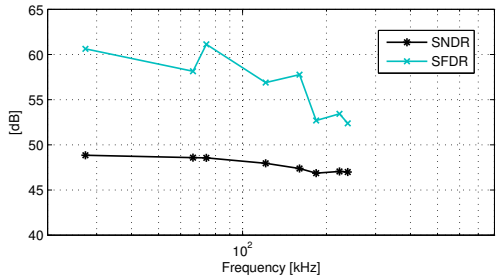


Fig. 14. Variations in SNDR and SFDR with respect to frequency

48.14 dB (ENOB = 7.7) and 47.03 dB (ENOB = 7.52) are obtained, respectively. The variation of the SNDR and SFDR with respect to frequency is shown in Fig. 14. The total power consumption for 56.64 kHz and 232.42 kHz input sine wave are simulated to be 1.8 mW and 2.02 mW respectively.

## VI. Conclusion

A low power 8-bit SAR-ADC is implemented in 0.18 $\mu$m technology. The designed ADC consumes 1.8 mW power from 3.3 V supply for low frequencies. The power increased to 2 mW at Nyquist frequency. Charge recycle based 2-bit per step conversion is employed to achieve 500 kS/s conversion speed. The porting of the design to 90 nm or 65 nm technology and lower supply voltage could bring in a great deal of performance improvement and minimize power and area. The ENOB of 7.52 was obtained when operated at Nyquist rate.

TABLE I
Performance summary of the ADC

| Parameter | Value |
|---|---|
| Technology | 0.18 $\mu$m |
| Supply Voltage | 3.3 V |
| Resolution | 8 bit |
| Sampling Frequency | 500 kS/s |
| SNDR | 47.03 dB @ 232.42 kHz, 48.14 dB @ 56.64 kHz |
| ENOB | 7.52 @ 232.42 kHz, 7.7 @ 56.64 kHz |
| Maximum DNL, INL | 0.5 LSB, 0.5 LSB |
| Total Power | 1.8 mW |

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