INVESTIGATION AND DESIGN OF CAPACITOR-BASED MULTILEVEL INVERTERS

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled "Investigation and Design of Capacitor-based Multilevel Inverters" which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me.* The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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Date:

CERTIFICATE

This is to *certify* that the Research Thesis entitled "Investigation and Design of Capacitor-based Multilevel Inverters" submitted by Banavath Shiva Naik (Register Number: 177093) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

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Abstract

As a result of enormous research and development in multilevel inverters (MLIs), their presence in industries over a wide-ranging application is noticeable. With the advent of high-power semiconductors in the last two decades, conventional voltage source inverters (VSIs) are replaced by MLIs. Output voltage boosting property along with curtailment in the circuit voltage stress and component count are considered as the essential topological features for the new MLI circuits. At present, electric vehicles and renewable power generation are subjects of high interest. In such applications, a secondary circuit such as front- or back-end boosting stage is incorporated into the converter to meet the requirements. In such cases, using MLIs with boosting ability is more logical and reduces the intermediate boosting stage or even eliminates them. Furthermore, most of the available high-power rotating machines require variable speeds and special control algorithms. A power conversion stage using semiconductor switches is required in these renewable energy systems and industrial applications. Therefore, a deep understanding of the design of high-power converters is required for researchers and industrial engineers.

Ever since the inception of MLIs, cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) converters are among the earliest topologies deemed to be well-established. Though these converter circuits have their remarkable peculiarities, they suffer from a control complexity, higher components. The Diode-clamped inverters require more power diodes. Also, the capacitor voltage balancing in diode-, capacitor-clamped MLIs is a severe problem that requires sophisticated modulation techniques and external balance circuitry. Since then, many derivatives and refinements to these classic topologies have been proposed. In recent years, the evolution of MLIs is tending to reduce the number of components, especially dc sources based on the combination of capacitors. In these topologies, dc sources are replaced with switched capacitors (SCs) to reduce the number of dc sources and the cost of the converter. SCs are used as alternative DC supply to boost the output voltage. Due to the self-voltage balancing property of SCs, an uncomplicated sensor-less

control scheme can be employed. SC-based converters are the basic alternative solution that does not need any transformer to boost the voltage. This research work's motivation stems from the demand to generate substantial voltage levels while keeping the circuit reliability as high as possible. Therefore, three different topologies with voltage boosting property are proposed in this thesis by taking advantage of the switched-capacitor multilevel inverter (SC-MLI) configurations. The offered solutions exhibit considerable topological improvements with reduced and control complexity.

This thesis mainly deals with the design and development of multilevel converter topologies with the reduced number of power devices and real-time implementation of the converters. Firstly, a modified T-type multilevel inverter (MT-MLI) with a reduced part count is proposed. Besides, a sensor-based voltage balancing control to regulate the FC voltage is elaborated. Methods to extend the topology for higher voltage levels are studied. Detailed simulation and experimental studies are carried out to validate the proof of controllability of the proposed topologies and their associated control system.

Secondly, a novel SC-based hexad boost 13-level topology with only three capacitors, 14 semiconductor switches, and one diode is introduced. The series-parallel technique is utilized effectively to balance the capacitor voltages. The circuit operation, modulation scheme, and extension for higher voltage levels are discussed. Capacitors' voltage ripple loss and curve-fitting approaches to calculating the semiconductor losses are analyzed in detail. Results validating the performance of the proposed topology and control schemes are presented.

Lastly, two hybrid MLI configurations are proposed: Boost hybrid multilevel inverter (BH-MLI), Hybrid nine-level inverter topology (HNIT) with voltage boosting ability, and less component count. Simple structure, and easy control are the additional benefits of the proposed arrangements. A simple logic gate based (LGB) switching controller is developed for the presented circuits. Extensions of BH-MLI for higher levels are presented. Further, the performance of the proposed circuits is validated experimen-

tally with PD-PWM and round control methods at different modulation indices, load conditions.

All the developed circuits are simulated in MATLAB/Simulink for stand-alone operations. All the topologies are tested experimentally in the laboratory at scaled-down ratings. Further, quantitative and generic cost comparisons are conducted among the state-of-art capacitor-based MLIs to highlight the superiority of the proposed configurations.

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List of Abbreviations

AC	Alternating current
ANPC	Active neutral-point-clamped
BH-MLI	Boost hybrid multilevel inverter
CHB	Cascaded H-bridge
DC	Direct current
ETO	emitter turn-off thyristor
FFT	Fast fourier transform
FC	Flying capacitor
FCB	Flying capacitor bridge
GCT	Gate commutated thyristor
GTO	Gate turn-off thyristor
HNIT	Hybrid nine-level inverter topology
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
LGB	Logic gate based
LV	Low-voltage
MCT	MOS-controlled thyristor
MLI	Multilevel inverter
MT-MLI	Modified T-type multilevel inverter
MV	Medium-voltage
NPC	Neutral point clamped
PD	Phase disposition
PF	Power factor
PIV	Peak inverse voltage
PV	Photo voltaic
PWM	Pulse width modulation
RMS	Root mean square
SC	Switched-capacitor
SCCs	Switched-capacitor cells
SC-MLIs	Switched-capacitor multilevel inverters
SGCT	Symmetrical gate-commutated thyristor
SIT	static induction thyristor

SSHB	Single stage hexad boost
TBV	Total blocking voltage
THD	Total harmonic distortion
VBF	Voltage boosting factor
VSIs	Voltage source inverters

List of Symbols

V_{dc}	DC-link voltage
m_a	Amplitude modulation index
f_{sw}	Switching frequency
S_n	n^{th} switch
C_n	n^{th} capacitor
C_f	Flying capacitor
C_B	Boost capacitor
C_{LD}	Level doubling capacitor
N_l	Number of levels
N_{sw}	Number of switches
N_{diode}	Number of diodes
N_{cap}	number of capacitors
N_{dc}	Number of DC sources
V_o	Output voltage
V_{ab}	Voltage between a-b terminals
V_d	Diode forward voltage drop
i_o	Output current
V_{ref}	Reference wave
V_m	Peak magnitude of reference wave
i_{sx}	Source current of phase-x
α_n	n^{th} transition angle
r_s	Internal resistance of switch
r_d	Internal resistance of diode
r_c	Equivalent series resistance of capacitor
R	Load resistance
ΔQ_{C_n}	Charge of n^{th} capacitor
v_{FC}	FC voltage
Z	Load impedance
V_{CE}	Collector-emitter voltage
i_C	Collector current
$^{\circ}C$	Degree Celsius

T_{min}	minimum temperature (25℃)
T_{max}	and maximum temperature (125℃)
$P_{igbt}(i_c, T°C)$	IGBT conduction loss at T℃
$P_D(i_f, T°C)$	Diode conduction loss at T℃
V_f	Forward voltage drop of the diode
i_f	Forward current of the diode
$K_{IGBT}(i_C)$	IGBT switching loss factor
$K_D(i_f)$	Diode switching loss factor
f_{ref}	Fundamental reference frequency
$P_{C_{rpl}}$	Ripple loss of Capacitor

Chapter 1

INTRODUCTION

This chapter introduces the thesis, including an overview, features, topological aspects, and common issues encountered in the application of MLIs. Following the discussion on the advantages and challenges of the current MLIs, a critical review of emerging MLI topologies is presented. In the end, the research objectives and organization of the thesis are included.

1.1 Overview of high power converters

The evolution of medium-voltage (MV) and high-power converter drives started in the mid of 1980 when 4500 V gate turn-off (GTO) thyristors are commercially available. Conventional two-level voltage source inverters are widely replaced by MLIs. MLIs became popular with the advent of high-power semiconductors in the last two decades. In the past, several high-power converters are developed and commercialized in standard and customized products that power a wide range of industrial applications (Rodriguez et al., 2002), (Rizzo and Zargari, 2004). The power rating of the MV drives at the medium voltage level of 2.3 - 13.8 kV ranging from 0.4 to 40 MW. This power rating can be increased to 100 MW, where synchronous motor drives are often used with load-commutated inverters. Nonetheless, most installed MV drives fall in the 1 - 4 MW range with 3.3 to 6.6 kV voltage ratings. A study on the market has shown that around 85% of MV drives are employed for fans, pumps, conveyors, and compressors. The technical requirements for these drives are comparatively simple and can be achieved by standard MV drives (Wu and Narimani, 2017).

The voltage and current ratings of the semiconductors which are available com-

Table 1.1: Market overview of semiconductors

Rating	Power diode	Thyristor	GTO	GCT/IGCT/ SGCT	IGBT
Maximum voltage	8.5 kV at 1.2 kA	12 kV at 1.5 kA	6 kV at 6 kA	10 kV at 1.7 kA	6.5 kV at 0.75 kA
Maximum current	9.6 kA at 1.8 kV	5 kA at 0.4 kV	6 kA at 6 kV	5 kA at 4.5 kV	2.4 kA at 1.7 kV

mercially in the market are shown in Table 1.1. There are some other semiconductor devices, including power MOSFET, static induction thyristor (SIT), emitter turn-off thyristor (ETO), and MOS-controlled thyristor (MCT). Nevertheless, they have not achieved considerable importance in high-power applications. These semiconductor switches are available in the MV range and can not withstand the higher operating voltages individually. On the other hand, MV semiconductors can be connected in series to enhance the operating voltage of power converters. The semiconductors in series connection and their gate drivers may not show similar static/dynamic performance. These series-connected devices may not share the inverse voltage equally during the blocking modes and transients. A separate equalization circuit is required to obtain equal voltage sharing during blocking modes. However, power losses are introduced to the converter because of the additional voltage equalization circuit (Rodriguez et al., 2009b).

1.2 Multilevel inverters

With the advent of high-power semiconductors in the last two decades, conventional two-level VSCs are replaced by MLIs. MLIs have become a preferred choice for DC to AC energy conversion applications to ensure high power quality. Voltage source MLIs exhibited higher market penetration and more noticeable improvements than matrix converters and current source inverters over the past decade. The most notable advancements in VSIs are presented in Figure 1.1. Two-level inverters are confined to low-voltage, low-power applications. These converters require more semiconductor devices in series and in parallel to meet medium-, high-power applications (Stemm-

ler, 1994). However, the series and parallel connection of semiconductors do not offer any added benefit to the power quality of the converter. Further, power losses, uneven voltage blocking, and problems in switching the semiconductors string are introduced. Thus, the two-level inverters are not familiar with high-power requirements (Rodriguez et al., 2009a).

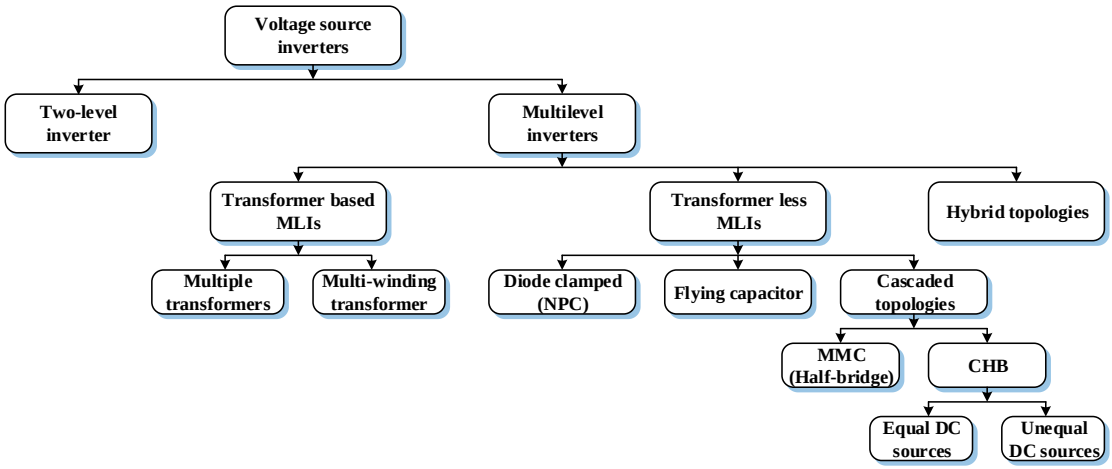


Figure 1.1: Classification of MLIs

New inverter topologies with a higher number of levels and low-cost semiconductor technology are developed for high-power applications. These inverter circuits are referred to as multilevel inverters. The multilevel inverters offer excellent advantages compared with two-level inverters, including low dv/dt, harmonic distortion, near sinusoidal currents, smaller size filters, high-efficiency, low common-mode voltage, and high efficiency and fault-tolerant operation in some instances (Narimani et al., 2014). MLIs generate a stepped voltage waveform using proper controlling methods, semiconductors, and capacitors as virtual voltage sources. Due to MLIs high-quality output waveform, the need of MLIs have increased notably in various domains such as renewables, electric vehicles, motor drives, and UPS systems, etc. (Abu-Rub et al., 2010), (Kouro et al., 2010).

1.2.1 Classical MLI topologies

Several MLI circuits are designed and developed in the past years. Figure 1.2 shows the power circuits of the three classical/traditional topologies. In particular, NPC and FC inverters are well-established for 2.3 - 4.16 kV drive applications. It can be

seen in Figure 1.2(a) that it requires only two gate pulses for the upper two switches, whereas the lower ones receive inverted gating signals to avoid dc-link short-circuit. The NPC topology can be extended to a higher power rating and more output voltage levels by adding additional power switches and clamping diodes. The FC topology is slightly similar to the NPC, with the main difference that flying capacitors replace the clamping diodes, as shown in Figure 1.2(b). As like an NPC, it also requires only two gating pulses. However, the complementary device positions are not the same.

Compared to an NPC, FC has a modular structure that enables its extension to extend to a higher number of levels effortlessly. The modularity of FC also adds to the extra degree of freedom to control the converter with the help of many available redundant states. However, NPC, FC, suffer from many switching components, voltage-balancing issues, and complex control schemes as the voltage levels increase. Due to that, the application of an NPC, FC are limited to three levels by the industries. The problems mentioned above can be overcome with the CHB topology. CHB is suitable for voltage rating higher than 6 kV up to 13.8 kV.

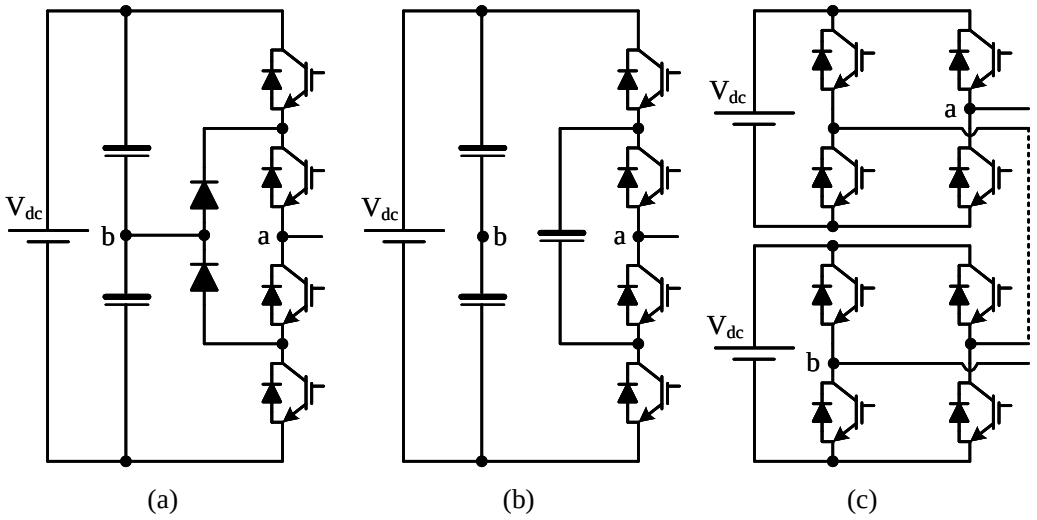


Figure 1.2: Classic multilevel inverter topologies: (a) Three-level NPC, (b) Three-level FC, (c) Five-level CHB

On the other hand, the CHB is well suited for high power applications because of the modularity that enables higher voltage operation with low voltage semiconductors. However, it needs phase-shifting isolation transformers to provide isolated dc sources, which are more bulky and expensive. If the CHB inverter, shown in Figure 1.2(c), is supplied with unequal dc voltage ratios between bridges, some or even all voltage level

redundant switching states can be eliminated, maximizing the number of different voltage levels generated by the converter. This concept of asymmetric voltage supply ratios was proposed in (Mueller and Park, 1994) for magnetic resonance imaging applications. Later this idea was further explored for medium-voltage inverters (Rufer et al., 1999) with two or more cells in series with a powers of two voltage ratio asymmetry (1: 2:...: 2^{n-1}), in powers of three (1: 3:...: 3^{n-1}), and another popular ratio, 1: 2: 6:...: 2Σ(previous ratios), were introduced that eliminate all redundancies, maximize the number of levels. Due to modularity and a simple control scheme, CHB stands out at the cost of individual isolated DC sources for each bridge.

1.2.2 Emerging topologies

Various topologies are introduced in the literature to overcome the drawbacks of classical converters. Several efforts have been made to generate higher voltage levels with less part count in the recent past. The idea of using a capacitor as an intermediate voltage level generating device has gained more attention. In this regard, (Wang et al., 2015), (Khoshkbar-Sadigh et al., 2016) are presented configurations in the combination of FCs and reduced component count with lower switch stress. In hybrid MLIs with FCs, capacitors play a vital role in producing voltage levels. However, to maintain the capacitor voltages at the requisite reference value, a complex control circuit is involved (Sandeep and Yaragatti, 2017). The active neutral point clamped (ANPC) topology (Sheng and Ge, 2018) with the combination of NPC, FC is proposed for medium power applications. Nevertheless, these circuits still need a high number of devices. Moreover, only half of the source voltage appears across the load. In other words, these topologies work as voltage step-down inverters.

Aiming at higher voltage levels, authors in (Alishah et al., 2016) proposed a ladder-type inverter structure, whose source voltage magnitudes are selected in asymmetrical nature and also recommends a higher number of bidirectional switches. Structures presented in (Soeiro et al., 2013), (Wang et al., 2017), (Sadigh et al., 2017), and (Nair et al., 2017) require more number of capacitors and switches. Moreover, maximum voltage obtained in (Soeiro et al., 2013), (Sadigh et al., 2017) is half of the supply voltage ($0.5V_{dc}$). Proceeding further, structure (Dao and Lee, 2018) requires more switching components and needs to maintain different voltage references at DC-link capacitors, which intern increases the topology control complexity.

Consequently, an attempt is made to boost the output voltage to meet the requirements. Besides, the development of MLIs is leading to reduce part count, particularly dc sources. In such circuits, transformers are used to step up the voltages, which in turn result in increased size of the system (Marusarz, 1989). A secondary circuit such as front-, back-end boosting converters are incorporated to the inverter topologies in (Liang et al., 2002), (Abdullah et al., 2014). It is worth noted that this type of method solves the capacitor voltage boosting inability but enhances the complexity, cost, and overall size of the converter. SC-MLIs are another promising converter variant and have become an alternative solution to boost output voltage without the requirement of transformers. Besides, SCs do not require any supplement circuit or complex algorithm to balance capacitor voltages. The SC-based inverters are employed in various fields such as renewables, electric vehicles. In such applications, voltage boost is one of the vital requirements for inverter circuit design. New SC structures are developed accordingly with boost ability (Marusarz, 1989) in 1989, (Mak and Ioinovici, 1998) in 1998. Thenceforth, several SC structures are designed on voltage-boosting features. In (Mak and Ioinovici, 1998) and (Hinago and Koizumi, 2012) presented on SCs, which use end side H-bridges to generate the bi-polar output voltage waveform, in which H-bridge switches have to tolerate the magnitude of the output voltage. This part may restrict the converter for specific applications, particularly in the high-power range. Also, these circuits require more capacitors to increase the levels.

Authors in (Axelrod et al., 2005), (Peng et al., 2019) developed SC converter with self voltage balancing; however, use a considerable number of components for higher levels. A seven-level module in (Liu et al., 2018b) is introduced with one dc source and used two capacitors to split the source into equal halves. The maximum voltage stress on semiconductors is V_{dc}. However, the boosting factor is 0.5 and needs more isolated dc sources for the higher-level extension.

An SC converter based on cascaded MLI for high-frequency applications is proposed in (Liu et al., 2013). Each basic cell of SC is comprised of an H-bridge unit. Isolated dc sources are required to extend the topology for higher levels. The authors of (Ye et al., 2014) have derived an SC-MLI with a single dc source from the topology presented in (Liu et al., 2013), which reduced the number of required semiconductors as well as dc sources. However, the boosting factor is unity per capacitor, and the H-bridge at the second-end increases the blocking voltage of the converter. Topology presented in (Barzegarkhoo et al., 2016) has been analyzed for asymmetric

configuration and can produce higher levels with a reduced number of components. However, the boosting factor is unity per capacitor, and the structure suffers from the higher standing voltages across the devices. For high voltage boosting gain, authors of (Saeedian et al., 2018a), (Liu et al., 2018a) have developed asymmetrical circuits with binary boosting factor. However, more capacitors are involved in producing the levels, and stress on the semiconductor devices is more across the H-bridge, which generates polarity.

1.3 Research motivation

In practice, it is challenging to assess various hybrid topologies as they are diverse and represent a vast family (Rufer et al., 1999, Manjrekar et al., 2000). The combination of several MLIs, either traditional or just a part of an individual structure, is termed hybrid MLI. Theoretically, there are innumerable such possible combinations. With such an ingenious arrangement, the advantage of both the topologies can be extracted when put together, which is not achievable by considering them individually. Among the wide-ranging available hybrid MLIs, it is apparent that no specific solution seems to stand out from the others remarkably. Various factors that influence the selection of a particular topology are cost, intended application, and lifespan. Some of the critical topological aspects that are to be considered while assessing the merits of a hybrid MLI are as follows:

1. Number of semiconductors used
2. Total blocking voltage of the converter
3. Optimal controllability of the topology, i.e., the degree of freedom on modulation and capacitor voltages.
4. Possibility of employing asymmetric sources/capacitor voltage ratios in the topology
5. Number of passive components

Parameters 1 and 2 affect the reliability, cost of the inverter. At the same time, the efficiency is influenced by parameters 1, 2, 3, and 5. A number of redundant states and fault-tolerant operations are directly influenced by 1 and 4. Parameter 5 influences

the dynamic response of the inverter. Several efforts are made to generate higher voltage levels with less part count in the recent past. In that process, capacitors as intermediate voltage level generating devices have gained more attention. On this line, the research work in this thesis aims to investigate the hybrid MLIs and synthesize possible topological variations for enhancing the structural and operational behavior of the selected emerging converter families. Besides, it also aims at developing suitable control strategies for the developed structures for their reliable operation. For this study, two converter families, flying-, switched-capacitor are considered.

Having outlined the variants and limitations of the available hybrid topologies, this research is oriented toward developing novel MLI configurations and control strategies to enhance their operational performance in stand-alone and grid-connected applications. Considering the optimization of converter topologies and generating a higher number of voltage levels, the thesis aims at developing 9-, 13-level inverter topologies since these level voltage waveforms are found to exhibit global compliance on the whole standard imposed range (Chaudhuri, 2008).

1.4 Thesis objectives

The main objective of this work is to study and develop novel models of MLI in simulation software and implement them for passive loads as a prototype hardware module. In detail, the objectives are focused towards:

1. Design and develop a flying capacitor based MLI circuits with less component.
2. Design and develop a switched-capacitor based MLI circuits.
3. Design and develop a hybrid (flying capacitor + switched-capacitor) MLI circuits with less component.
4. Systematically evaluate, measure the losses of the developed circuits and compare with state-of-art topologies in terms of performance, component count.

1.5 Thesis organization

There are five chapters and four appendices in this thesis document. The outline of this thesis is highlighted in Figure 1.3.

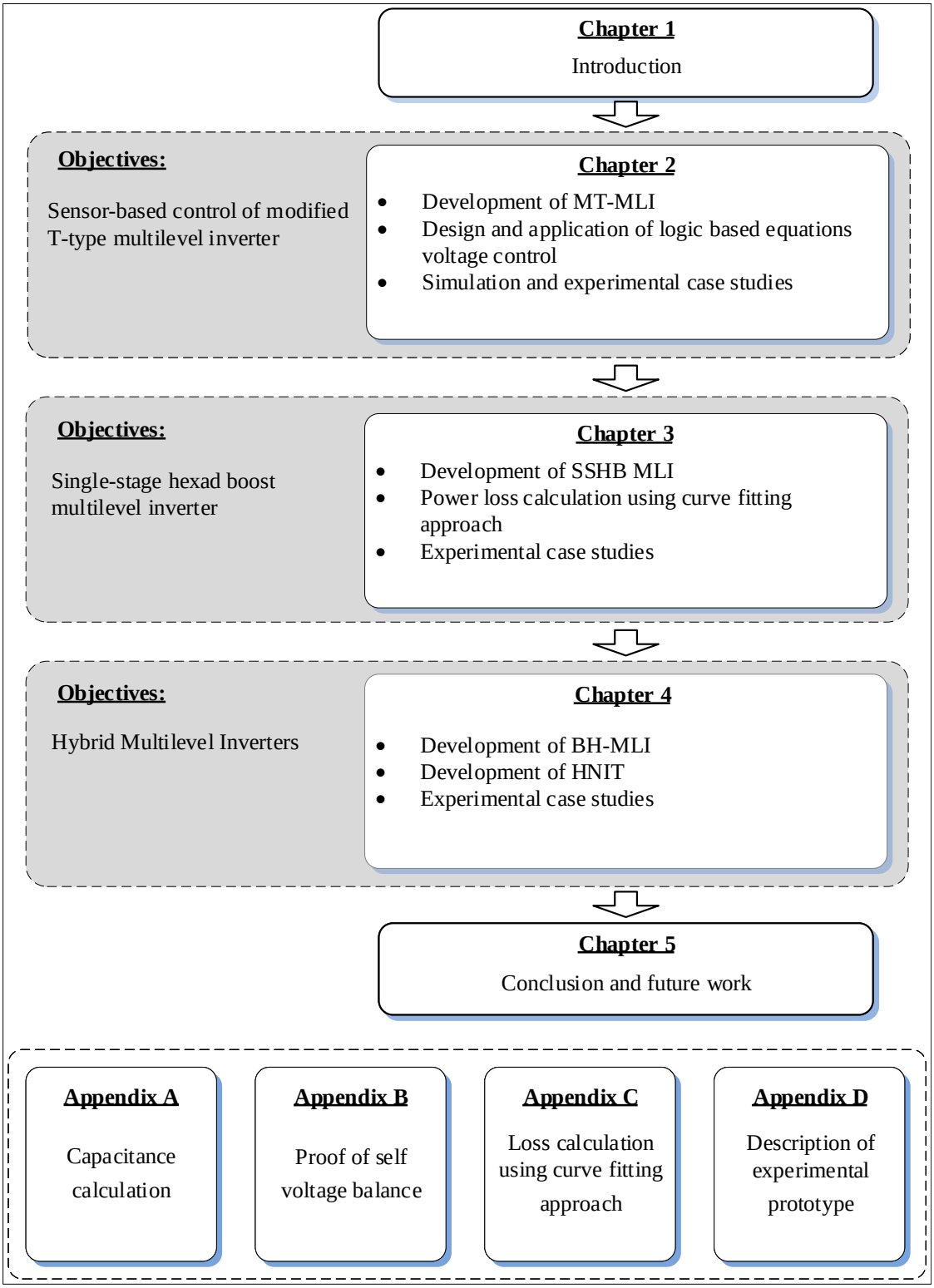


Figure 1.3: Outline of the thesis

Chapter 1 presents a brief introduction to high-power converters, and state-of-the-art MLI topologies and in particular, critically reviews the MLIs with reduced part count and their associated intricacies concerning grid-connected application.

Chapter 2 proposes a MT-MLI with reduced part count. Besides, a sensor-less voltage balancing control to regulate the FC voltage is elaborated. Detailed simulation and experimental studies are carried out to validate the proof of controllability of the proposed topologies and its associated control system. Furthermore, a detailed comparison in terms of the number of power switches, capacitors, and their ratings is deliberated to highlight the potential merits of the proposed MT-MLI.

Chapter 3 introduces a novel SC-based hexad boost 13-level topology with only three capacitors, 14 semiconductor switches, and one diode. The series-parallel technique is utilized effectively to balance the capacitor voltages. The circuit operation, modulation scheme, and extension for higher voltage levels are discussed. Capacitors' voltage ripple and curve-fitting approaches to calculating the power losses are analyzed in detail. Later, experimental results at different loading conditions, modulation indices are presented for validation, followed by a comparative examination. The generic cost comparison is also conducted to estimate the cost of recently presented topologies comprehensively.

Chapter 4 proposes two hybrid MLI configurations: BH-MLI, HNIT with voltage boosting ability, and less component count. The BH-MLI topology can be easily extendable to obtain a higher level output voltage waveform due to its modular switched capacitor cells (SCCs). Besides, the higher voltage level generation does not pose high-voltage stress on any topology components, as the blocking voltage of all devices within the source voltage magnitude. Later two versions of the HNIT circuit are discussed. A simple LGB voltage balancing controller is developed for the presented circuits. Further, a quantitative comparison is conducted among the state-of-art capacitor based MLIs to highlight the superiority of the proposed configurations. Finally, the performance of the proposed

circuits is validated experimentally with PD-PWM and round control method at different modulation indices, load conditions.

Chapter 5 summarizes the significant contributions of the thesis and includes some discussions on possible future research.

Chapter 2

MODIFIED T-TYPE MULTILEVEL INVERTER

2.1 Introduction

This chapter introduces a modified T-type MLI. As the proposed MLI includes an FC, its voltage regulation is imperative for generating an output voltage with equal steps and less harmonic distortion. For this, a sensor-based voltage balancing control to regulate the FC voltage is developed to maintain the same around the reference value. The FC voltage is regulated instantaneously with the LGB controller's help, thereby reducing ripple across the capacitor.

In this chapter, the topological details of the proposed MT-MLI circuit are described in detail, followed by the modulation scheme. Extensions for higher voltage levels are discussed. The simulation and experimental results for stand-alone operation of the MT-MLI circuit are provided with a detailed comparative evaluation.

2.2 MT-MLI circuit

The three possible structures of the proposed MT-MLI inverter with a single DC source arrangement are shown in Figure 2.1. Switching states of corresponding voltage levels for type I and type II structures are formulated in Table 2.1. Note that mid-point four-quadrant switches S_3, S_4 employ only one active switch. Therefore only eight switches are required to form these topologies. With this arrangement, higher

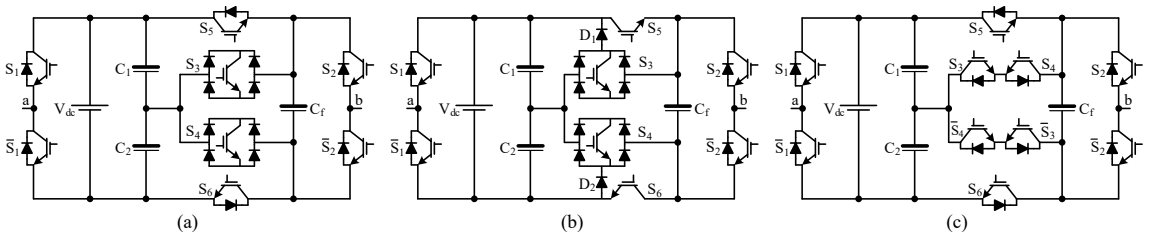


Figure 2.1: MT-MLI structures: (a) Type I (b) Type II (c) Type III

utilization of S_3, S_4 is obtained, but at the cost of the high number of diodes. However, the high number of semiconductors in conduction during voltage levels $\pm 0.25V_{dc}$, $\pm 0.5V_{dc}$, $\pm 0.75V_{dc}$ lead to losses. An alternative configuration for the above types is shown in 2.1(c). Table 2.2 represents the switching states and the corresponding output voltage level formation of type III topology. Since only three devices carry current during voltage levels $\pm V_{dc}$ for both power flow operations (inverter, rectifier), this configuration attains lower conduction losses. Moreover, the circuit implementation of this type is feasible. For instance, the mid-point four-quadrant switches S_3, S_4 can be a common-collector series connection or a common-emitter connection of IGBT switch. With all the above considerations, type III circuit is chosen for the analysis and experimental verification. The notable features of the proposed MT-MLI are:

- Requires lesser components for the generation of same number of voltages levels.
- Total blocking voltage and voltage stress across the switches corresponding to flying capacitor bridge (FCB) units are lesser and thus leads to reduced power losses. As the number of voltage level increases, power loss reduction becomes more significant.
- For a given number of voltage levels and output peak-to-peak voltage value, the required number of dc sources and their magnitudes are halved when compared with the T-type and ANPC topologies.

In fact, the popular configurations like five-level ANPC inverter (ACS5000) concede five distinct output voltage levels ($\pm 0.5V_{dc}$, $\pm 0.25V_{dc}$, 0) with eight switches. Nevertheless, the proposed circuit generates nine output levels ($\pm V_{dc}$, $\pm 0.75V_{dc}$, $\pm 0.5V_{dc}$, $\pm 0.25V_{dc}$, 0) with four pairs of complementary switches (S_1 - $\bar{S_1}$, S_2 - $\bar{S_2}$, S_3 - $\bar{S_3}$, S_4 - $\bar{S_4}$) and two individual switches (S_5, S_6). Herein, the blocking voltage

Table 2.1: Switching table for Type I, Type II

V_o	S_1	S_2	S_3	S_4	S_5	S_6	C_f voltage	
							$i_{inv} > 0$	$i_{inv} < 0$
$1V_{dc}$	0	1	0	0	1	0	N	N
$0.75V_{dc}$	0	0	0	0	1	0	C	D
	0	1	0	1	0	0	D	C
$0.5V_{dc}$	0	1	1	0	0	0	N	N
$0.25V_{dc}$	0	0	1	0	0	0	C	D
	0	1	0	0	0	1	D	C
0	0	0	0	0	0	1	N	N
	1	1	0	0	1	0	N	N
$-0.25V_{dc}$	1	1	0	1	0	0	D	C
	1	1	0	0	1	0	C	D
$-0.5V_{dc}$	1	1	1	0	0	0	N	N
$-0.75V_{dc}$	1	1	0	1	0	1	D	C
	1	1	0	0	0	1	C	D
$-1V_{dc}$	1	0	0	0	0	1	N	N

(0 - OFF, 1 - ON, N - No effect, C - Charge, D - Discharge)

Table 2.2: Switching table for Type III

V_o	S_1	S_2	S_3	S_4	S_5	S_6	C_f voltage	
							$i_{inv} > 0$	$i_{inv} < 0$
$1V_{dc}$	1	0	0	1	0	1	N	N
$0.75V_{dc}$	1	1	0	1	0	1	C	D
	1	0	1	1	0	0	D	C
$0.5V_{dc}$	1	1	1	1	0	0	N	N
$0.25V_{dc}$	1	1	0	0	0	0	C	D
	1	0	1	0	1	0	D	C
0	1	1	1	0	1	0	N	N
	0	0	0	1	0	1	N	N
$-0.25V_{dc}$	0	1	0	1	0	1	C	D
	0	0	1	1	0	0	D	C
$-0.5V_{dc}$	0	0	0	0	0	0	N	N
$-0.75V_{dc}$	0	1	0	0	0	0	C	D
	0	0	1	0	1	0	D	C
$-1V_{dc}$	0	1	1	0	1	0	N	N

(1 - ON, 0 - OFF, N - No effect, C - Charge, D - Discharge)

(maximum voltage across the switch when it is OFF) of the switches S_2, $\bar{S_2}$, S_3 and $\bar{S_3}$ is one-fourth of the input supply ($0.25V_{dc}$), likewise switches S_4, $\bar{S_4}$ blocks the half of the input supply ($0.5V_{dc}$), and the switches S_5, S_6 blocks the three-fourths of the input supply ($0.75V_{dc}$), and remaining switches S_1, $\bar{S_1}$ bear full magnitude of the input supply ($1V_{dc}$). These highest blocking voltage switches (S_1, $\bar{S_1}$) are operated at the fundamental frequency (50 Hz) and the rest of the low power rating switches are operated based on the switching frequency. In the current scenario of semiconductor technology, the requirement of semiconductors with different blocking voltages does not pose any setback to implement the proposed circuit. Moreover, the proposed circuit's half-bridge module nature is an added advantage. And also, these high voltage blocking switches operate at a fundamental reference frequency, which intern results in only considerable conduction losses compared to switching losses.

2.2.1 Modes of operation

Output voltage levels are generated by adding voltage across dc-link capacitors and FC. Switching combination for the respective voltage levels of proposed MT-MLI is listed in Table 2.1, Table 2.2. Type III topology is chosen to show the modes of operation. Figure 2.2 illustrates the operation of various modes with the current path and active switches for the output voltage, $V_o = V_{ab}$. Operating modes for the positive half cycle are explained as follows:

- Maximum positive voltage ($1V_{dc}$): S_1, $\bar{S_2}$, $\bar{S_3}$, S_4, and S_6 are ON, the load point a connecting to dc-link positive and point b to dc-link negative. Thus the voltage at the output $V_o = V_{dc} + 0 = V_{dc}$.

- Three fourth positive voltage ($0.75V_{dc}$): Two possible switching modes are exist. In one mode, S_1, S_2, $\bar{S_3}$, S_4, and S_6 are ON, C_f charges. Thus the voltage across the load is $V_o = V_{dc} - 0.25V_{dc} = 0.75$Vdc. In second mode, S_1, $\bar{S_2}$, S_3, and S_4 are ON, current direction at C_f reversed. Thus the voltage across the load is $V_o = 0.5V_{dc} + 0.25V_{dc} = 0.75V_{dc}$.

- Half positive voltage ($0.5V_{dc}$): S_1, S_2, S_3, and S_4 are ON, the potential point a connecting to dc-link midpoint and point b to the dc-link negative, resulting in the voltage at output is $V_o = 0.5V_{dc} + 0 = 0.5V_{dc}$.

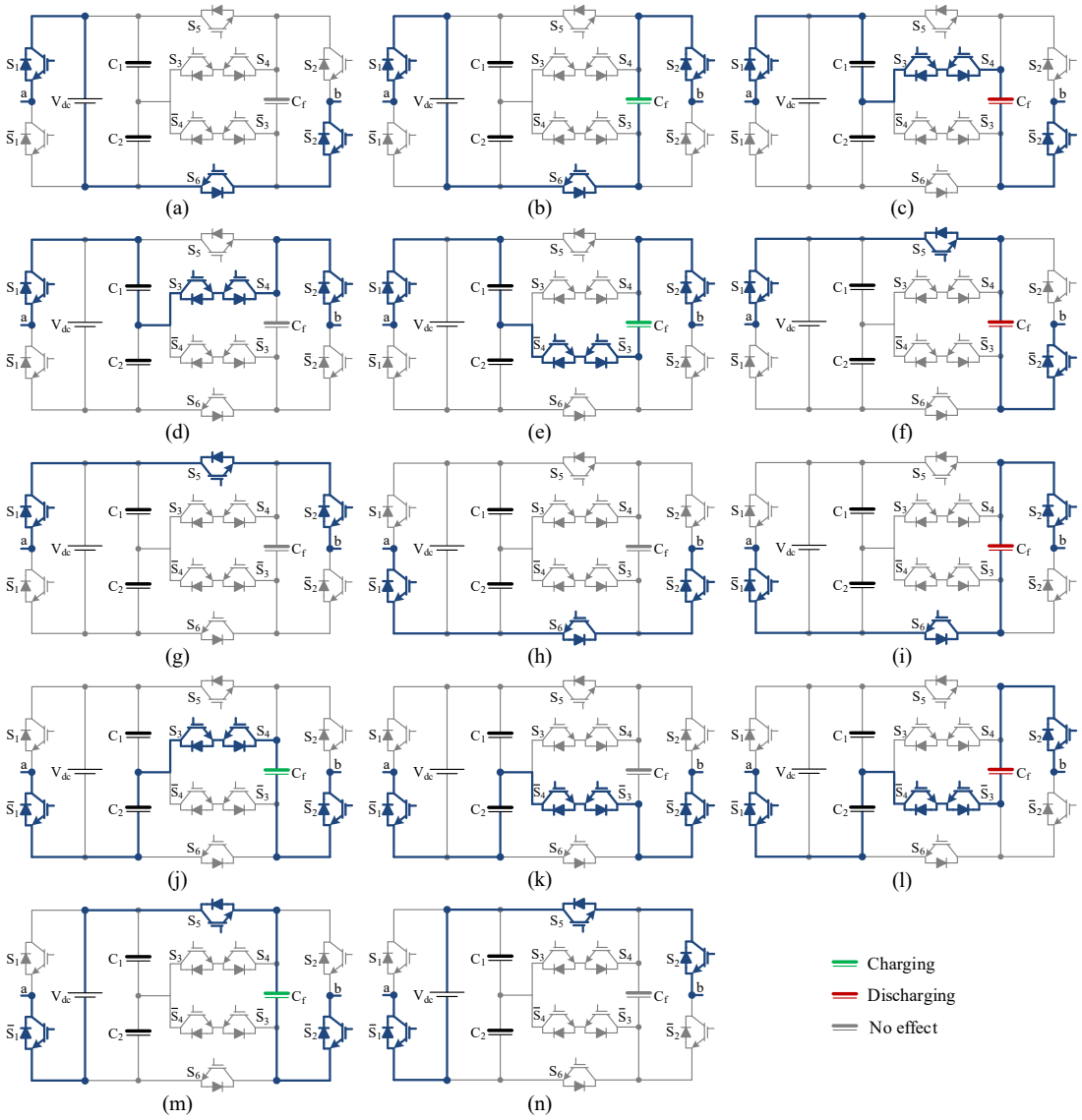


Figure 2.2: Operating states of MT-MLI topology: (a) $1V_{dc}$, (b) $0.75V_{dc}$, (c) $0.75V_{dc}$, (d) $0.5V_{dc}$, (e) $0.25V_{dc}$, (f) $0.25V_{dc}$, (g) 0, (h) 0, (i) $-0.25V_{dc}$, (j) $-0.25V_{dc}$, (k) $-0.5V_{dc}$, (l) $-0.75V_{dc}$, (m) $-0.75V_{dc}$, (n) $-1V_{dc}$.

- One fourth positive voltage ($0.25V_{dc}$): Two possible switching modes are available. In one mode, S_1, S_2, $\bar{S_3}$ and $\bar{S_4}$ are ON, C_f charges. Thus the voltage across the load is $V_o = 0.5V_{dc} - 0.25V_{dc} = 0.25V_{dc}$. In second mode, S_1, $\bar{S_2}$, S_3, $\bar{S_4}$, and S_5 are ON. Thus the voltage across the load is $V_o = 0 + 0.25V_{dc} = 0.25V_{dc}$.

- Zero output voltage ($0V_{dc}$): Two possible switching modes are exist. S_1, S_2, S_3, $\bar{S_4}$ and S_5 are ON or $\bar{S_1}$,$\bar{S_2}$, $\bar{S_3}$, S_4, and S_6 are ON. In both combinations point a and point b are short circuited, resulting in the voltage across the output in both cases is $V_o = 0 + 0 = 0V_{dc}$.

2.3 PWM switching strategy

The FC voltages are usually controlled by applying two types of techniques, namely active and natural balancing approaches (Thielemans et al., 2012). In the active balancing technique, the control algorithm determines suitable switching states followed by unbalanced states to balance the FC voltages. However, this approach propagates uneven switching losses among the switches. Next, the natural balancing technique is specially applied for FC inverters. Herein the capacitor voltage balancing is obtained without any additional control algorithms by using the phase-shifted PWM (PS-PWM) technique. Due to large time constants, in turn, causing poor voltage balancing dynamics, it makes PS-PWM not to use redundant states optimally in some duty ratio ranges (Sadigh et al., 2010), (McGrath and Holmes, 2011). To overcome this issue, a new switching pattern is developed.

In general, the FC voltage starts decreasing when the current leaves the positive plate of the capacitor, and the effect reverses with the reversal of load current. The FC voltage remains unaltered in bypass mode since it neither connects to the load nor the source. Once the effect of each switching state is analyzed thoroughly, the switching strategy required for the generation of the multilevel waveform is developed. One of the critical issues in developing the switching strategy is maintaining the FC voltage at its reference value. The voltage across FC gets diverged from its desired value in generating output voltage levels. Thus a dedicated controller is essential to take care of this issue. Since the proposed MLI exhibits sufficient redundancies, the necessity of an additional controller and a sensor can be confronted by integrating the capacitor balancing feature with the proposed modulation technique. This technique

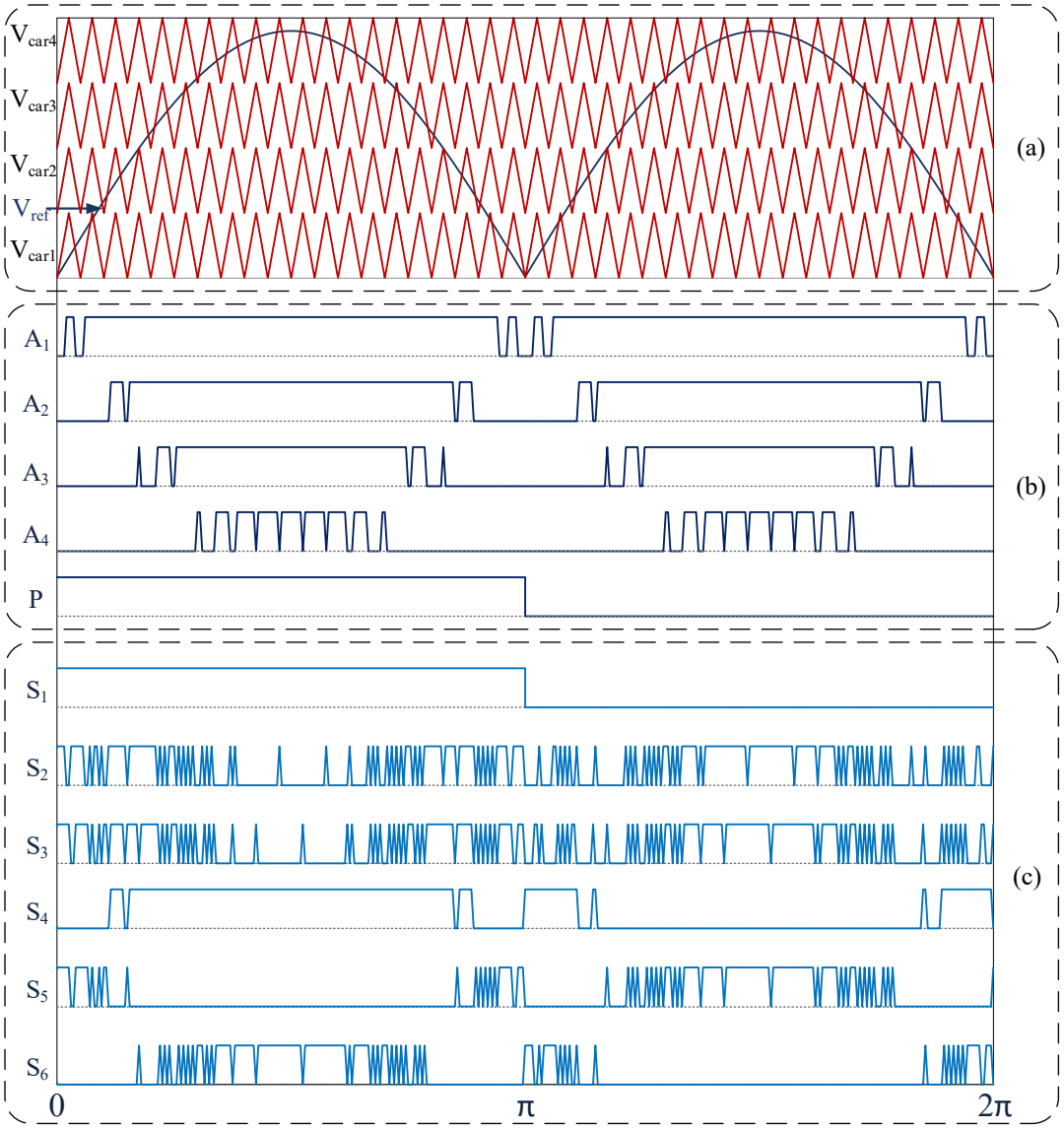


Figure 2.3: PD-SPWM approach: (a) Reference & Carrier waves, (b) Selector signals, (c) Gating pulses.

obviates the need for complex computations and simplifies the control implementation in real-time.

The proposed switching algorithm originates from the level shift PWM technique, where the carrier waves are vertically displaced with equal magnitude and frequency. The proposed control algorithm is built with the PD-SPWM approach, which is portrayed in Figure 2.3(a). A rectified modulated sinusoidal signal (double the fundamental frequency) is considered as a reference signal ($|\mathrm{V_{ref}}|$). The carrier waves ($\mathrm{N_{Car}}$) required to generate $\mathrm{N_l}$ voltage levels at the output is presented as

$$\mathrm{N_{Car}} = \frac{\mathrm{N_l} - 1}{2}. \tag{2.1}$$

The reference voltage is defined by

$$\mathrm{V_{ref}} = \mathrm{V_m sin}\omega\mathrm{t} \tag{2.2}$$

Here, $\mathrm{V_m}$ is peak magnitude of reference wave and amplitude modulation index, m_a, is given by

$$\mathrm{m_a} = \frac{\mathrm{V_m}}{4 \times \mathrm{V_{Car}}} \tag{2.3}$$

where $\mathrm{V_{Car}}$ is peak amplitude of a carrier wave.

The magnitude of m_a usually depends on the $\mathrm{V_m}$. Since the $\mathrm{V_{Car}}$ assumed to be fixed and in the present case and $\mathrm{V_{Car}}$ equals 0.25. For $m_a \leq 0.25$, three levels will be produced in the output voltage. If $0.25 < m_a \leq 0.50$, five levels will be produced in the output voltage, if $0.50 < m_a \leq 0.75$, the output voltage will have seven levels and if m_a is higher than 0.75, nine voltage levels at output will be produced.

The mathematical expression of PWM multilevel voltage waveform in terms of dc offsets, fundamental, carrier harmonics, and their side-band harmonics can be expressed as a double summation Fourier series

$$\begin{aligned}\mathrm{v(t)} = \frac{\mathrm{A_{oo}}}{2} &+ \sum_{n=1}^{\infty} \mathrm{A_{on}} \cos(\mathrm{n}\omega_\mathrm{o}\mathrm{t}) + \mathrm{B_{on}} \sin(\mathrm{n}\omega_\mathrm{o}\mathrm{t}) + \sum_{\mathrm{m}=1}^{\infty} \mathrm{A_{mo}} \cos(\mathrm{m}\omega_\mathrm{c}\mathrm{t}) + \mathrm{B_{mo}} \sin(\mathrm{m}\omega_\mathrm{c}\mathrm{t}) \\ &+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \{\mathrm{A_{mn}} \cos(\mathrm{m}\omega_\mathrm{c}\mathrm{t} + \mathrm{n}\omega_\mathrm{o}\mathrm{t}) + \mathrm{B_{mn}} \sin(\mathrm{m}\omega_\mathrm{c}\mathrm{t} + \mathrm{n}\omega_\mathrm{o}\mathrm{t})\}. \end{aligned} \tag{2.4}$$

The coefficients of (2.4) are expressed in the double Fourier integral as

$$\mathrm{A_{mn}} + \mathrm{jB_{mn}} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} \mathrm{v(x,y)e^{j(mx+ny)}dxdy}. \tag{2.5}$$

Where $\mathrm{x} = \omega_\mathrm{c}\mathrm{t}$, $\mathrm{y} = \omega\mathrm{t}$. To evaluate (2.5), the function $\mathrm{v}(x, y)$ is compared against the carrier wave forms in the x dimension, and the reference waveform in the y dimension.

Table 2.2 report the suitable switching states for the capacitor charging, discharging, and no effect modes over a fundamental cycle. Thus, instantaneous capacitor voltage balance is possible within an inverter half cycle by utilizing switch state redundancy. Moreover, Like (Sadigh et al., 2010), (Chaudhuri et al., 2010), there is no restriction on the amplitude modulation index in the proposed circuit and also no need to maintain an equal width for each level.

Capacitor voltage balancing technique proposed in (Khoshkbar-Sadigh et al., 2016) is adopted to regulate FC voltage. FC voltage is regulated instantaneously in this technique. Firstly, the sensed FC voltage ($\mathrm{V_{C_f}}$) is compared with the reference value ($\mathrm{V_{C_f}|_{ref}}$), and the error is processed through a hysteresis controller. The output of hysteresis controller, from now on, $\Delta_{\mathrm{C_f}}$ has two distinct values; "1" indicating that the FC voltage is lesser than the reference value and thus needs charging and "0" for vice versa given as,

$$\Delta \mathrm{V_{C_f}} = \frac{\mathrm{V_{C_f}}}{\mathrm{V_{C_f}|_{ref}}} - 1 \tag{2.6}$$

$$\Delta_{\mathrm{C_f}} = \begin{cases} 1, & \text{if } \Delta \mathrm{V_{C_f}} \leq 0. \\ 0, & \text{otherwise.} \end{cases} \tag{2.7}$$

It is to note in Table 2.2, that the effect of each state on FC voltage is tabulated assuming that the load current is flowing out of the converter. Thus it is vital to have the information on the polarity of the converter current for the exercise of appropriate switching state. Therefore, a zero crossing detector, from now on, "I" is employed

and is given as,

$$\mathrm{I} = \begin{cases} 1, & \text{if } i_{inv} \geq 0. \\ 0, & \text{otherwise.} \end{cases} \tag{2.8}$$

Further, the procedure for developing a logic form equation based switching function is described. Only those output voltage levels (Table 2.2) where the entry for a particular switch is "1" are considered.

1. Switching function of S_2: S_2 is ON for positive voltage levels $0V_{dc}$, $0.25V_{dc}$, $0.5V_{dc}$ and $0.75V_{dc}$. Since S_2 is to be ON during the voltage level $0V_{dc}$, $0.5V_{dc}$, the term $\bar{A_1}$, $A_2\bar{A_3}$ are to be included, respectively. For the voltage levels $0.25V_{dc}$, and $0.75V_{dc}$, S_2 is ON when the FC needs discharging and if one of the following conditions are satisfied

   - Current is positive ($\mathrm{I} = 1$) and C_f needs to charge ($\Delta_{C_f} = 1$), which is equal to $\mathrm{I} \cdot \Delta_{C_f}$.
   - Current is negative ($\bar{\mathrm{I}} = 1$) and C_f needs to discharge ($\bar{\Delta_{C_f}} = 1$), which is equal to $\bar{\mathrm{I}} \cdot \bar{\Delta_{C_f}}$.

   The above conditions are logically expressed as $\mathrm{I} \cdot \Delta_{C_f} + \bar{\mathrm{I}} \cdot \bar{\Delta_{C_f}}$. Since it is applicable only during voltage levels $0.25V_{dc}$, and $0.75V_{dc}$, the terms $A_1\bar{A_2}P$, $A_3\bar{A_4}P$ are multiplied with it.

2. Switching function of S_5: S_5 is ON for positive output voltage levels $0.25V_{dc}$ and $0V_{dc}$. The term to be included for voltage level $0V_{dc}$ is $\bar{A_1}P$. Coming to voltage level $0.25V_{dc}$, S_5 is ON when the FC needs discharging and if one of the following conditions is fulfilled.

   - Current is positive ($\mathrm{I} = 1$) and C_f needs to discharge ($\bar{\Delta_{C_f}} = 1$), which is equal to $\mathrm{I} \cdot \bar{\Delta_{C_f}}$.
   - Current is negative ($\bar{\mathrm{I}} = 1$) and C_f needs to charge ($\Delta_{C_f} = 1$), which is equal to $\bar{\mathrm{I}} \cdot \Delta_{C_f}$.

   The above conditions are logically expressed as $\mathrm{I} \cdot \bar{\Delta_{C_f}} + \bar{\mathrm{I}} \cdot \Delta_{C_f}$. Since it is applicable only during voltage level $0.25V_{dc}$, the term $A_1\bar{A_2}P$ is multiplied with it. The same principle is applied during the negative half cycle as well.

The switching functions derived using the above principle for all the six switches are as follows:

$$S_1 = P \tag{2.9}$$

$$S_2 = (A_1 \cdot \bar{A_2} + A_3 \cdot \bar{A_4}) \cdot D_1 + (\bar{A_1} + A_2 \cdot \bar{A_3}) \cdot P + A_4 \cdot \bar{P} \tag{2.10}$$

$$S_3 = (A_1 \cdot \bar{A_2} + A_3 \cdot \bar{A_4}) \cdot D_2 + (\bar{A_1} + A_2 \cdot \bar{A_3}) \cdot P + A_4 \cdot \bar{P} \tag{2.11}$$

$$S_4 = (A_2 \cdot \bar{A_3} + A_3 \cdot \bar{A_4} + A_4) \cdot P + (\bar{A_1} + A_1 \cdot \bar{A_2}) \cdot \bar{P} \tag{2.12}$$

$$S_5 = (\bar{A_1} + A_1 \cdot \bar{A_2} \cdot D_2) \cdot P + (A_3 \cdot \bar{A_4} \cdot D_2 + A_4) \cdot \bar{P} \tag{2.13}$$

$$S_6 = (A_3 \cdot \bar{A_4} \cdot D_1 + A_4) \cdot P + (\bar{A_1} + A_1 \cdot \bar{A_2} \cdot D_1) \cdot \bar{P} \tag{2.14}$$

where, $D_1 = (I \cdot \Delta_{C_f} + \bar{I} \cdot \bar{\Delta_{C_f}})$ and $D_2 = (I \cdot \bar{\Delta_{C_f}} + \bar{I} \cdot \Delta_{C_f})$.

2.4 Recommended extensions of MT-MLI

For generating the more number of output voltage levels (>9), the following extensions are recommended in this section.

2.4.1 Structure - 1

To produce more voltage levels at output, FCs are added in cascade manner, as depicted in Figure 2.4. The voltage levels are dependent on the number of FCs connected. The number of FCs and the output voltage levels (N_l) are related as, $N_l = 8 \times 2^{(p-1)} + 1$. Where p is the number of FCs cascaded in series.

The required voltage reference at the added FC is expressed as

$$V_{Cf_p} = \frac{V_{dc}}{4 \times 2^{(p-1)}} \quad p = 1, 2, 3, ... \tag{2.15}$$

2.4.2 Structure - 2

In this method, a facility to integrate multiple sources is achieved by considering the proposed nine-level topology as a fundamental MLI units are cascaded as drawn in Figure 2.5. The voltage across the multiple dc-links is designated as V_{dc_1}, V_{dc_2},...,

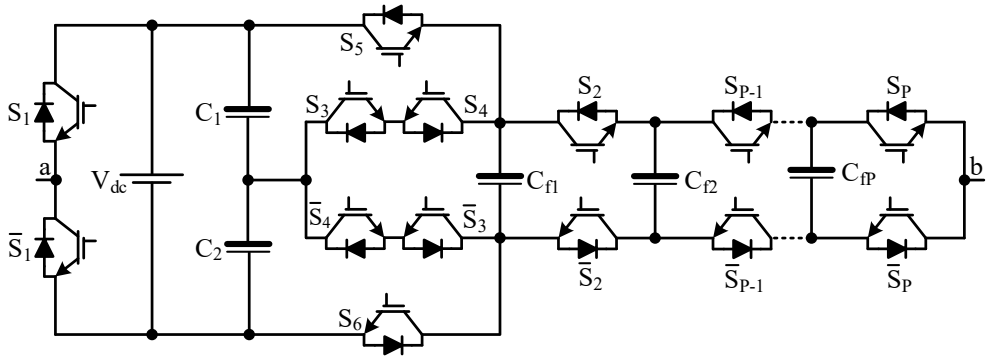


Figure 2.4: Structure - 1: Extension by cascading FCs

V_{dc_q}. The total output voltage between terminals *ab* is the sum of individual proposed MLI outputs and expressed as,

$$V_o = V_1 + V_2 + ... + V_q \tag{2.16}$$

Based on the dc-link voltage magnitude ratios of each cascaded subsystem, the MT-MLI can operate in two modes:

- The total dc-link voltage ratio of each cascade unit is equal (symmetric mode) to one in this mode. In other words $V_{dc_1} = V_{dc_2} = ... = V_{dc_q} = V_{dc}$. The value of N_l is same as that of configuration in structure-1.

- The total dc-link voltage ratio of each cascaded unit differs in the order of two. In other word $V_{dc_1} = 2^0 \times V_{dc}$, $V_{dc_2} = 2^1 \times V_{dc}$,..., $V_{dc_q} = 2^q \times V_{dc}$. The value of N_l is calculated as,

$$N_l = 2 \times \frac{V_{o,peak}}{V_{C_1}} + 1 \tag{2.17}$$

  Here,

$$V_{o,peak} = \sum_{i=1}^{q} V_{dc_i}$$

2.4.3 Structure - 3

In this method, adding more number of FCBs in cascade enables the proposed topology to produce more output voltage levels as shown in Figure 2.6. As the number of

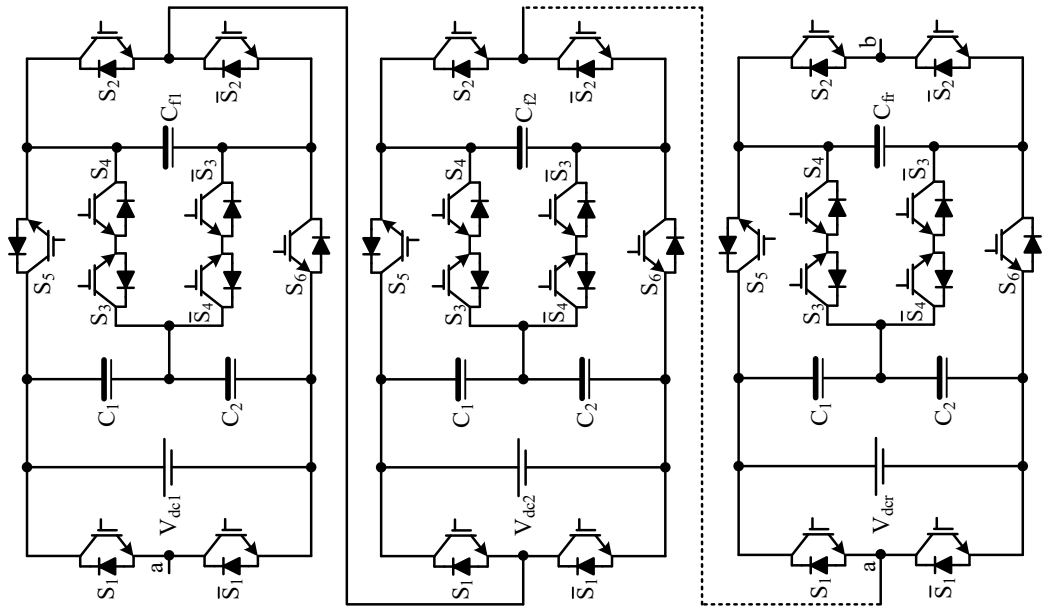


Figure 2.5: Structure - 2: Extension by cascading nine-level fundamental blocks

FCBs increases, voltage stress across switches corresponding to FCB units will reduce and thus leads to reduced power losses. However, when compared to structure - 1, it requires $2m$ extra switches for m added FCs. The relation between the number of FCBs (r) and the number of voltage levels (N_l) is given as, $N_l = 8 \times 2^r + 1$. Where r is the number of FCB modules joined in cascade.

The voltage to be maintained across the appended FCs of the FCB is obtained using,

$$V_{Cf} = \frac{V_{dc}}{4 \times 2^r} \quad r = 0, 1, 2, 3, ... \tag{2.18}$$

As a consequence of such an addition, the topology attains modularity and easily

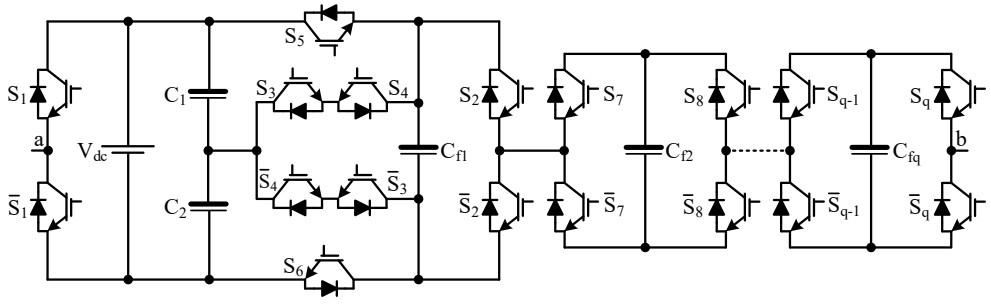


Figure 2.6: Structure - 3: Extension by cascading H-bridges

scalable. Which also translates in higher reliability since failure in any of the FCB will not shut down the entire MLI instead enables it to operate at a lower number of voltage levels by bypassing the defective cell(s).

2.5 Simulation and hardware studies

2.5.1 Simulation study

Simulations are carried out in MATLAB/Simulink environment. Firstly, a stand-alone system with an input voltage of 230 V root mean squared (RMS) with different variations of the passive load is considered. The minimum capacitance value needed with 2.5% voltage-ripple for C_1, C_2, C_f is 1000 μF, 1000 μF, and 0.1 mF, respectively. A detailed capacitance calculation is included in Appendix A. The steady-state waveforms at $m_a = 1$ is shown in Figure 2.7(a). Voltage of capacitor C_f is balanced at a peak of 81.25 V and capacitors C_1, C_2 at 162.5 V each. The achieved peak output voltage is nearly equal to 325 V, with nine different levels between +325 V to -325 V. The fundamental RMS values of load voltage, current are 230 V, and 3.67 A respectively. Capacitor voltages, load voltage and currents at different load conditions are portrayed in Figure 2.7(b)-(f). The dynamic change is applied to the load and supply voltage at t_{tr} sec. In first scenario, the inverter load is changed from (90 + j56.54) Ω to (180 + j113.09) Ω and in second scenario, load is changed from 90 Ω to (90 + j56.54) Ω. Figure 2.7(d) shows the sudden increment in load from (90 + j56.54) Ω to (90 + j56.54) Ω. A sudden change is applied on load from no load to full load in Figure 2.7(e). A step increment in supply voltage is also applied to the converter input in Figure 2.7(f). All the capacitor voltages are maintained their reference value at all dynamic changes in load and supply. It is perceived from the figures that the output voltages, currents, and capacitors' voltages are at their expected values. Therefore, the proposed inverter has a fast and proper voltage and current response under sudden changes in power conditions.

Secondly, a three-phase grid-connected case study is considered to validate the proposed topology. The basic architecture of a three-phase three-wire shunt active power filter (SAPF) is shown in Figure 2.8. Active power filters (APFs) inject equal and opposite harmonics into the power system to neutralize the harmonics that are generated by other components. APF is controlled to supply the compensating cur-

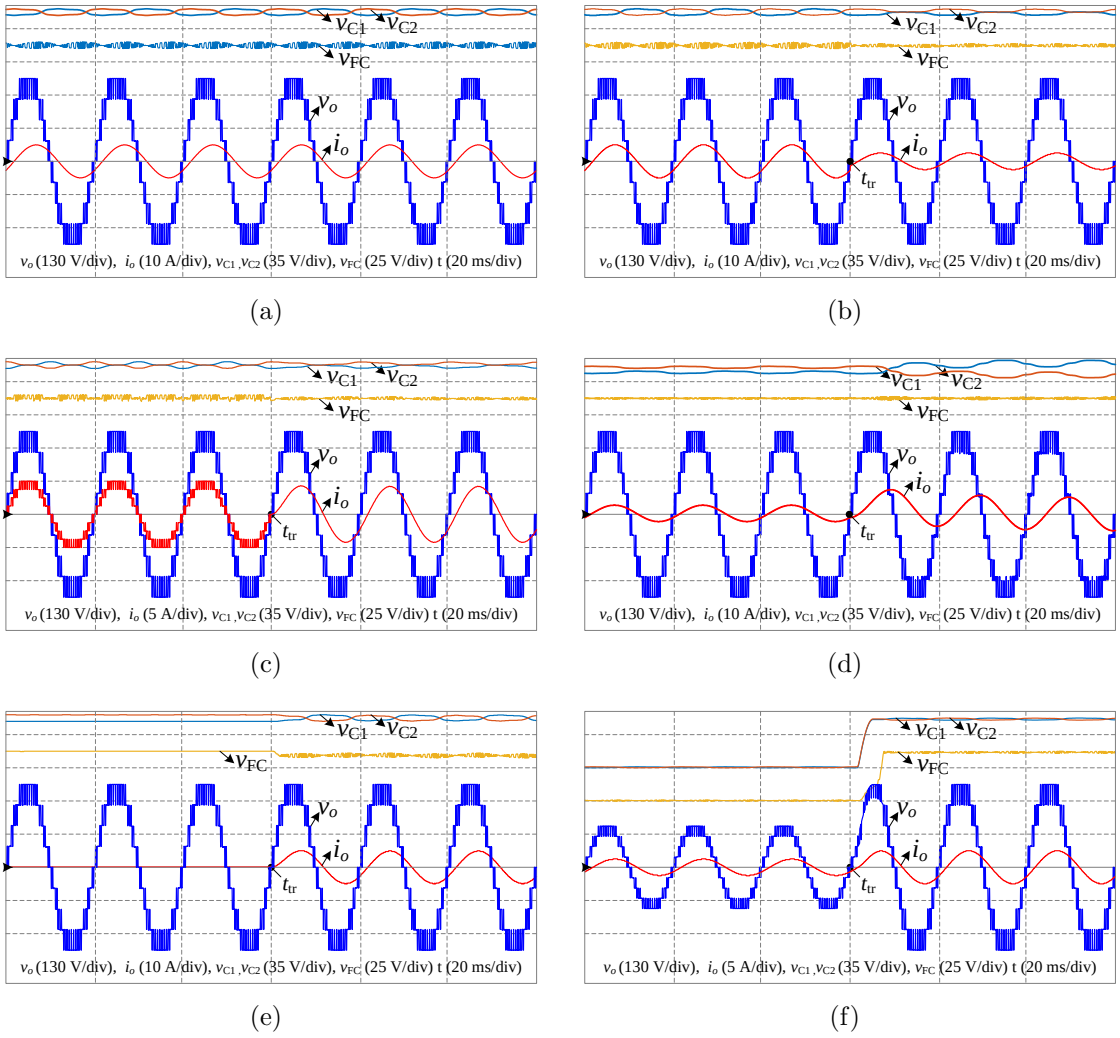


Figure 2.7: Simulation waveforms of stand-alone system: (a) steady-state waveforms at (90 + j56.54) Ω, (b) step increment in load from (90 + j56.54) Ω to (180 + j113.09) Ω, (c) sudden change in load from 90 Ω to (90 + j56.54) Ω, (d) change in power factor from highly resistive load to highly inductive load, (e) dynamic change in load from no-load to full load, (f) step change in supply from 162 V to 325 V.

rent to cancel out the current harmonics on the AC side and reactive power flow to the source, thereby making the source current in phase with the source voltage. The switch-in response of the APF and load dynamics are implemented by incorporating circuit breaker models in the system. A rectifier is a harmonics-producing nonlinear load is connected to the AC mains. The simulation of three APFs with a three-phase and a three-wire system using MATLAB/Simulink along with Sim Power System toolbox are described for the application of harmonics elimination and power factor correction. The MLI is controlled to inject the active power and exchange reactive power with the grid. A standard PQ-based current controller is employed for the control of grid current.

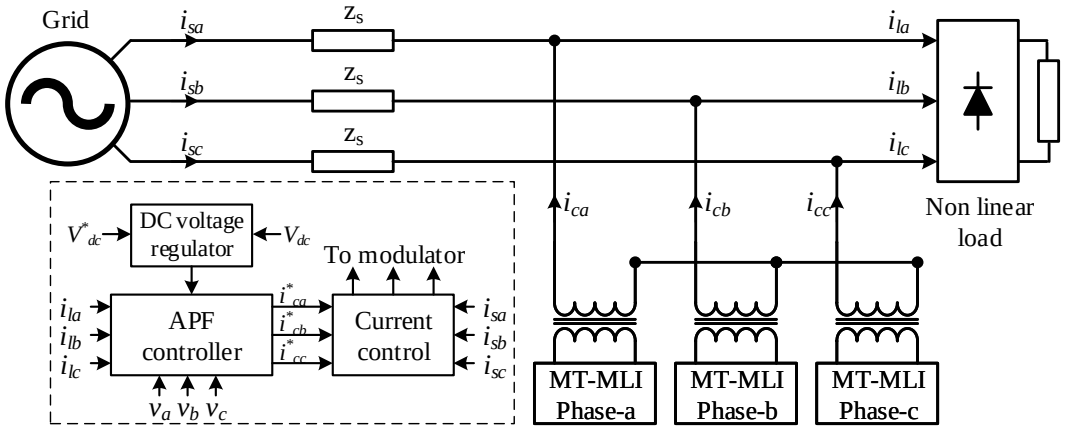


Figure 2.8: Block diagram of shunt active power filter with proposed topology

A diode rectifier is considered as a non-linear load, as shown in Figure 2.8. i_{sx}, i_{lx}, and i_{cx} refer to source, load, and compensating currents of phase x (x = a, b, c). A grid voltage of line-line peak value 415 V with a switching frequency of 2 kHz is considered. The output voltage of the inverter, grid current, injected compensating current are shown in Figure 2.9(a)-(d). As evident in Figure 2.9(b), the grid currents are in phase with the grid voltage confirming the unity PF after t = 0.05 sec. The harmonic spectra of source current before and after applying APF are shown in Figure 2.10(a), (b). All the dominant harmonics are suppressed to a great extent. The results show the satisfactory performance of the proposed converter in APF application for harmonics mitigation and power factor correction in nonlinear loads.

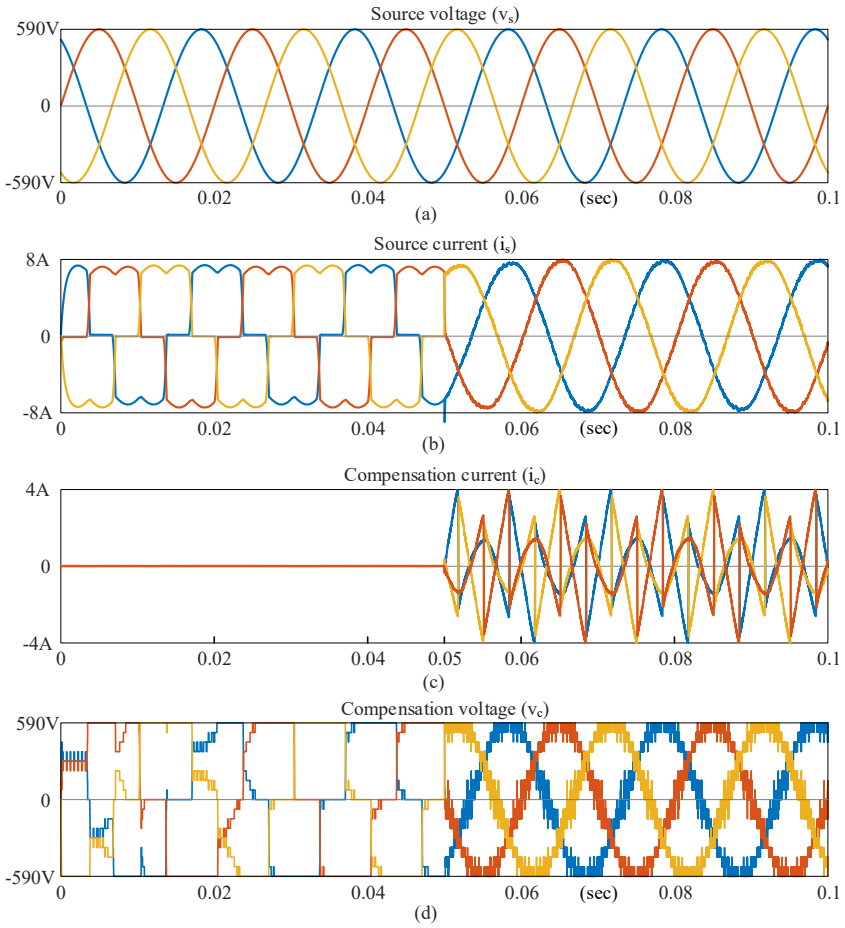


Figure 2.9: Simulation waveforms of shunt active power filter: (a) source voltage, (b) source current, (c) compensating current, (d) compensating voltage.

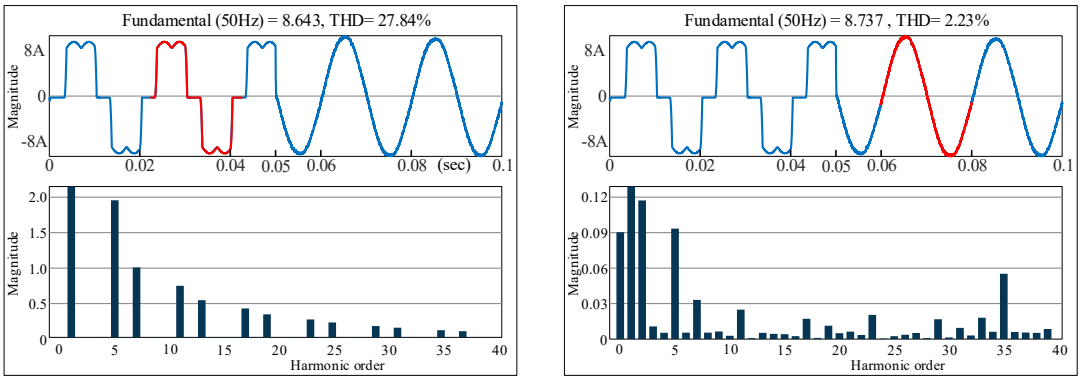


Figure 2.10: FFT spectrum of current waveform (a) before applying APF, (b) after applying APF.

2.5.2 Experimental study

Afterward, the stated features of the proposed inverter are validated experimentally. SKM75GB123D IGBT modules, Capacitor unit, Gate drives (TLP250) along with the dead band circuit, and RL-load are the attributes for building the prototype set up in the laboratory. The Real-Time simulator, OP4200, is employed as a controller which has fed PWM pulses to the proposed MLI. Complete description of prototype set-up is demonstrated in Appendix D. Table 2.3 summarizes the details of attributes considered for the prototype setup. THD versus modulation index graph is portrayed in Figure 2.11. Capacitor, load voltages and currents of nine-level MT-MLI at different load conditions are validated experimentally. The steady-state experimental capacitor voltages, load voltage and current at 30Ω - 2mH load are represented in Figure 2.12(a)-(b). It is obvious that the output voltage waveform is comprised of nine-levels with the magnitude of 50 volts and current magnitude of 1.67 A. Figure 2.12(c)-(d) portraits step change in load from 30Ω - 2mH to 60Ω - 4mH. And also waveforms for dynamic change in load from 30Ω to 60Ω - 4mH are portrayed in Figure 2.12(e)-(f). High inductive - low resistive load is employed to test the proposed topology and results are depicted in Figure 2.12(g)-(h). Load current waveform is sinusoidal with 4.427 A (rms) and lagging behind the output voltage with an angle of 51.488°, since the load is (5 + j6.28) Ω. From the above experimental results, it is proving that the proposed MT-MLI is maintaining its output, FC voltages at reference irrespective of load variation.

Table 2.3: Attributes for hardware set-up

Parameters	Value
dc-link voltage	50 V
Fundamental output frequency	50 Hz
dc-link capacitances (C_1, C_2)	1000 μF, 1000 μF
Flying capacitance (C_f)	0.1 mF
Switching frequency (f_{sw})	2kHz
Load resistance and inductance	30 Ω - 2 mH;
	60 Ω - 4 mH & 10 Ω - 30 mH

The proposed one has the least number of device count without missing switching redundancy as compared with recent developed FC based configurations which are

reported in Table 2.4. Additionally, a single isolated supply is employed to curtail vast input setup and operating with one FC reduces the voltage balancing issue. Further, the peak inverse voltage (PIV), 0.55 *pu* leads to choose the medium voltage rating switches to meet the load requirements. In a nutshell, proposed circuit performing well in terms of part count, PIV, efficiency, and cost.

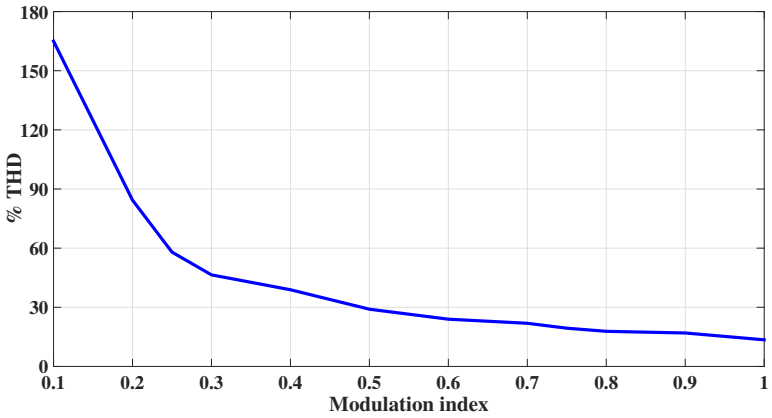


Figure 2.11: THD versus modulation index plot

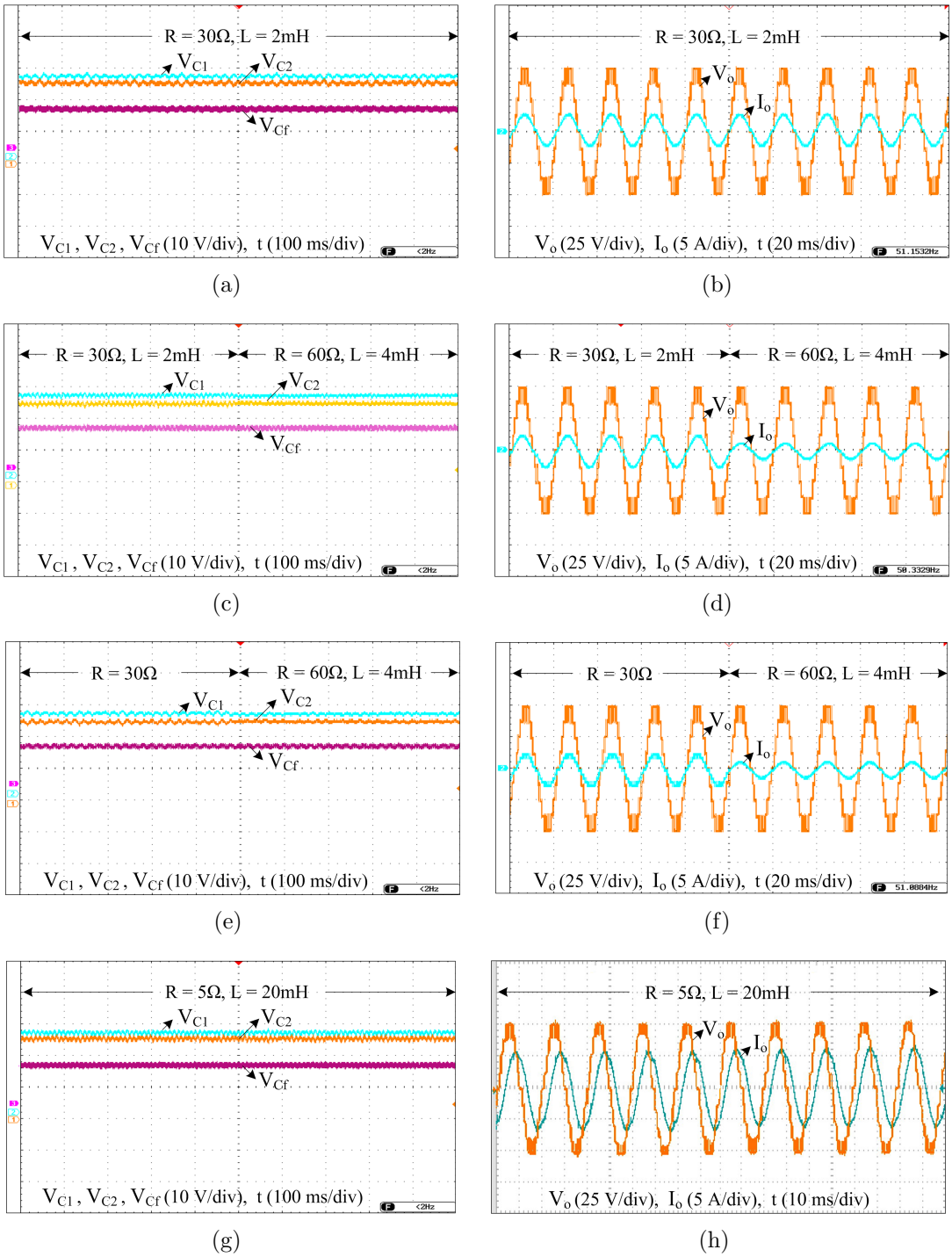


Figure 2.12: Experimental results: (a), (b): Capacitor, load voltages and current at 30 Ω - 2 mH load; (c), (d): Capacitor, load voltages and current at step change in load from 30 Ω - 2 mH to 60 Ω - 4 mH; (e), (f): Capacitor, load voltages and current at dynamic change in resistive-inductive load from 30 Ω to 60 Ω - 4 mH; (g), (h): Capacitor, load voltages and current at 5 Ω - 20 mH load.

Table 2.4: Comparative analysis of the proposed configuration with recently developed topologies

Parameter		Topology										
		1	2	3	4	5	6	7	8	Proposed Type I	Proposed Type II	Proposed Type III
N_{sw}		10	9	14	12	12	12	14	12	8	8	10
N_{dc}		2	1	2	2	2	2	2	2	1	1	1
N_{diode}		0	1	0	0	0	0	0	0	8	10	0
N_{cf}		2	1	3	3	2	1	2	3	1	1	1
V_{Cf}	$1V_{dc}$	0	1	0	0	0	0	0	0	0	0	0
	$0.5V_{dc}$	1	2	0	1	1	1	1	0	0	0	0
	$0.25V_{dc}$	1	0	2	1	1	1	1	0	1	1	1
	$0.125V_{dc}$	0	0	1	1	0	0	0	3	0	0	0
PIV(p.u)		0.85	2.1	0.4	0.6	0.7	0.6	7.5	1.05	0.825	1.0	0.55

N_{sw} - No. of switches, N_{dc} - No. of DC sources, N_{Cf} - No. of flying capacitors, N_{diode} = no. of diodes.

1. Chaudhuri et al. (2010)
2. Liu et al. (2018a)
3. Nair et al. (2017)
4. Barbosa et al. (2005)
5. Li et al. (2011)
6. Sandeep and Yaragatti (2017)
7. Chaudhuri et al. (2007)
8. Rajeevan et al. (2013)

Chapter 3

SINGLE-STAGE HEXAD BOOST MULTILEVEL INVERTER

3.1 Introduction

In the previous chapter, a reduced component count MT-MLI circuit with unity voltage gain is presented. An uncomplicated sensor-based voltage balancing is developed to control the FC voltages. In this chapter, a switched-capacitor-based MLI with a voltage gain of six will be discussed. The principle of the series-parallel technique is adopted to charge and discharge the capacitors. For this, a control strategy without voltage, current sensors is developed to maintain the capacitor voltage around the reference value. The advantages of such a control scheme are reduced control requirement, cost, and overall system intricacies.

This chapter is composed as follows: The proposed structure's circuit description and operating principle are discussed, followed by the developed PWM switching strategy. Possible extensions for high voltage levels are discussed. Further, experimental verifications at different loading conditions and loss calculation of the proposed configuration are provided.

3.2 SSHB topology

Figure 3.1 depicts the proposed single-stage hexad boost (SSHB) inverter circuit. As the name implies, SSHB produces six times boosted output with the magnitude of

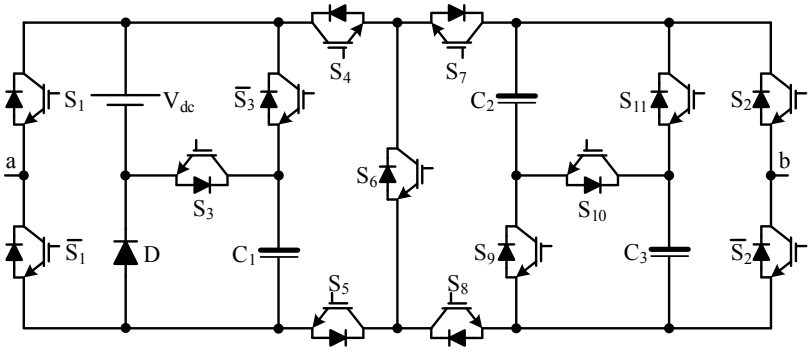


Figure 3.1: 13-level SSHB inverter topology

$1V_{dc}$ for each level and provides 13-levels in output voltage. The SSHB generates 13-levels from $6V_{dc}$ to -$6V_{dc}$ with 14 power electronic switches, three capacitors, and one diode. Capacitors C_1, C_2, and C_3 are charged-discharged several times with series-parallel technique to generate all levels expect zero and $\pm 1V_{dc}$. The equivalent switching circuitries for all 13 voltage-levels/modes are portrayed in Figure 3.2, 3.3. The green, red, and grey capacitors indicate the charge, discharge, and no effect states, respectively. Another notable benefit of the proposed SSHB is that it forms zero and negative levels without a back-end H-bridge. Therefore, lower-voltage rated semiconductor switches can be used in the inverter. The blocking voltages of the semiconductors are examined and enlisted in Table 3.1. The blocking voltage of the semiconductors does not exceed four times of source voltage even for higher levels.

Table 3.1: Peak voltage across each component of SSHB circuit

Component	Peak voltage
S_3, D	V_{dc}
S_1, S_4, S_5 S_6, S_9, S_{10}, S_{11}	$2V_{dc}$
S_2, S_7, S_8	$4V_{dc}$
C_1	V_{dc}
C_2, C_3	$2V_{dc}$

Table 3.2 shows the switching pattern and the effect on the capacitor for the respective voltage level. Here C, D, -, 1, and 0 stands for a charge, discharge, idol, ON, and OFF, respectively. Capacitors C_1, C_2, and C_3 charge, discharge several times, as shown in Table 3.2. Capacitor C_1 charges to the source voltage V_{dc} through $\bar{S_3}$, D. C_2, C_3 charge to twice the source voltage through switches S_3 - S_5, S_7 - S_9,

and S_{11}. Load impedance does not affect the charging loop's time constant, and capacitor voltages instantly reach their final value because semiconductors' parasitic resistance is meager. However, load impedance increases the discharging loop's time constant while discharging the capacitors because the load resistance is high compared to the component parasitic resistance. Thereby, capacitor voltages are maintained at required values even with few charging modes. It is worthy of mentioning that the C_1, C_2, and C_3 voltages are kept at V_{dc}, $2V_{dc}$, and $2V_{dc}$ (by neglecting component voltage drop) without any additional balancing circuit, therefore, reduced control complexity.

Table 3.2: Switching table for the 13-level SSHB-MLI

$V_o = V_{ab}$	Switch											Capacitor state		
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	C_1	C_2	C_3
$6V_{dc}$	1	0	1	0	1	1	1	0	0	1	0	D	D	D
$5V_{dc}$	1	0	0	0	1	1	1	0	0	1	0	C	D	D
$4V_{dc}$	1	0	1	0	1	1	1	0	1	0	0	D	D	-
$3V_{dc}$	1	0	0	0	1	1	1	0	0	0	1	C	-	D
$2V_{dc}$	1	0	1	1	1	0	1	1	1	0	1	D	C	C
V_{dc}	1	0	0	0	1	0	0	1	0	0	0	C	-	-
0	1	1	0	1	0	0	1	0	0	0	0	-	-	-
0	0	0	0	0	1	0	0	1	0	0	0	-	-	-
$-V_{dc}$	0	1	0	1	0	0	1	0	0	0	0	C	-	-
$-2V_{dc}$	0	1	1	1	1	0	1	1	1	0	1	D	C	C
$-3V_{dc}$	0	1	0	1	0	1	0	1	0	0	1	C	-	D
$-4V_{dc}$	0	1	1	1	0	1	0	1	1	0	0	D	D	-
$-5V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	C	D	D
$-6V_{dc}$	0	1	1	1	0	1	0	1	0	1	0	D	D	D

(1 - ON, 0 - OFF, D - Discharge, C - Charge, - - No effect)

3.3 Modulation strategy

Several modulation approaches are available to generate a required output waveform in multilevel inverters Kouro et al. (2010). Fundamental frequency switching (nearest level control), selective harmonic elimination pulse width modulation (SHE-PWM),

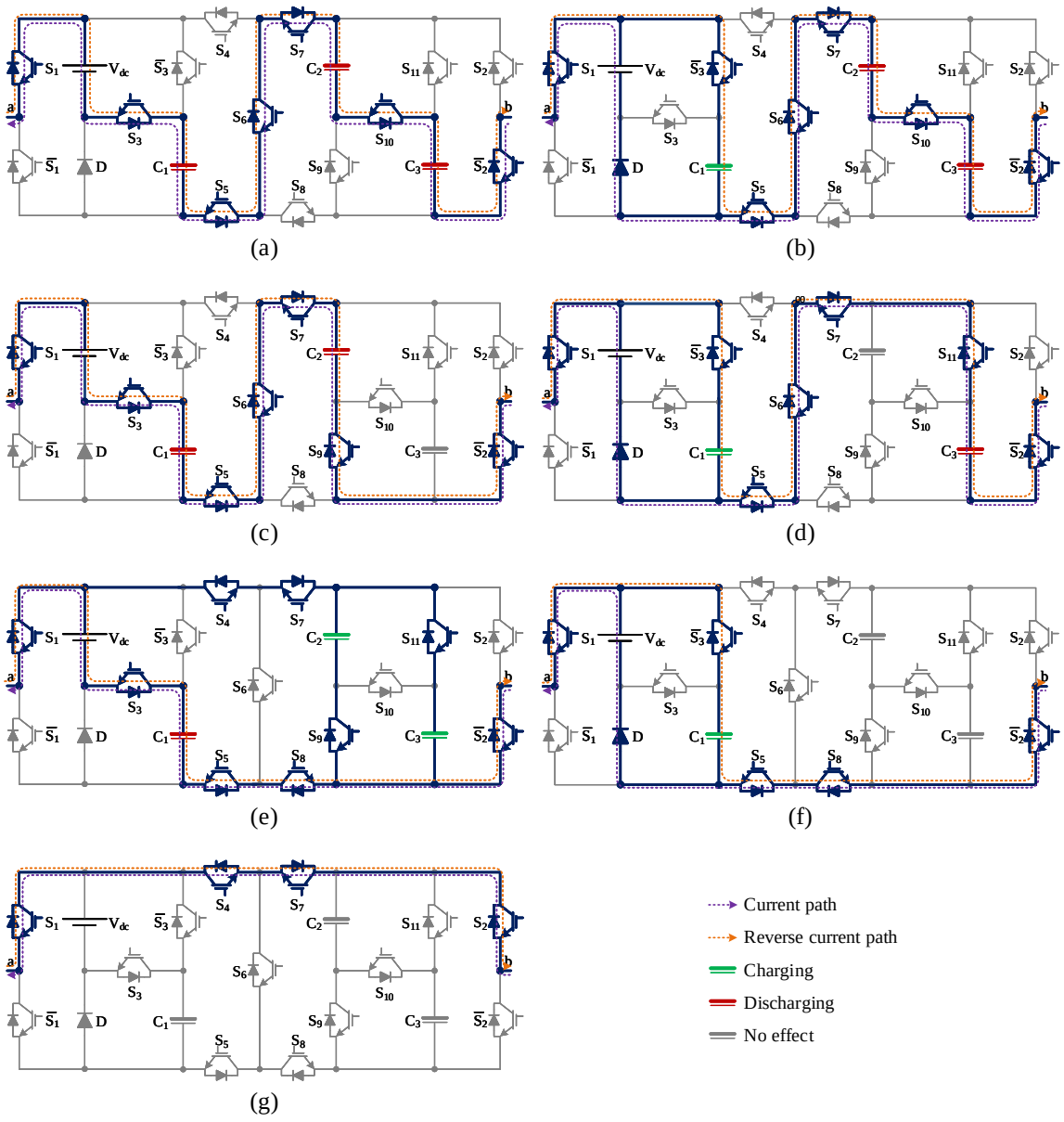


Figure 3.2: Positive levels of SSHB-MLI: (a) $6V_{dc}$, (b) $5V_{dc}$, (c) $4V_{dc}$, (d) $3V_{dc}$, (e) $2V_{dc}$, (f) $1V_{dc}$, (g) $0V_{dc}$.

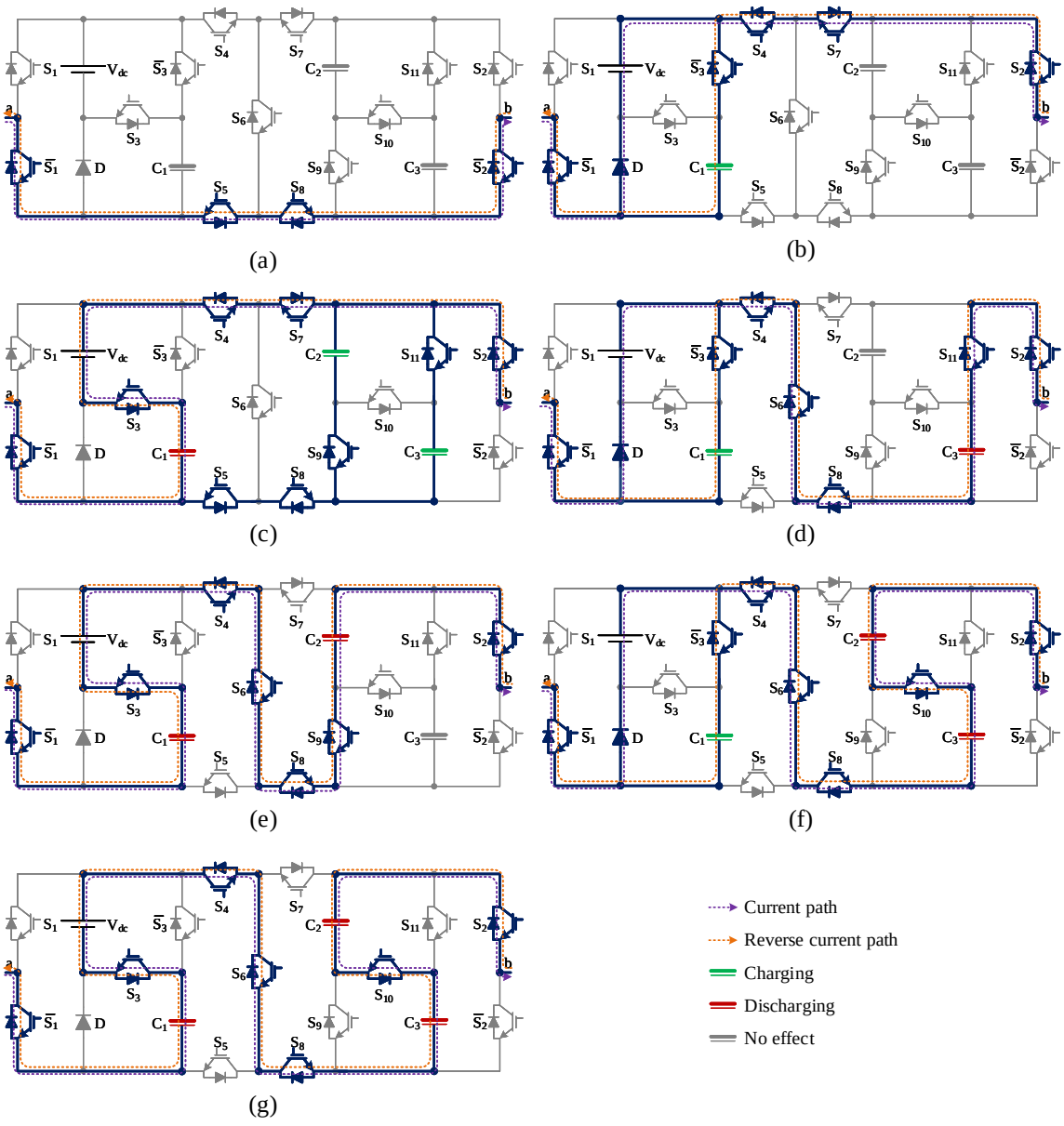


Figure 3.3: Negative levels of SSHB-MLI: (a) $0V_{dc}$, (b) $-1V_{dc}$, (c) $-2V_{dc}$, (d) $-3V_{dc}$, (e) $-4V_{dc}$, (f) $-5V_{dc}$, (g) $-6V_{dc}$.

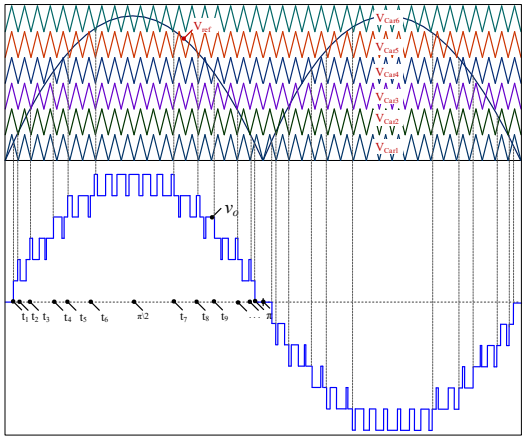


Figure 3.4: Key waveform of SSHB MLI with PD-PWM technique

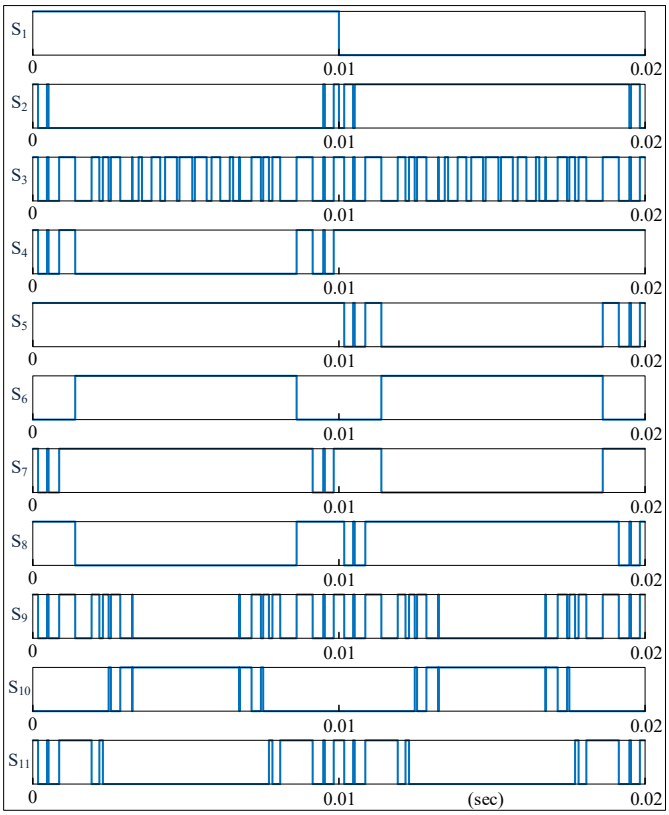


Figure 3.5: Gating pulses of the switches for 13-levels

sinusoidal PWM, space vector PWM, and other (Venkataramanaiah et al., 2017), (Jammala et al., 2018), (Azeem et al., 2019) switching techniques are applied in multilevel inverters to produce staircase output waveforms. Phase-disposition PWM control strategy is employed to generate the gating signals to the semiconductors. An absolute sinusoidal reference ($V_{ref} = |V_m sin(\omega t)|$) is compared with level-shifted, in-phase triangular carrier waves (V_{car1} - V_{car6}) to generate pulses. Besides, carrier signals like absolute-sinusoidal, ramp, trapezoidal are also equally suitable for the proposed inverter. In this technique, $(N_l - 1)/2$ carrier waves are needed to create N_l levels. Figure 3.4 depicts the key waveforms with the fundamental reference frequency of 50 Hz and the carrier frequency of 2 kHz. Only six carriers (V_{car1} - V_{car6}) with equal frequency but different off-set voltages are used to produce 13 output voltage levels. Semiconductors' gating pulses are derived according to Table 3.2 and are portrayed in Figure 3.5. Amplitude modulation index, m_a in terms of carrier waveforms and reference is represented as

$$m_a = \frac{V_m}{\left(\frac{N_l - 1}{2}\right) \times \widehat{V}_{Car}} \tag{3.1}$$

Where $\widehat{V}_{Car}$, V_m are the peak amplitude of the carrier signal, peak magnitude of the reference wave, respectively. The RMS of the voltage at a-b terminals of the topology can be measured as

$$V_{ab} \simeq m_a \frac{6V_{dc}}{\sqrt{2}} \tag{3.2}$$

3.4 Extension methods for higher levels

The SSHB circuit can be extended to produce more voltage levels at output terminals. Two different extension methods are discussed in this section.

3.4.1 Structure - 1

To produce more voltage levels at output, capacitors are added in cascade manner, as depicted in Figure 3.6. The voltage levels are dependent on the number of SCs connected. For the effective levels generation, the required voltage to be maintained at the capacitor C_1 is V_{dc}, and remaining capacitors C_2, C_3, C_4,...C_n is $2V_{dc}$. Com-

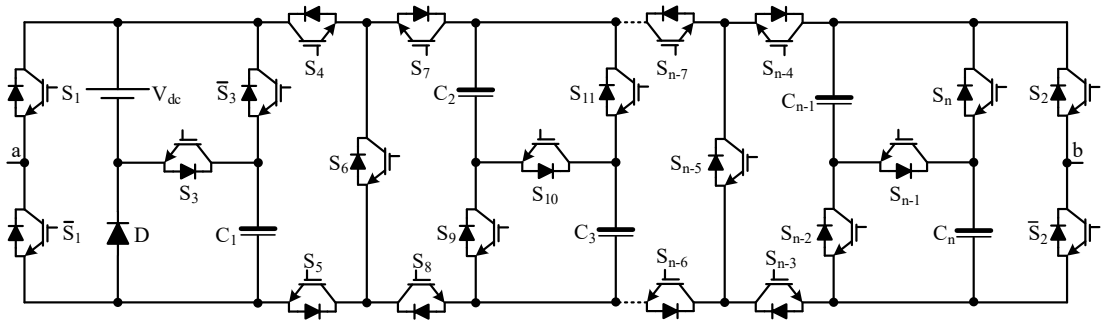


Figure 3.6: Extension structure - 1

ponents required for the generation of n-levels (N_l) can be given as

- No. of switches, $N_{Sw} = (N_l + 1)$
- No. of diodes, $N_{diode} = 1$
- No. of capacitors, $N_{Cap} = \left(\frac{N_l - 1}{4}\right)$
- Voltage boosting factor, VBF $= \left(\frac{N_l - 1}{2}\right)$
- Peak Inverse voltage $= 4V_{dc}$

3.4.2 Structure - 2

By considering the proposed 13-level topology as a fundamental block/unit, a facility to integrate multiple sources as shown in Figure 3.7 is achieved.

- The voltage across the multiple dc-links is designated as V_{dc_1}, V_{dc_2},..., V_{dc_m}.
- The total output voltage between terminals ab is the sum of individual proposed MLI outputs and expressed as, $V_o = V_1 + V_2 + ... + V_m$

Based on the DC-link voltage magnitude ratios of m-module, the SSHB can operate in three modes:

1. Unity: The total dc-link voltage ratio of each cascade unit (m) is equal to one, i.e., $V_{dc_1} = V_{dc_2} = ... = V_{dc_m} = V_{dc}$.

   $N_l = 12m + 1$; VBF $= 6m$.

2. Binary: The total dc-link voltage ratio of each cascaded unit differs in the order of two, i.e., $V_{dc_1} = 2^0 \times V_{dc}$, $V_{dc_2} = 2^1 \times V_{dc}$,..., $V_{dc_q} = 2^3 \times V_{dc}$.

   $N_l = 12 \times 2^m$ - 11; VBF = 6×2^m - 6.

3. Ternary: The total dc-link voltage ratio of each cascaded unit differs in the order of three, i.e., $V_{dc_1} = 3^0 \times V_{dc}$, $V_{dc_2} = 3^1 \times V_{dc}$,... $V_{dc_m} = 3^m \times V_{dc}$.

   $N_l = 6 \times 3^m$ - 5; VBF = 3×3^m - 3

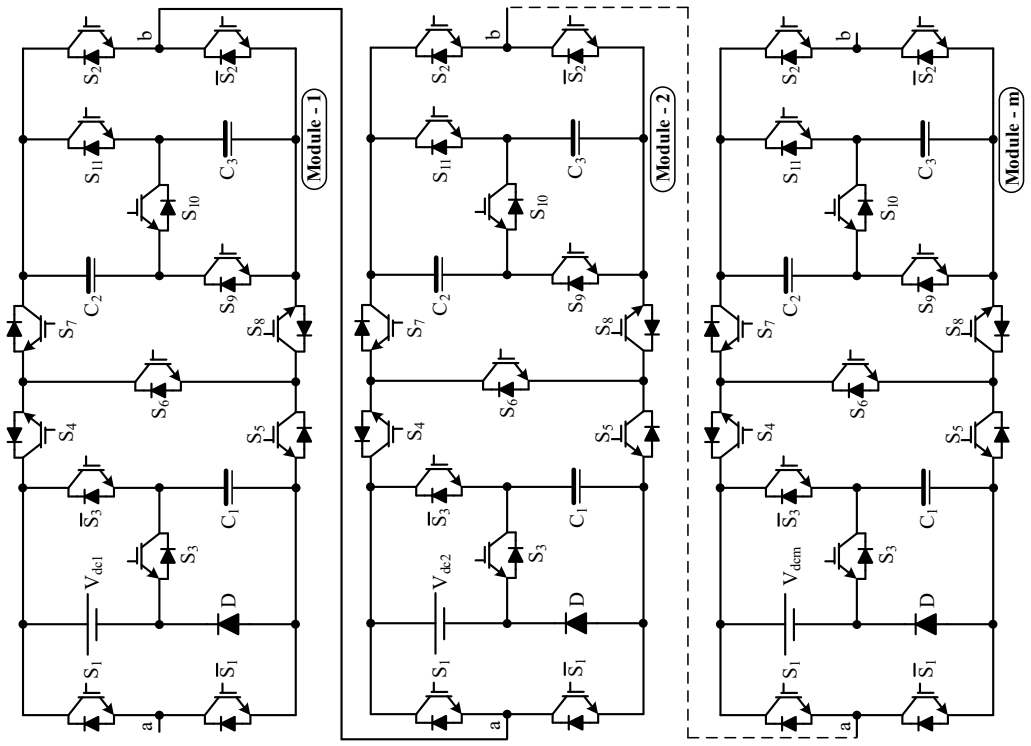


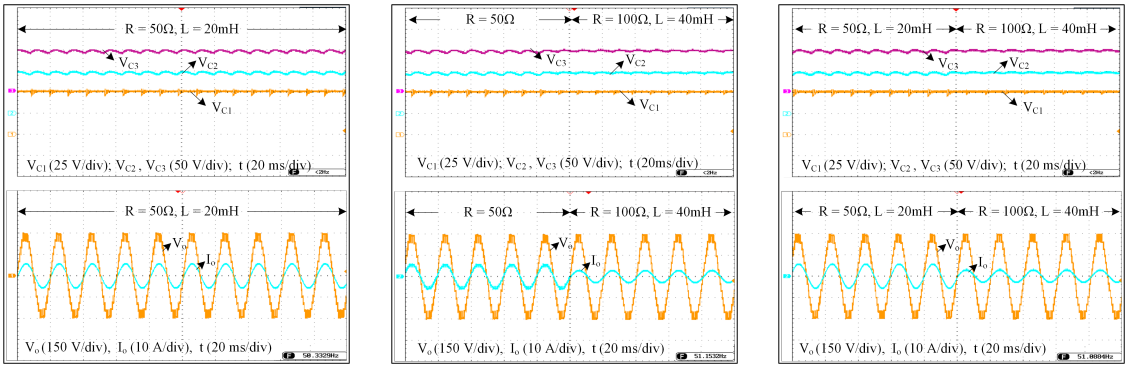
Figure 3.7: Extension structure - 2

3.5 Experimental results

An experiment is executed for 13 levels to verify the proposed SSHB-MLI with the parameters mentioned in Table 3.3. A setup picture representing the developed inverter circuit is shown in Figure 3.10. The proposed converter is executed using SKM75GB123D IGBT modules, TLP250 gate drives along the dead band circuit. The minimum capacitance value needed with 16% voltage-ripple for C_1, C_2, C_3 is

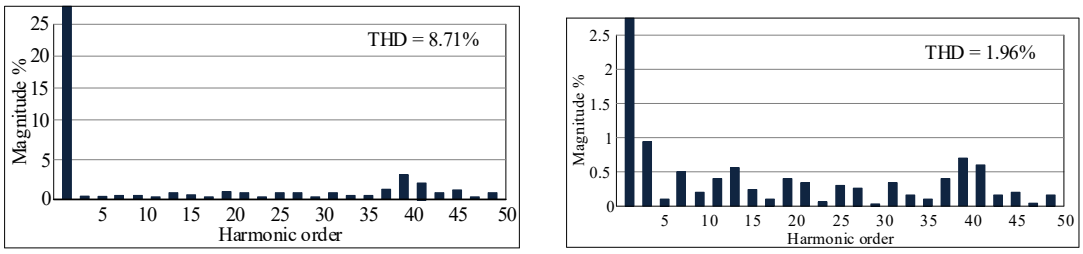
Table 3.3: Attributes for hardware set-up

Parameters	Value
DC-link voltage	50 V
Fundamental output frequency	50 Hz
Capacitance of capacitors (C_1, C_2 & C_3)	1.2 mF each
Switching frequency (f_{sw})	2 kHz
Load resistance and inductance	50 Ω - 20 mH
	100 Ω - 40 mH & 50 Ω



(a) (b) (c)

Figure 3.8: Experimental waveforms: (a) at 50 Ω - 20 mH load, (b) dynamic change in load from 50 Ω to 100 Ω - 40 mH, (c) step increase in load from 50 Ω - 20 mH to 100 Ω - 40 mH.



(a) (b)

Figure 3.9: FFT spectrum of SSHB: (a) harmonic profile of 13-level load voltage waveform, (b) harmonic profile of load current waveform.

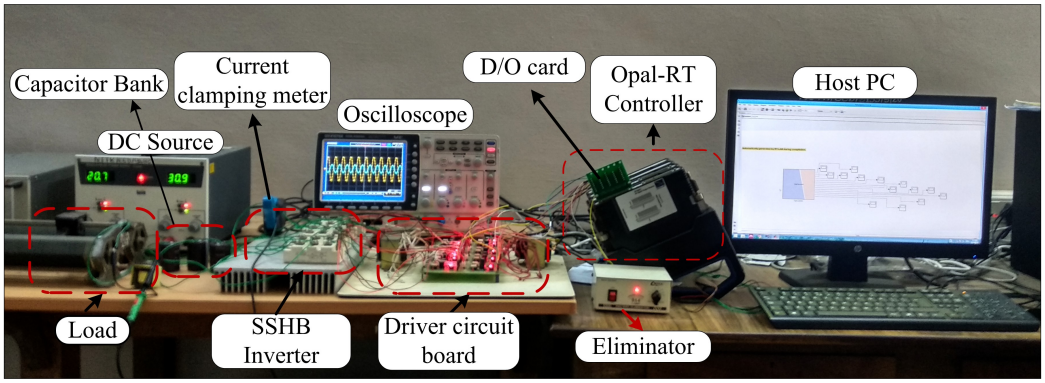


Figure 3.10: Laboratory set-up of SSHB

1.208 mF, 1.140 mF, and 1.085 mF, respectively. A detailed capacitance calculation is included in Appendix A. The rationale behind selecting a 16% ripple is to use the 1.2 mF capacitors, which are available readily in the laboratory. The real-time simulator OP4200 is used as a controller to feed the gating pulses to the semiconductors. A complete description of the simulator and laboratory setup is discussed in Appendix D. Output waveforms, capacitor voltages at different loading, modulation conditions are depicted in Figure 3.8. The steady-state waveforms at $m_a = 1$ is shown in Figure 3.8(a). Voltage of capacitor C_1 is balanced at a peak of 50 V and capacitors C_2, C_3 at 97.5 V each. The achieved peak output voltage is nearly equal to 300 V (neglecting voltage drop), with 13 different levels between -300 V to +300 V. The fundamental RMS values of load current, voltages are 4.03 A and 203 V, respectively.

Experiments are continued to examine the prototype's dynamic responses for load transients in Figure 3.8(b), (c). Figure 3.8(b) shows the sudden increment in load from 50 Ω to 100 Ω - 40 mH. Figure 3.8(c) shows the step increment in load from 50 Ω - 20 mH to 100 Ω - 40 mH. It is perceived from the figures that the output voltages, currents, and capacitors' voltages are at their expected values. Ripple in capacitor voltages has reduced due to the increased time constant of the discharging loop. The same effect is observed on the capacitor voltages due to a step increment in load impedance. The speedy response in load current, capacitor voltages are perceived. Irrespective of the transients in load, it is seen that no deterioration is noticed in the capacitor and output voltages. Meantime, all capacitors continued to maintain their reference values with an agreeable ripple. The fundamental, other components of the output voltage and current from the FFT spectrum for PD-PWM are captured in Figure 3.9(a), (b). The odd harmonics are greatly suppressed, and a THD of 8.71

% for voltage and 1.96% for current is recorded. It is observed that the dominant harmonics are slipped to 39^{th} & 41^{st} order at 2 kHz switching frequency.

Conduction and switching loss equations are derived from the curve fitting approach for the 13-level inverter. The curve fitting approach has high accuracy and can be planted directly in any circuit simulator. These loss calculations are based on switch data-sheet values and experimental measurements. The MLI developed in the above section is built with the SKM75GB123D IGBT module. Therefore the SKM75GB123D data-sheet information is considered for further explanation. An actual procedure presented in (Drofenik and Kolar, 2005) is followed, and complete derivation of loss calculation and capacitor ripple losses are described in Appendix C. The derived transistor (P_{igbt}) and anti-parallel diode (P_D) conduction loss equations from the curve-fitting method at temperatures 25°C, and 125°C (minimum and maximum) are

$$P_{igbt,25°C} = 0.02365 \times i_c^2 + 1.551 \times i_c - 0.8995 \tag{3.3}$$

$$P_{D,25°C} = 0.0153 \times i_f^2 + 1.245 \times i_f - 0.2321 \tag{3.4}$$

$$P_{igbt,125°C} = 0.02876 \times i_c^2 + 1.914 \times i_c - 2.452 \tag{3.5}$$

$$P_{D,125°C} = 0.01485 \times i_f^2 + 1.06 \times i_f - 0.8451 \tag{3.6}$$

Here, i_c is the transistor collector current, i_f is the diode forward current. As the temperature (T) is one of the influencing factors; the modified conduction loss equations of transistor ($P_{igbt}(i_c, T)$), diode ($P_D(i_f, T)$) with temperature coefficients based on I-V curves can be expressed as follows

$$\begin{aligned} P_{igbt}(i_c, T) = {} & (0.0224 + 0.000058 \times T)i_c^2 + (1.46025 + 0.00363 \times T)i_c \\ & - (0.511375 + 0.015525 \times T) \end{aligned} \tag{3.7}$$

$$\begin{aligned} P_D(i_f, T) = {} & (0.0153 \times T)i_f^2 + (1.2913 - 0.0019 \times T)i_f \\ & - (0.0789 + 0.0061 \times T) \end{aligned} \tag{3.8}$$

A pulse train of the device and the current flowing through it are the inputs to calculate the switching loss of the semiconductor. The switching loss factor of the transistor ($K_{IGBT}(i_C)$) or diode ($K_D(i_f)$) at a given temperature is related to the total energy loss (E_{total}) and the current flow through it. The expression for $K_{IGBT}(i_C)$ and

$K_D(i_f)$ can be represented as

$$K_{IGBT}(i_C) = 0.0001487 \times i_c^3 - 0.03366 \times i_c^2 + 3.224 \times i_c + 170.3 \quad (3.9)$$

$$K_D(i_f) = -0.00077266 \times i_f^2 - 0.0436 \times i_f + 65.53 \quad (3.10)$$

From the derived loss equations, achieved efficiency at a load of 888.63 W is 95.20%. While the total calculated loss is 42.71 W (conduction loss = 29.50 W, switching loss = 1.19078 W, and capacitor loss = 11.055 W). Individual conduction, switching losses for each switch is added in Tables 3.4, 3.5.

Table 3.4: Power loss distribution (in Watts) at 25℃

Switch	Conduction loss	Switching loss	Switch	Conduction loss	Switching loss
S_1	1.0689	0.0013404	S_5	1.0746	0.001269
$\bar{S_1}$	1.0746	0.0001059	S_6	2.4494	0.0001059
S_2	1.0689	0.0098275	S_7	1.0378	0.0010097
$\bar{S_2}$	0.9666	0.000551	S_8	1.0378	0.0010097
S_3	1.0666	0.05142	S_9	2.8224	0.039699
$\bar{S_3}$	3.884	0.05145	S_{10}	1.3583	0.009482
S_4	1.0666	0.000551	S_{11}	2.8224	0.0020199

Table 3.5: Power loss distribution (in Watts) at 125℃

Switch	Conduction loss	Switching loss	Switch	Conduction loss	Switching loss
S_1	2.143	0.0013404	S_5	2.1459	0.001269
$\bar{S_1}$	2.1459	0.0001059	S_6	4.4514	0.0001059
S_2	2.143	0.0013404	S_7	2.073	0.0010093
$\bar{S_2}$	2.143	0.0013404	S_8	2.073	0.0010093
S_3	2.1071	0.05517	S_9	2.4347	0.0039699
$\bar{S_3}$	1.4335	0.0598275	S_{10}	3.0514	0.009482
S_4	1.4335	.0098275	S_{11}	3.1434	0.0020199

3.6 Comparative analysis

A quantitative and cost comparison is conducted among newly recommended single dc-source SC-based inverters. Active and passive part count and their ratings are the foremost challenges for MLIs. A quantitative comparison is carried by considering blocking voltage, required SCs, and semiconductors for SC-MLIs in Table 3.6. As shown in Table 3.6, the proposed SSHB circuit requires the least number of switches. Though the topology in (Ye et al., 2014) needs fewer switches than the proposed topology, the former requires a high number of diodes. At the same time, the proposed topology needs only one diode. Capacitors being the second vulnerable component, it is desirable to restrict their number in the converter. Thus, the number of capacitors qualifies as one of the prominent MLI measures of competency merits. The proposed topology requires only three switched capacitors (least among all the topologies under consideration). Thus the size and therefore cost of the proposed topology is less.

Besides, it is essential to evaluate the blocking voltage and H-bridge stress as it reflects the heat-sink requirement and a converter's cost. The proposed circuit is found to present a low value of PIV in comparison to other topologies except (Liu et al., 2018a), (Sandeep et al., 2018), and (Taghvaie et al., 2018). Topologies (Liu et al., 2018a), (Sandeep et al., 2018), and (Taghvaie et al., 2018) have the lowest blocking voltage among all the circuits under consideration but at the cost of a considerable component count. Moreover, the H-bridge switches in (Hinago and Koizumi, 2012), (Ye et al., 2014), (Barzegarkhoo et al., 2016), and (Babaei and Gowgani, 2013) have to endure a peak of the output voltage, whereas the proposed circuit does not require an H-bridge at the back end to generate polarity. Therefore, less part count, blocking voltage, and high boost gain indicate that the proposed converter is best suited for an expanded area of applications than the SC-MLIs listed in Table 3.6.

Cost analysis is conducted to ratify the economic benefits of the proposed SSHB inverter. A sample case of 900 W, with 300 V voltage, is considered, and the resulted prices of the compared topologies are enlisted in Table 3.7. The generic rating, cost of the components are considered. It is evident from Table 3.7 that the proposed topology costs the least compared to the prior topologies. In brief, the price of the proposed circuit is economical and performing well compared to other converters.

Table 3.6: Quantitative comparison of the proposed configuration with recently developed topologies

Parameter	Topology							
	1	2	3	4	5	6	7	SSHB
N_{sw}	$\left(\frac{3N_l-1}{2}\right)$	$\left(\frac{N_l+7}{2}\right)$	$\left(\frac{3N_l-1}{2}\right)$	$\left(\frac{5N_l+1}{4}\right)$	$\left(\frac{5N_l-7}{2}\right)$	$\left(\frac{5N_l-7}{2}\right)$	(N_l+1)	(N_l+1)
N_{cap}	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l+5}{4}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-1}{4}\right)$
N_{diode}	-	(N_l-3)	-	$\left(\frac{N_l-3}{2}\right)$	-	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	1
$PIV * V_{dc}$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	2	1	1	$\left(\frac{N_l-1}{2}\right)$	4
H-Bridge stress (V_{dc})	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	-	-	-	$\left(\frac{N_l-1}{2}\right)$	-
Voltage gain	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{4}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$

N_{sw} - No. of active switches, N_{cap} - No. of capacitors, N_{diode} - No. of diodes, PIV - Peak Inverse Voltage

1. Hinago and Koizumi (2012)
2. Ye et al. (2014)
3. Barzegarkhoo et al. (2016)
4. Liu et al. (2018a)
5. Sandeep et al. (2018)
6. Taghvaie et al. (2018)
7. Babaei and Gowgani (2013)

Table 3.7: Cost comparison of proposed SSHB MLI with other SC based topologies for 13-levels

Component	Series	Rating	Unit price	Topology							
			($)	1	2	3	4	5	6	7	SSHB
MOSFET	STP45N60DM6	600 V	6.13	4	4	4	-	-	-	4	-
	IRFP350PBF	400 V	2.98	-	-	-	-	-	-	-	4
	IRFP240PBF	200 V	2.31	-	-	-	5	-	-	-	8
	IRFP9140NPBF	100 V	1.89	15	6	15	28	29	29	10	2
Gate driver	IR2110SPBF	-	1.92	19	10	19	33	29	29	14	14
Capacitor	B41231A9128M	1.2 mF	1.51	5	5	5	5	5	5	5	3
Diode	SDT10A100P5	100 V	0.61	-	10	-	5	-	5	5	1
Total price ($)				97.02	71.27	96.9	138.3	110.5	121.1	80.9	66.2

Courtesy: mouser.com, in.element14.com, www.digikey.com, www.mouser.com; *prices are subject to change

1. Hinago and Koizumi (2012)
2. Ye et al. (2014)
3. Barzegarkhoo et al. (2016)
4. Liu et al. (2018a)
5. Sandeep et al. (2018)
6. Taghvaie et al. (2018)
7. Babaei and Gowgani (2013)

Chapter 4

HYBRID MULTILEVEL INVERTERS

4.1 Introduction

A 13-level SSHB inverter is developed with the use of SCs in the previous chapter. Unlike SSHB-MLI, an attempt is made to hybridize the topology by incorporating FC with SCs in one inverter circuit. The difference between FC and SC is the difference between the time constants of the charging and discharging loops. The time constant of the FC is the same for the charging and discharging loop. In contrast, the time constant of the SC is different for the charging and discharging loop. The time constant of the discharging loop is much higher than the charging loop in SC. Another difference between the FC and SC is charging with different magnitudes of voltages. Depending on the number of levels and capacitors, FC is charged with $1V_{dc}$, $0.5V_{dc}$, $0.25V_{dc}$, $0.125V_{dc}$.... However, SC is charged with the fixed voltage magnitude. Herein, FC is used to double the voltage levels, and SCs are utilized to boost the voltage magnitude as well as levels. Two novel hybrid MLI circuits, namely BH-MLI, HNIT are presented in this chapter. The proposed converters constitute the following notable features

1. Requires less number of components
2. Output voltage boosting ability
3. Capacitors with self-voltage balancing capability

4. Capacitors' voltages are independent of modulation index and power factor

5. Produces zero and bipolar levels without an additional H-bridge.

This chapter is composed in the following way: firstly, the proposed BH-MLI circuit's description and operating principle are presented. Secondly, another version of the hybrid topology, HNIT, is discussed. Further, the experimental results of both circuits at different loading conditions are provided, followed by a detailed quantitative and cost evaluation.

4.2 BH-MLI structure

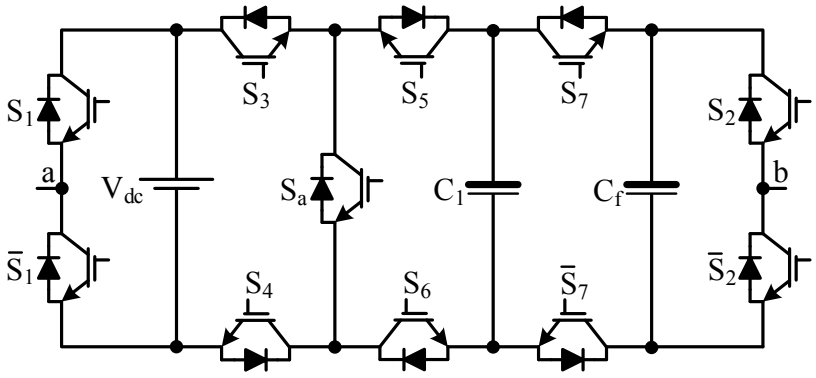


Figure 4.1: BH-MLI circuit

The devised BH-MLI structure with a single DC source arrangement is shown in Figure 4.1. It produces nine distinct voltage levels ($\pm 2V_{dc}$, $\pm 3V_{dc}/2$, $\pm V_{dc}$, $\pm V_{dc}/2$, 0) with a voltage gain of two. Structurally, this configuration contains three pair of complementary switches (S_1 - $\bar{S_1}$, S_2 - $\bar{S_2}$, S_7 - $\bar{S_7}$) and five individual switches (S_3 - S_6 and S_a), one SC (C_1) and one FC (C_f). The complementary nature of the circuit productively lessens the pulse generating logic gates and driver circuits. Herein, the switches S_1, S_3, S_4, S_5, S_6 and S_a have to withstand the input supply (V_{dc}) as a maximum blocking voltage, likewise half of the input supply ($0.5V_{dc}$) is the blocking voltage of the remaining switches S_2 and S_7. The capacitors C_1 and C_f are rated at V_{dc} and $0.5V_{dc}$ respectively. The capacitor C_1 has inherent self voltage balance ability since it is charged/discharged using a series-parallel approach. Therefore it does not require any voltage balancing algorithm. Unlike C_1, capacitor C_f is charged in a positive half cycle and discharged in a negative half cycle of the output voltage

waveform. Determining the capacitance plays a major role in the overall size of the converter. The procedure to calculate capacitance by considering the maximum discharging period, ripple voltage, and frequency is given in Appendix A. A detailed derivation validating the natural balancing of FC is included in Appendix B. As a result of self-voltage balancing, a sensor-less controlling technique can be employed to generate N_l levels. Structurally, switching devices have minimum voltage stresses; therefore, the individual rating of the switching component is significantly lesser than the other SC-based configurations. As a result, the efficacy of the proposed inverter is improved.

4.2.1 Operating modes of BH-MLI

Table 4.1: Switching and capacitor states of the BH-MLI

$V_o = V_{ab}$	Switch								Capacitor state	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_a	C_1	C_f
$2V_{dc}$	1	0	0	1	1	0	0	1	D	-
$\frac{3V_{dc}}{2}$	1	1	0	1	1	0	0	1	D	C
V_{dc}	1	0	1	1	1	1	0	0	C	-
$\frac{V_{dc}}{2}$	1	1	1	1	1	1	0	0	C	C
0	1	1	1	0	1	0	1	0	-	-
	0	0	0	1	0	1	0	0	-	-
$-\frac{V_{dc}}{2}$	0	1	0	1	0	1	0	0	-	D
$-V_{dc}$	0	1	1	1	1	1	0	0	C	-
$-\frac{3V_{dc}}{2}$	0	1	1	0	0	1	0	1	-	D
$-2V_{dc}$	0	1	1	0	0	1	1	1	D	-

(0 - OFF, 1 - ON, D - Discharge, C - Charge, - - No effect)

Output voltage levels of the proposed BH-MLI are generated by adding voltages across capacitors. The switching combinations for the respective voltage levels are listed in Table 4.1. A detailed operating modes are pictorially represented in Figure 4.2 with current paths of each level and active switches. Operating modes for a fundamental cycle are explained as follows:

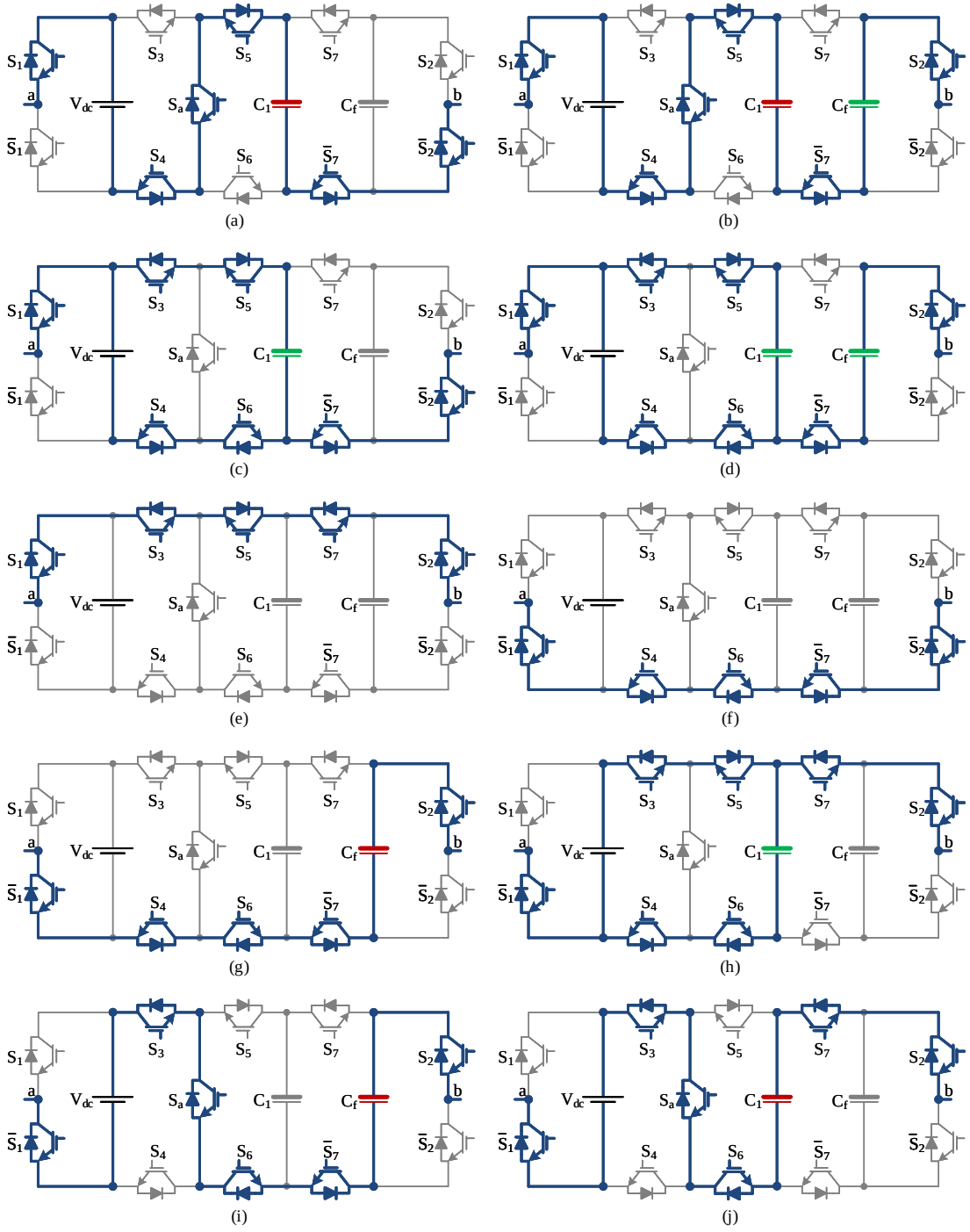


Figure 4.2: Switching states of BH-MLI structure: (a) $2V_{dc}$, (b) $3V_{dc}/2$, (c) V_{dc}, (d) $V_{dc}/2$, (e) 0, (f) 0, (g) $-V_{dc}/2$, (h) $-V_{dc}$, (i) $-3V_{dc}/2$, (j) $-2V_{dc}$.

- $\pm 2V_{dc}$ - Mode: Switches S_1, $\bar{S_2}$, S_4, S_5, $\bar{S_7}$ and S_a are ON, resulting in the voltage across the output is $V_{ab} = 2V_{dc}$ as shown in 4.2(a). At the same time, for the $-2V_{dc}$ state as portrayed in 4.2(j), switches $\bar{S_1}$, S_2, S_3, S_6, S_7 and S_a are turned ON. In both cases, capacitor C_1 get discharged and C_f remains unaffected.

- $\pm 3V_{dc}/2$ - Mode: Switches S_1, S_2, S_4, S_5, $\bar{S_7}$ and S_a are ON, resulting in a voltage of $3V_{dc}/2$ across the output terminal as shown in 4.2(b). Thereby, capacitor C_1 starts to discharge whereas C_f get charged. For the $-3V_{dc}/2$ state as shown in 4.2(i), switches $\bar{S_1}$, S_2, S_3, S_6, $\bar{S_7}$ and S_a are turned ON. Thereby, capacitor C_1 remains unaffected and C_f get discharged.

- $\pm V_{dc}$ - Mode: Switches S_1, $\bar{S_2}$, S_3, S_4, S_5, S_6 and $\bar{S_7}$ are ON, resulting in a voltage of V_{dc} across the output terminal and it is portrayed in 4.2(c). For the $-V_{dc}$ state, switches S_1, $\bar{S_2}$ and $\bar{S_7}$ are OFF as shown in 4.2(h). In both cases, capacitor C_1 get charged and C_f is unaffected.

- $\pm V_{dc}/2$ - Mode: Switches S_1, S_2, S_3, S_4, S_5, S_6, and $\bar{S_7}$ are ON, resulting in a voltage of $V_{dc}/2$ across the output terminal in which both capacitors get charged as shown in 4.2(d). At the same time, for the $-V_{dc}/2$ state, switches S_1, S_3 and S_5 are OFF in which C_f get discharged as shown in 4.2(g).

- Zero - Mode: Two possible switching modes are exist as portrayed in 4.2(e), (f). S_1, S_2, S_3, S_5, and S_7 or $\bar{S_1}$, $\bar{S_2}$, S_4, S_6, and $\bar{S_7}$ are ON. In both combinations terminals a and b are short circuited, resulting in the voltage across the output in both cases is $V_{ab} = 0$. In both cases, capacitors are unaffected.

4.3 Modulation technique

The proposed topology is evaluated with the well-known controlling approach, phase disposition-pulse width modulation (PD-PWM), to generate the gating pulses. For PD-PWM switching technique, peak-to-peak voltage magnitude of the carrier is calculated as follows

$$\alpha_n = (V_{Car} + U(n-1)) \times V_m; \;\; n = 1, 2, 3..., \frac{N_l - 1}{2} \tag{4.1}$$

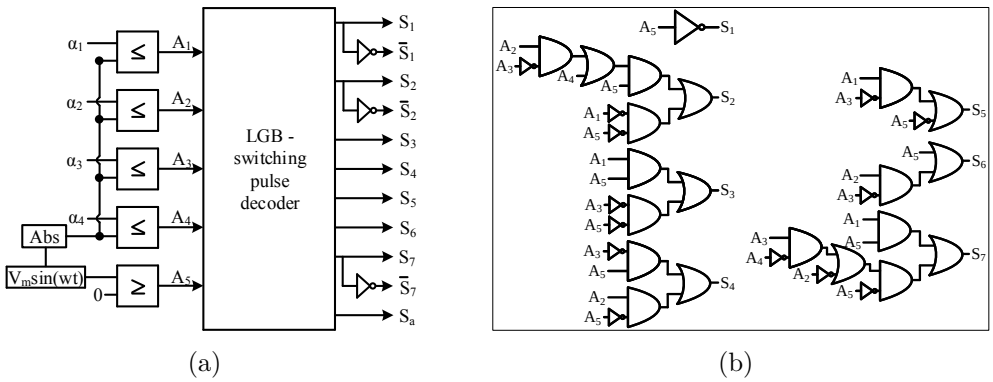


Figure 4.3: PWM signal generation scheme: (a) Switching scheme for nine-level generation, (b) LGB switching pulse decoder.

Where V_{Car} is the triangular carrier waveform with a peak-peak magnitude of U. N_l, V_m are the number of output voltage levels and peak magnitude of reference wave respectively. Amplitude modulation index, m_a, is given by

$$m_a = \frac{V_m}{\left(\frac{N_l - 1}{2}\right) \times \widehat{V}_{Car}} \tag{4.2}$$

here $\widehat{V}_{Car}$ is peak amplitude of the carrier signal. Further, other carrier signals (ramp, trapezoidal, absolute-sinusoidal, etc) are also equally applicable.

The rectified sinusoid voltage ($V_{ref} = |V_m \sin(\omega t)|$) is used as a reference in the switching technique. This reference wave is compared with each of the carrier waveforms, and the information regarding the voltage levels is constructed from these comparator outputs by applying suitable logic operation as portrayed in Figure 4.3(a). Wherein A_1, A_2, A_3, and A_4 are the binary interpretation corresponding to the voltage step to be generated. These comparator outputs are fed to the LGB switching decoder, which is shown in Figure 4.3(b). At a given instance, either of the four variables is '1'. Owing to the rectified nature of the reference sinusoidal waveforms, one needs to know the half-cycle change. Therefore, a cycle separation/identification unit is incorporated, which is designated as A_5. The output voltage levels correspond to positive values and negative values if $A_5 = 1$ and $A_5 = 0$, respectively. The gating pulses of each switch are derived using the switching combination depending on the capacitor state, and the corresponding combination is applied. Thus, instantaneous voltage control of FC is possible within the fundamental cycle. By using boolean

functions, each switching equation is formulated as follows

$$S_1 = \bar{A_5} \tag{4.3}$$

$$S_2 = [(A_2 \cdot \bar{A_3}) + A_4] \cdot A_5 + \bar{A_1} \cdot \bar{A_5} \tag{4.4}$$

$$S_3 = A_1 \cdot A_5 + \bar{A_3} \cdot \bar{A_5} \tag{4.5}$$

$$S_4 = \bar{A_3} \cdot A_5 + A_2 \cdot \bar{A_5} \tag{4.6}$$

$$S_5 = (A_1 \cdot \bar{A_3}) + \bar{A_5} \tag{4.7}$$

$$S_6 = A_5 + (A_2 \cdot \bar{A_3}) \tag{4.8}$$

$$S_7 = A_1 \cdot A_5 + [\bar{A_2} + (A_3 \cdot \bar{A_4})] \cdot \bar{A_5} \tag{4.9}$$

$$S_a = A_3 \tag{4.10}$$

It is worth mentioning that the developed procedure is independent of the modulation technique. Thus, it can be used for either carrier-based or non-carrier ones.

4.4 Recommended extensions of BH-MLI

The proposed topology can be extended to higher levels (>9) with a minimum device count. The recommended extension circuits are presented as follows

4.4.1 Structure - 1

In this method, SCCs are added in a cascade manner, as depicted in Figure 4.4. The voltage levels are dependent on the number of SCCs connected. The proposed extension for higher levels resembles the extension of (Sandeep et al., 2018), but the contrary is requirement of active and passive components. The topology in (Sandeep et al., 2018) requires $\left(\frac{5N_l-7}{2}\right)$ switches, $\left(\frac{N_l-3}{2}\right)$ capacitors to generate N_l level output voltage. Herein, proposed topology requires $\left(\frac{5N_l-1}{4}\right)$ switches, $\left(\frac{N_l-1}{4}\right)$ switched capacitors, which are less compared to the extension (Sandeep et al., 2018). A boost gain of $\left(\frac{N_l-1}{4}\right)V_{dc}$ is achieved with proposed extension. The peak magnitude of the output voltage is related to the number of capacitors, N_{cap} as

$$V_{o,peak} = N_{cap} \times V_{dc}$$

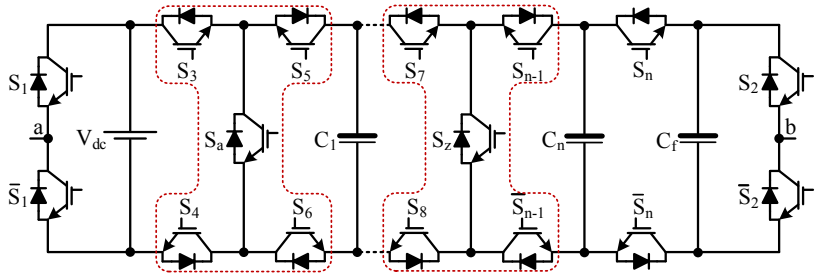


Figure 4.4: Extension structure - 1

4.4.2 Structure - 2

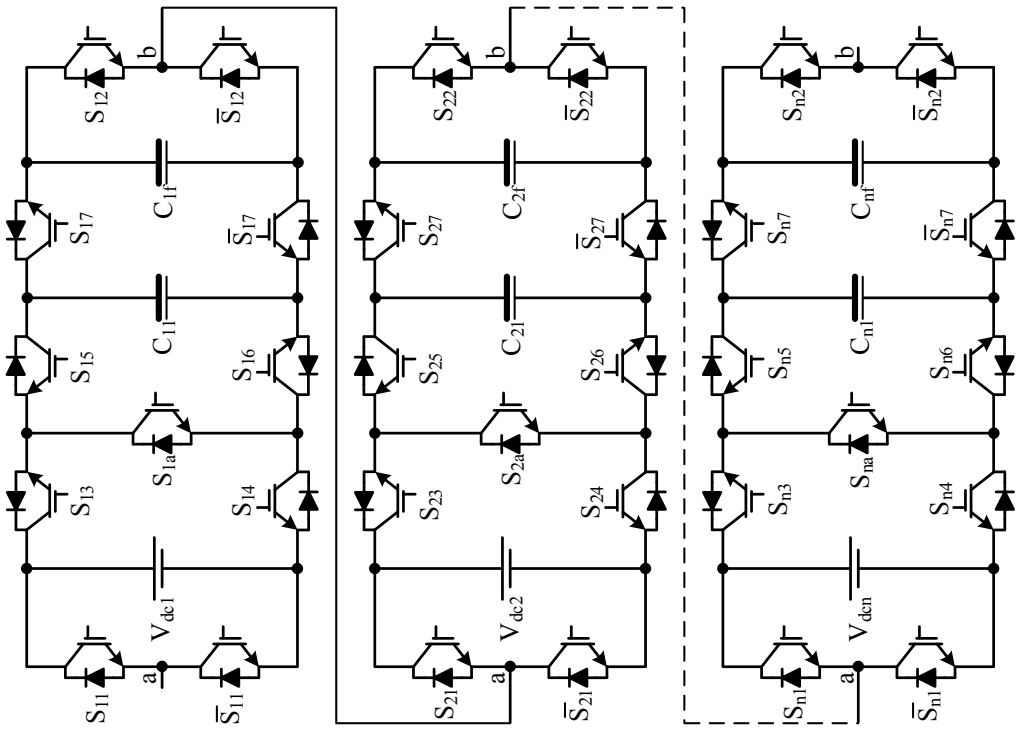


Figure 4.5: Extension structure - 2

This structure facilitates to integrate multiple sources by considering the proposed BH-MLI topology as a fundamental block, and these units are cascaded as portrayed in Figure 4.5. The voltages across the multiple dc-links are designated as V_{dc_1}, V_{dc_2},..., V_{dc_n}. The total output voltage between terminals *a*-*b* is the sum of individual proposed MLI outputs and expressed as,

$$V_{ab} = V_1 + V_2 + ... + V_n \tag{4.11}$$

Based on the dc-link voltage magnitude ratio of each cascaded subsystem, the BH-MLI can operate in three modes:

- The total dc-link voltage ratio of each cascaded unit is equal (symmetry) to one in this mode. In other words $V_{dc_1} = V_{dc_2}$ ... $= V_{dc_n} = V_{dc}$. To produce N_l levels at output, $11\left(\frac{N_l-1}{8}\right)$ switches, $\left(\frac{N_l-1}{4}\right)$ capacitors, and $\left(\frac{N_l-1}{8}\right)$ sources are required. The peak magnitude of output voltage is related to the fundamental blocks, n as

$$V_{o,peak} = 2n \times V_{dc}; \qquad n = 1, 2, 3...$$

- In this mode, total dc-link voltage ratio of each cascaded unit differs in the order of binary. In other words, $V_{dc_1} = 2^0 \times V_{dc}$, $V_{dc_2} = 2^1 \times V_{dc}$,..., $V_{dc_n} = 2^{n-1} \times V_{dc}$. To produce N_l levels at output, $11 \log_2\left(\frac{N_l+7}{8}\right)$ switches, $2 \log_2\left(\frac{N_l+7}{8}\right)$ capacitors, and $\log_2\left(\frac{N_l+7}{8}\right)$ sources are required. The peak magnitude of output voltage is related to the fundamental blocks, n as

$$V_{o,peak} = (2^{n+1} - 2) \times V_{dc}$$

- The total dc-link voltage ratio of each cascaded unit differs in the order of ternary. In other words, $V_{dc_1} = 3^0 \times V_{dc}$, $V_{dc_2} = 3^1 \times V_{dc}$,..., $V_{dc_n} = 3^{n-1} \times V_{dc}$. To produce N_l levels at the output, $11 \log_3\left(\frac{N_l+3}{4}\right)$ switches, and $2 \log_3\left(\frac{N_l+3}{4}\right)$ capacitors, and $\log_3\left(\frac{N_l+3}{4}\right)$ sources are required. The peak magnitude of output voltage can be related to the fundamental blocks, n as

$$V_{o,peak} = (3^n - 1) \times V_{dc}$$

4.5 Experimental results

A prototype is built and tested in the laboratory at different load conditions to investigate the performance of the proposed BH-MLI. The attributes required for the setup are tabulated in Table 4.2. The capacitance of C_1, C_f are considered as 1.2 mF and a passive load of 30 Ω - 20 mH are chosen. Output voltages at different modulation indices are depicted in Figure 4.6(a)-(d). When the modulation index, m_a is tuned between $0 < m_a \leq 0.25$, the generated output voltage levels are three with the voltage amplitude of 25 V. During $0.25 < m_a \leq 0.5$, the output levels are

changed from three to five. The magnitude of the output voltage is 50 V at $m_a = 0.5$. During $0.5 < m_a \leq 0.75$, the output levels are changed from five to seven. The magnitude of the output voltage is 75 V at $m_a = 0.75$. Similarly, when $m_a > 0.75$, the generated output voltage levels are nine with a magnitude of 100 V. The proposed circuit, therefore, can produce a different number of output levels stably under the different modulation indices.

The steady-state capacitor voltages, load voltage and currents at 30 Ω - 20 mH load are represented in Figure 4.7(a). To demonstrate the self-voltage balancing of involved capacitors C_1 and C_f, the experimental voltage waveforms are shown in Figure 4.7(a). The capacitor C_1 is balanced to the magnitude of source voltage (V_{dc}) and C_f is settled at half of the source voltage magnitude. Load current waveform is sinusoidal with 2.28 A (RMS) and lagging behind the output voltage with an angle of 11.82° since the load is (30 + j6.28) Ω. It is obvious that the output voltage waveforms are comprised of nine levels with a magnitude of 100 volts, proving the boost gain and inductive load ability.

Table 4.2: Attributes for hardware set-up

Parameters	Value
dc-link voltage	50 V
Fundamental output frequency	50 Hz
Capacitance of capacitors (C_1, C_f)	1.2 mF, 1.2 mF
Switching frequency (f_{sw})	2 kHz
Load resistance and inductance	30 Ω - 20 mH; 60 Ω - 40 mH & 30 Ω

Further, a step-change in load from 30 Ω - 20 mH to 60 Ω - 40 mH and dynamic change in power factor from 30 Ω to 30 Ω - 40 mH are applied to study the performance, smooth level generation of the inverter. Capacitor, load voltages and currents at these load conditions represented in Figure 4.7(b), (c). The transient response of the load from no-load to full-load is shown in Figure 4.7(d). When the load is connected, the current reaches its reference immediately without affecting the capacitors' and output voltages. Also, a step-change in the dc-link is applied to confirm the capacitors' voltage balancing capability of the BH-MLI circuit. This experiment is executed by using a two-channel DC power supply (TD3202M). Figure 4.7(e) shows

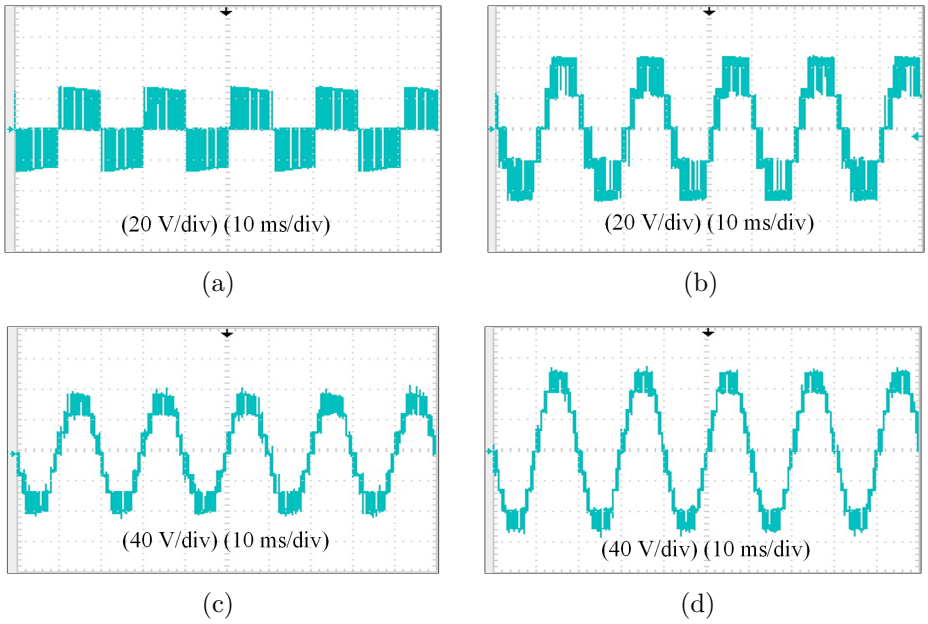


Figure 4.6: Output voltage at (a) $m_a = 0.25$, (b) $m_a = 0.50$, (c) $m_a = 0.75$, (d) $m_a = 1.0$.

the test results of the circuit topology to a step-change in the source voltage from 30 V to 50 V. Output voltage is reached to its reference peak in 0.02 sec, keeping the symmetry of the ac output waveforms. Figure 4.7(f) shows the capacitors C_1, C_f currents (i_{C_1}, i_{C_f}) at step-change in the source voltage from 30 V to 50 V. Output voltage is reached to its reference peak in 0.02 sec, keeping the symmetry of the ac output waveforms. The stable generation of the output voltage levels under all loading conditions has been observed. It can be seen that during all the operating conditions, the proposed BH-MLI has maintained the capacitors' voltages at their reference value. The laboratory tests, therefore, have a good agreement and confirming the viability of the proposed topology.

The harmonic profile of the load voltage waveform always depends on the m_a, since when m_a falls from high to low, the output levels of the inverter drops, which degrades the quality of the stepped waveform. Voltage THD of the nine-level BH-MLI is recorded as 13.51% with the PD-PWM technique at unity modulation index. Harmonic profile of the load voltage, current waveforms at $m_a = 1$ are portrayed in Figure 4.8(a), (b). All lower order harmonics are diminished, and the predominant harmonics are moved to 39^{th} and 41^{st} order with PD-PWM technique since the carrier

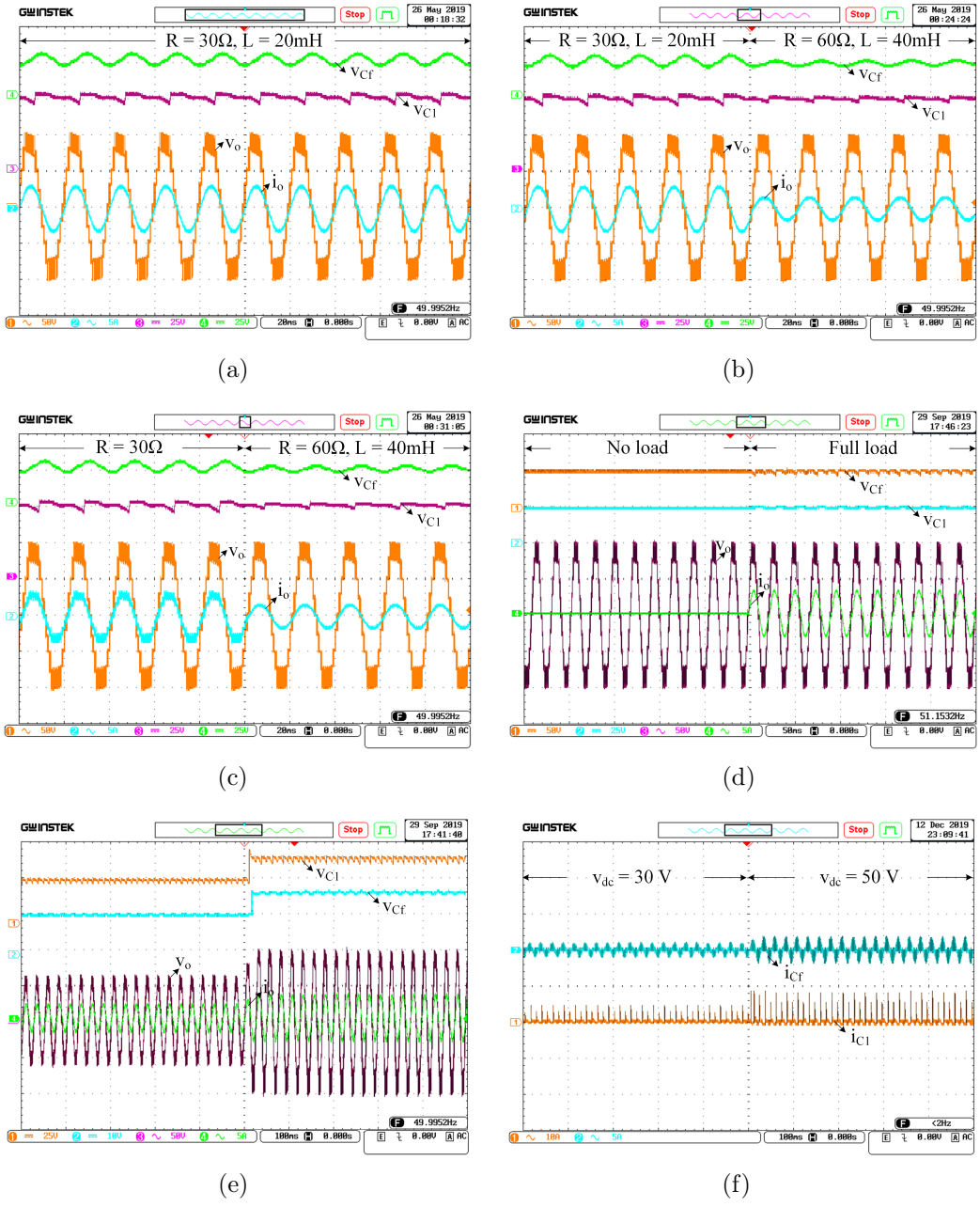
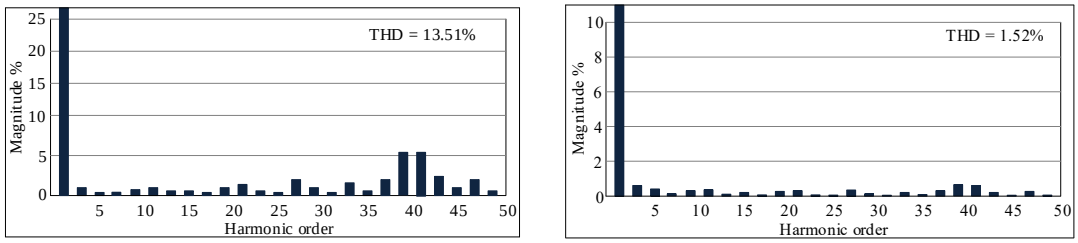


Figure 4.7: Experimental results of BH-MLI: (a) 30 Ω - 20 mH load, (b) a step change in load from 30 Ω - 20 mH to 60 Ω - 40 mH, (c) a dynamic change in power factor from 30 Ω to 60 Ω - 40 mH, (d) a dynamic change in load from no-load to full-load, (e) a step increment in source voltage from 30 V to 50 V, (f) capacitor currents at a step increment in source voltage from 30 V to 50 V.



(a) (b)

Figure 4.8: Harmonic profile with PD-PWM technique: (a) load voltage, (b) load current at (30 + j6.28) Ω.

frequency is considered as 2 kHz.

4.6 HNIT structure

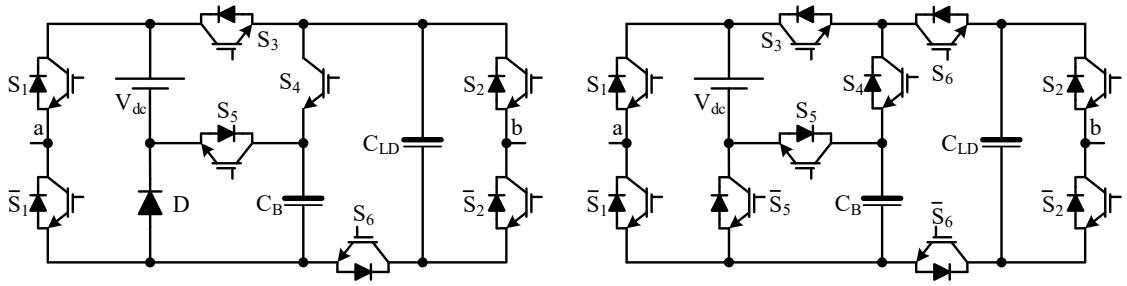


Figure 4.9: Circuit arrangement of the proposed HNIT module for (a) resistive load, (b) inductive load.

Figure 4.9 shows the proposed HNIT arrangements with a single DC source. Here, capacitor C_B is employed to boost the output voltage, and C_{LD} is utilized to double the output levels. Lack of return path for reverse current flow, topology in Figure 4.9(a) operates only for the power factors above 0.938. Because of this limitation, the circuit in Figure 4.9(a) is restricted to resistive load applications. A modified topology with a full range of pf is portrayed in Figure 4.9(b). This modification needs only two extra semiconductor switches than the prior. The circuit in Figure 4.9(b) is chosen to explain the operating principle of the HNIT. The proposed HNIT offers nine discrete voltage levels ($\pm 2V_{dc}$, $\pm 1.5V_{dc}$, $\pm 1V_{dc}$, $\pm 0.5V_{dc}$, and 0) and only two switches have to withstand a maximum voltage of $2V_{dc}$. The capacitors C_B, C_{LD} are

charged to V_{dc}, $0.5V_{dc}$ respectively. Since C_B is charged and discharged applying a series-parallel method, it does not need a supplementary voltage balance technique. Unlike C_B, capacitor C_{LD} is discharged in a positive half-cycle and charged in a negative half-cycle of the output voltage waveform. Therefore, a sensor-less control technique is employed to produce output voltage levels.

4.7 Generation of output voltage levels

Table 4.3: Switching table for the HNIT

$V_o = V_{ab}$	Switch						Capacitor state	
	S_1	S_2	S_3	S_4	S_5	S_6	C_B	C_{LD}
$2V_{dc}$	1	0	0	0	1	1	D	-
$1.5V_{dc}$	1	0	0	1	1	0	-	D
$1V_{dc}$	1	0	0	0	0	1	-	-
$0.5V_{dc}$	1	0	1	1	0	0	C	D
0	1	1	1	0	0	0	-	-
0	0	0	0	0	0	1	-	-
$-0.5V_{dc}$	0	0	1	1	0	0	C	C
$-1V_{dc}$	0	1	1	1	0	0	C	-
$-1.5V_{dc}$	0	0	1	0	1	0	D	C
$-2V_{dc}$	0	1	1	0	1	0	D	-

(1 - ON, 0 - OFF, D - Discharge - - No effect, C - Charge)

Complete Switching modes associated capacitor charge and discharge states of the proposed HNIT converter are enlisted in Table 4.3. Here, the entries "1" and "0" indicates ON and OFF state of respective switch. "D", "C", and "—" indicate discharging, charging, and no-effect states of a capacitor, respectively. Detailed operating modes with current paths are portrayed in Figure 4.10(a)-(j). Generation of positive output voltage levels as follows:

- $2V_{dc}$ mode: The required voltage to the load terminal is provided through input source of $1V_{dc}$ magnitude and voltage in C_B by turning S_1, $\bar{S_2}$, S_5, and $\bar{S_6}$ ON.

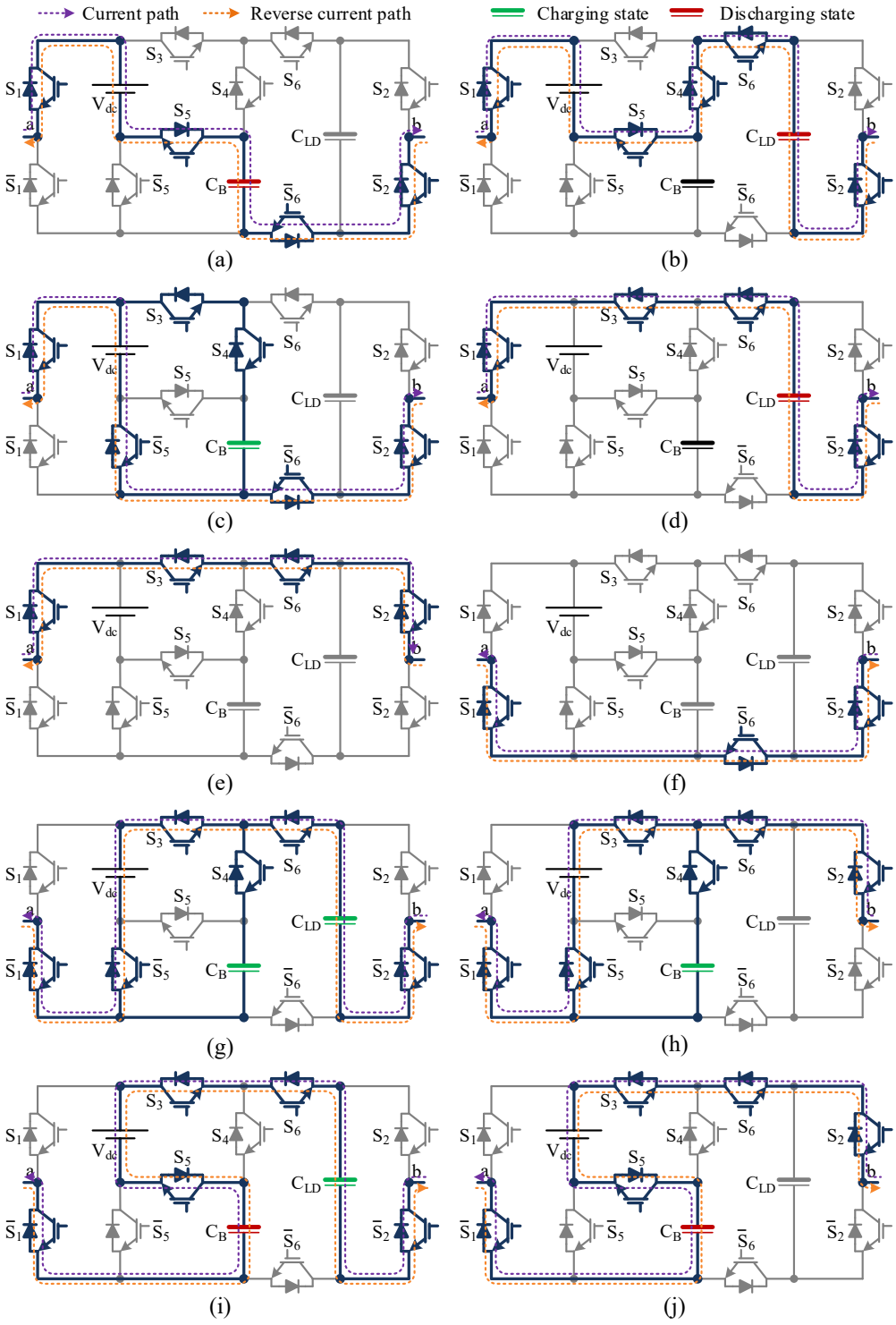


Figure 4.10: Switching states of HNIT structure: (a) $2V_{dc}$, (b) $1.5V_{dc}$, (c) $1V_{dc}$, (d) $0.5V_{dc}$, (e) $0V_{dc}$, (f) $0V_{dc}$, (g) $-0.5V_{dc}$, (h) $-1V_{dc}$, (i) $-1.5V_{dc}$, (j) $-2V_{dc}$.

- $1.5V_{dc}$ mode: The required voltage to the load terminal is supplied by input supply of $1V_{dc}$ and voltage in C_{LD} by turning S_1, $\bar{S_2}$, S_4, S_5, and S_6 ON. The voltage employed to the load terminal is $1V_{dc} + 0.5V_{dc}$.

- $1V_{dc}$ mode: The required voltage to the load terminal is supplied by input dc supply magnitude of $1V_{dc}$ by turning S_1, $\bar{S_2}$, $\bar{S_5}$, and $\bar{S_6}$ ON. At the same time, switch S_4 is turned ON to charge C_B.

- $0.5V_{dc}$ mode: For this voltage level generation, switches S_1, $\bar{S_2}$, S_3, and S_6 are ON, resulting in a voltage of $0.5V_{dc}$ across the load terminals.

- $0V_{dc}$ mode: This voltage level is generated by turning S_1, S_2, S_3, and S_6 ON, the voltage employed to the load terminal is 0. Both the capacitors are unaffected in this mode.

4.8 Modulation technique

The fundamental frequency PWM approach is utilized to produce gating signals. The rationale behind the selection of the fundamental switching frequency PWM method is to formulate the energy balance expressions straightforwardly. Besides that, switching losses decrease significantly, therefore, improving the quality of the output waveforms. In this regard, the obtained transition angles (α_n) in terms of the sinusoidal reference (V_m), number of voltage levels (N_l) are,

$$\alpha_n = \left(\frac{2n-1}{N_l}\right) \times V_m; \quad n = 1, 2, 3..., \frac{N_l - 1}{2} \tag{4.12}$$

Nonetheless, other PWM techniques like round-control method, selective harmonic minimization methods are also equally applicable. For the proposed nine-level inverter, four dc signals (α_1 - α_4) which corresponds to the switching angles obtained using (4.12) are compared with a rectified sine wave ($V_{ref} = |V_m \sin(\omega t)|$) to generate firing pulses of the semiconductor switches. The output of comparators are designated as A_1 - A_4 and a cycle selector as P. Further, the gating signals as shown in Figure 4.11 for each of the switches are derived using the switching combination listed in

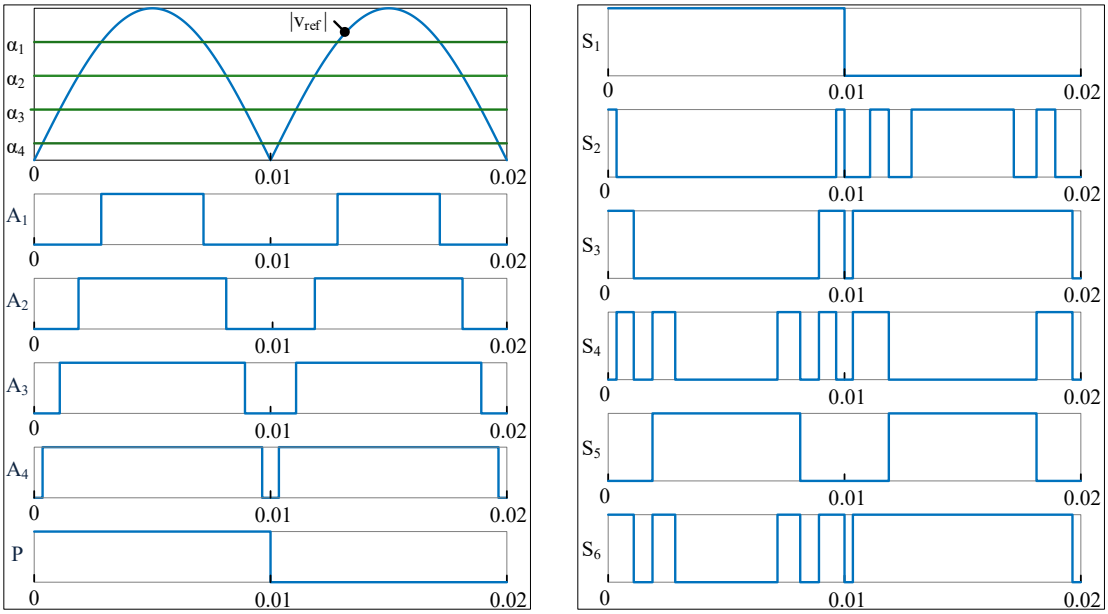


Figure 4.11: PWM switching scheme: (a) Comparator outputs, (b) Gating signals

Table 4.3. Thus, the overall switching function is given as,

$$S_1 = P \tag{4.13}$$

$$S_2 = \bar{A_4} \cdot P + (A_1 + \bar{A_2} \cdot A_3) \cdot \bar{P} \tag{4.14}$$

$$S_3 = \bar{A_2} \cdot P + A_1 \cdot \bar{P} \tag{4.15}$$

$$S_4 = (\bar{A_3} \cdot A_4 + \bar{A_1} \cdot A_2) \cdot P + \bar{A_2} \cdot A_4 \cdot \bar{P} \tag{4.16}$$

$$S_5 = A_2 \tag{4.17}$$

$$S_6 = (\bar{A_2} + A_3 \cdot A_4) \cdot P + A_1 \cdot \bar{P} \tag{4.18}$$

4.9 Simulation and experimental results

Stand-alone system with an input DC voltage of 50 V with different variations of the passive load is considered. The fundamental switching PWM approach is utilised to produce gating signals. The calculated capacitance with 5% voltage-ripple for C_B, C_{LD}, is 6352 μF, 3866 μF, respectively. Simulated results at different loading conditions are shown in Figure 4.12(a)-(d).

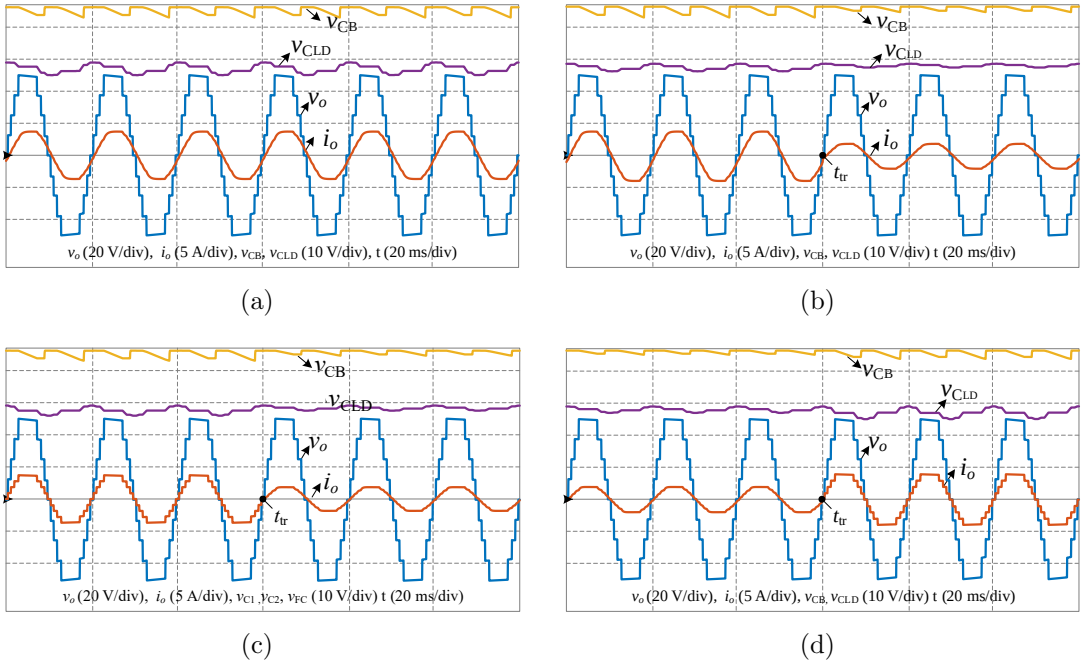


Figure 4.12: Simulation waveforms: (a) 30 Ω - 20 mH load, (b) step increment in load at t_{tr} sec from 30 Ω - 20 mH to 60Ω - 40 mH, (c) dynamic change in load at t_{tr} sec from 30 Ω to 60 Ω - 20 mH, (d) step decrement in load at t_{tr} sec from 60 Ω - 20 mH to 30 Ω.

The steady-state waveforms at $m_a = 1$ is shown in Figure 4.12(a). It is known that the ripples across the capacitors are unavoidable. Voltage of capacitor, C_{LD}, is fluctuating between 25.2 V to 23.8 V and C_B between 50 V to 47.3 V. The achieved peak output voltage is nearly equal to 100 V, with nine different levels between +100 V to -100 V. The transient response of the proposed topology is tested with different loading conditions. Capacitor voltages, load voltage, and currents at different dynamic changes in load are portrayed in Figure 4.12(b)-(d). The dynamic change is applied to the load at t_{tr} sec. In first scenario, the inverter load is changed from 30 Ω - 20 mH to 60 Ω - 40 mH and 30 Ω to 30 Ω - 20 mH as portrayed in Figure 4.12(b), (c). In second scenario, a sudden decrement in load from 60 Ω - 20 mH to 30 Ω is applied as shown in Figure 4.12(d). Capacitors maintained their reference voltages at all dynamic changes in load and produced nine voltage levels. Ripple across the capacitor voltage has reduced when the load is increased. And the reverse effect is also observed when half of the load is suddenly withdrawn. As discussed in Appendix B, the change in ripple is because of the change in time-constant of the charging and discharging loop. It is perceived from the figures that the output

voltages, currents, and capacitors' voltages are at their expected reference values. Therefore, the proposed inverter has a fast and proper voltage and current response under sudden changes in power conditions.

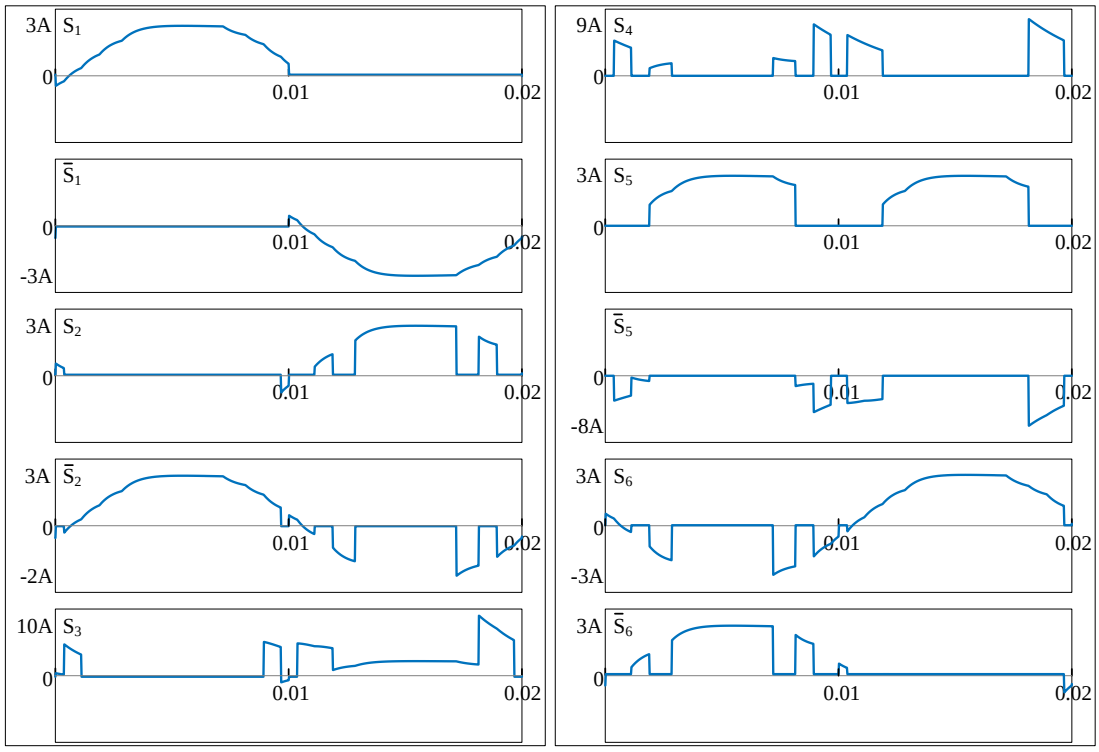


Figure 4.13: Current stress in the semiconductor devices

Later, simulated current stress of the semiconductors are shown in Figure 4.13. It is known that large currents flow in the semiconductors that are involved in the charging loop of SC-based converters. With the capacitance of 6352 μF, 3866 μF, and 3.47 A load current, the current peak of the switches involved in the charging loop (S_3, S_4), and $\bar{S_5}$ at ideal condition is about three times of load current. As power of the converter increases, the magnitude of the spike in component rises. However, the remaining switch current stress are with in the limits of load current, i.e., 3.47 A. Several techniques are proposed to limit these current spikes such as adjusting the rise and fall time of the semiconductor, increasing switching frequency, by selecting optimum capacitor value, by using an inductor or a resistor at the input (Khenar et al., 2018). At the given experimental parameters of the proposed work, semiconductor's internal resistance (22 mΩ - 38 mΩ) and capacitor's equivalent series resistance (18 mΩ - 26 mΩ) are self-sufficient to reduce the spikes of current.

A prototype is developed in laboratory to verify the viability of proposed HNIT. Figure 4.14(a)-(d) shows the experimental tests at different modulation indices. When the modulation index, m_a is tuned between $0 < m_a \leq 0.25$, the generated output voltage levels are three with the voltage amplitude of 25 V. During $0.25 < m_a \leq 0.5$, the output levels are changed from three to five. The magnitude of the output voltage is 50 V at $m_a = 0.5$. During $0.5 < m_a \leq 0.75$, the output levels are changed from five to seven. The magnitude of the output voltage is 75 V at $m_a = 0.75$. Similarly, when $m_a > 0.75$, the generated output voltage levels are nine with a magnitude of 100 V. The proposed circuit, therefore, can produce different number of output levels stably under the different modulation indices.

The proposed circuit is tested at different loading conditions as well and the waveforms are portrayed in Figure 4.15(a)-(d). Figure 4.15(a) show the waveforms of load current, output voltage, and capacitor voltages at 30 Ω - 20 mH. The load voltage is formed of nine distinct levels with a peak of 100 volts, verifying the boosting and inductive-load capability. The RMS value of load variables (current, voltage) are 70.1 V and 2.46 A, respectively.

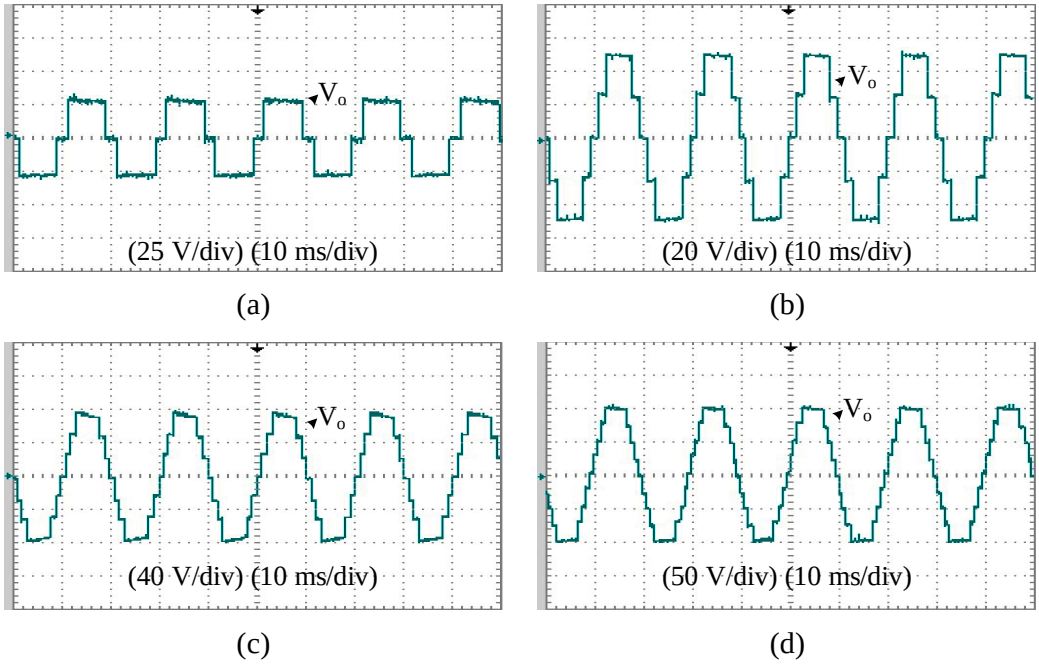


Figure 4.14: Output voltage at different modulation indices: (a) $m_a = 0.25$, (b) $m_a = 0.50$, (c) $m_a = 0.75$, and (d) $m_a = 1.0$.

The prototype is also examined at dynamic responses of load transients and corre-

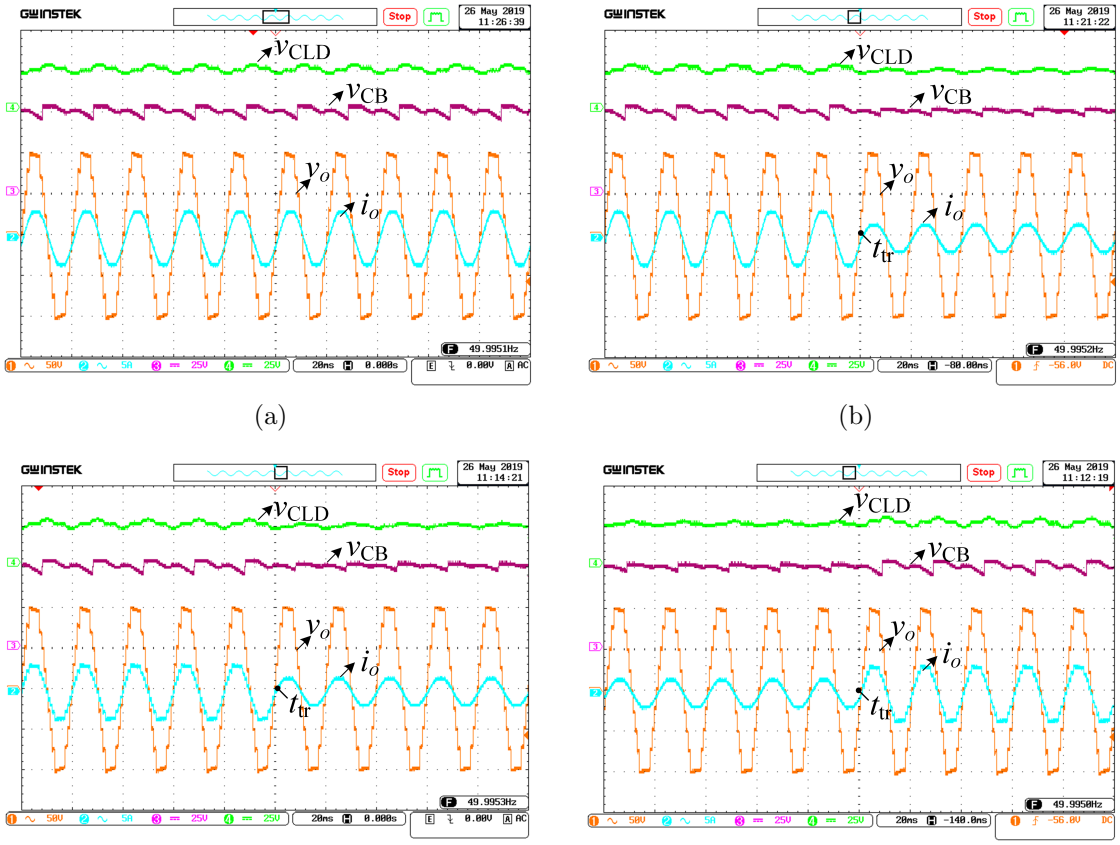


Figure 4.15: Experimental waveforms: (a) 30 Ω - 20 mH load, (b) step increment in load at t_{tr} sec from 30 Ω - 20 mH to 60Ω - 40 mH, (c) dynamic change in load at t_{tr} sec from 30 Ω to 60 Ω - 20 mH, (d) step decrement in load at t_{tr} sec from 60 Ω - 20 mH to 30 Ω.

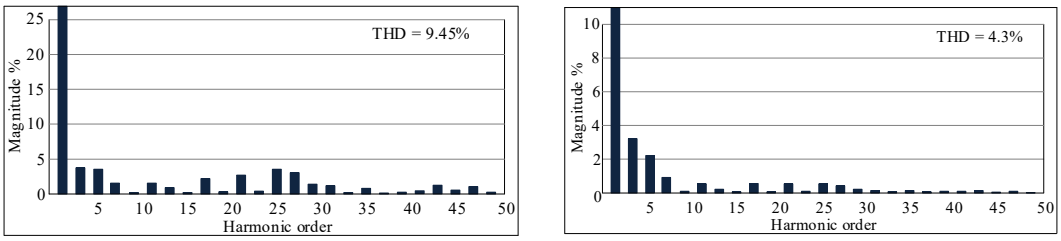


Figure 4.16: FFT spectrum of the load parameters: (a) load voltage, (b) load current.

sponding results are portrayed in Figure 4.15(b)-(d). The dynamic change is applied to the load at t_{tr} sec. Figure 4.15(b) shows the step increment in load from 30 Ω - 20 mH to 60 Ω - 40 mH. Figure 4.15(c) continues to examine the laboratory prototype's dynamic load transient response from 30 Ω to 60 Ω - 20 mH. Figure 4.15(d) shows the sudden decrement in load from 60 Ω - 20 mH to 30 Ω. It is perceived from the figures that the output voltages, currents, and capacitors' voltages are at their expected values. Ripple in capacitor voltages has reduced due to the increased time constant of the discharging loop. The same effect is observed on the capacitor voltages due to a step increment in load impedance. The speedy response in load current, capacitor voltages are perceived. Irrespective of the transients in load, it is seen that no deterioration is noticed in the capacitor and output voltages. Meanwhile, all capacitors continued to maintain their reference values with an agreeable ripple. Good agreement between simulation and laboratory results are observed. The 100 V peak of output voltage waveform proving the boosting ability. Sinusoidal load current waveform proving the inductive load ability of the proposed inverter. The boosting property of the topology eliminates half of the series batteries required in the non-boosting inverter topologies. Half of the battery cells can be eliminated with dual voltage boosting for the same voltage requirement. The proposed module can be expended for higher voltage levels to lower the need for battery cells, thereby the reduced equalization control complexity and inductive, resistive components. The fundamental, other components of the output voltage and current from the FFT spectrum are captured in Figure 4.16(a), (b). The odd harmonics are greatly suppressed, and a THD of 9.45% for voltage and 4.3% for current are recorded.

4.10 Comparative analysis

Further, a comparison is conducted in Table. 4.4, 4.5 with state-of-art voltage boosting topologies to highlight the benefits of proposed hybrid topologies. The comparison is carried for N_l levels and the proposed structure is performing well in terms of semiconductors, DC sources, capacitors and PIVs. Topology in (Ye et al., 2014) performs better in terms of switches but requires more capacitors and diodes than the proposed configurations. Moreover, H-bridge at the back-end has to withstand the peak value of the output voltage. Whereas the peak voltage of BH-MLI is not more than the supply voltage, and the peak voltage of HNIT is only twice the supply voltage.

The voltage gain property, less component requirement, and voltage stress on the semiconductors indicate that the proposed topology has a wide-range of utilization than the compared MLIs enlisted in Table 4.4. The proposed converters find their applications where the input voltage is low and requires high-voltage at the output like electric vehicles, renewable energy.

The peculiar advantages of the proposed configuration cannot be judged adequately through the component count. Hence, it is required to estimate the cost and thereby attest the benefits of the topology through a complete cost analysis. A comparison outcome is enlisted in Table 4.5. For the fair comparison, the generic rates of components and the identical source voltage is considered for all inverters. From the comparison presented in Table 4.5, the cost of the proposed circuit is lower than most of the other circuits, and it is marginally higher than the circuit in (Ye et al., 2014). On the other side, the circuit in (Ye et al., 2014) not suited for high voltage applications due to PIV of the H-bridge. In a nutshell, proposed topologies offer excellent operational performance for high-quality dc-ac energy conversion systems at economical cost.

Table 4.4: Comparison of the proposed circuits with the recently developed topologies

Parameter	Topology							
	1	2	3	4	5	6	7	BH-MLI
N_{sw}	$\left(\frac{5N_l-17}{2}\right)$	$\left(\frac{N_l+7}{2}\right)$	$\left(\frac{3N_l+7}{2}\right)$	$\left(\frac{5N_l-7}{2}\right)$	$3\left(\frac{N_l-1}{2}\right)$	$3\left(\frac{N_l-1}{2}\right)$	$\left(\frac{3N_l-1}{2}\right)$	$\left(\frac{5N_l-1}{4}\right)$
N_{Cap}	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-1}{4}\right)$	$\left(\frac{N_l-1}{2}\right)$	$\left(\frac{N_l-3}{2}\right)$	$\left(\frac{N_l-1}{4}\right)$
N_{diode}	$\left(\frac{N_l-5}{2}\right)$	$(N_l - 3)$	-	-	-	$\left(\frac{N_l-1}{2}\right)$	-	-
N_{dc}	1	1	1	1	$\left(\frac{N_l-1}{8}\right)$	$\left(\frac{N_l-1}{4}\right)$	1	1
PIV*V_{dc}	$\left(\frac{N_l-4}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	4	1	1	$2(N_l-1)$	$\left(\frac{N_l-1}{2}\right)$	1
H-Bridge stress	$\left(\frac{N_l-4}{2}\right)$	$\left(\frac{N_l-1}{2}\right)$	-	-	-	-	$\left(\frac{N_l-1}{2}\right)$	-
TSV	$\left(\frac{9N_l-41}{2}\right)$	$5\left(\frac{N_l-1}{2}\right)$	$\left(\frac{7N_l-11}{2}\right)$	$\left(\frac{5N_L-7}{2}\right)$	$\left(\frac{3N_l-5}{2}\right)$	$\left(\frac{9N_l-29}{2}\right)$	$\left(\frac{7N_l-5}{2}\right)$	$\left(\frac{5N_l-9}{4}\right)$

N_{sw} - No. of active switches, N_{Cap} - No. of capacitors, N_{diode} - No. of diodes, N_{dc} - No. of DC sources.

1. Liu et al. (2018a)
2. Ye et al. (2014)
3. Khenar et al. (2018)
4. Taghvaie et al. (2018)
5. Lee (2018)
6. Saeedian et al. (2018b)
7. Barzegarkhoo et al. (2016)

Table 4.5: Cost comparison of proposed circuits with other SC based topologies for nine-levels

Component	Series	Rating	Unit price	Topology							
			($)	1	2	3	4	5	6	BH-MLI	HNIT
MOSFET	IRFP350PBF	400 V	2.98	4	-	4	-	-	4	-	-
	IRFP240PBF	200 V	2.31	-	9	-	-	4	-	-	2
	IRFI4321PBF	150 V	2.12	-	-	-	-	-	-	-	2
	IRFP9140NPBF	100 V	1.89	4	8	15	10	8	11	7	2
	IRFZ20PBF	50 V	1.63	-	-	-	2	-	-	4	4
Gate driver	IR2110SPBF	-	1.92	8	14	19	12	12	15	11	10
Capacitor	B41231A9128M	1.2 mF	1.51	3	4	3	2	4	3	2	2
Diode	SDT10A100P5	100 V	0.61	6	4	3	0	4	1	-	-
Total price ($)				43.03	71.27	83.11	48.22	55.88	66.67	43.89	41.38

Courtesy: mouser.com, in.element14.com, www.digikey.com; *prices are subject to change

1. Ye et al. (2014)
2. Khenar et al. (2018)
3. Taghvaie et al. (2018)
4. Lee (2018)
5. Saeedian et al. (2018b)
6. Barzegarkhoo et al. (2016)

Chapter 5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

Nowadays, output voltage boosting property along with the curtailment in the component count and voltage stress are considered the essential topological features for the new MLI circuits. The need for MLIs has grown prominently in several fields such as motor drives, renewable, electric vehicles, and unit power supply systems due to their high-quality output wave-forms. Many topological and control issues of MLIs have been studied and described. Though significant efforts are made in reducing the complexity of MLIs, there is a way to develop alternate solutions that further lessen the operational and control challenges. Among the existing topologies, there is a need to investigate, understand the properties, and propose suitable modifications to make them more adaptable depending on the applications. Output voltage boosting ability is one of the main requirements of the converter for the applications like electric vehicles, renewable energy, high-voltage pulse generator. Besides, the evolution of MLIs is tending to reduce the number of components, especially dc sources based on the combination of capacitors. In these topologies, replacing dc sources with capacitors reduce the number of dc sources and the cost of the converter. SC-based converters are the basic alternative solution that does not need any transformer to boost the voltage. With this thought, the main contributions of this thesis are the proposal and verification of four different converters with suitable uncomplicated control strategies.

The general conclusion of each chapter has been collected as follows:

Chapter 1 presented a brief overview of high-power converters and state-of-the-art MLI topologies and, in particular, critically reviewed the classical, recent MLIs with reduced part count and their associated intricacies concerning the high-power applications. As an outcome, it was learned that despite many solutions capable of generating more voltage levels, an opportunity for developing an alternative way of achieving the same endures.

Chapter 2 demonstrated the MT-MLI with the reduced part count. Besides, a sensor-less voltage balancing control to regulate the FC voltage is elaborated. Detailed simulation and experimental studies are carried out to validate the proof of controllability of the proposed topology and their associated control scheme. Methods to extend the topology for higher voltage levels are studied. Furthermore, a comparison in terms of component count is deliberated to highlight the potential merits of the proposed MT-MLI.

A new SSHB-MLI structure based on SCs with hexad boost capability is presented in Chapter 3. The circuit operation and modulation scheme are discussed. Extension methods for the high number of levels with a single as well as multiple dc voltage sources are derived. Capacitors' voltage ripple and curve-fitting approaches to calculate the power losses are analyzed in detail. Besides, a detailed quantitative-, cost-comparison with existing inverter circuits verified that the proposed SSHB inverter is a viable and economical solution where the source is a low voltage supply. Finally, experimental test results at different load conditions are discussed.

Chapter 4 proposed two hybrid-MLI configurations: BH-MLI, HNIT with voltage boosting ability, and less component count. A simple LGB switching controller is developed for the presented circuits. Simple structure, voltage boosting, and easy control are the additional benefits of the proposed arrangements. Output voltage waveforms have proved a gain of two for nine-level constructions. Extensions of BH-MLI for higher levels using are presented. Further, the performance of the proposed circuits is validated experimentally with PD-PWM and round control method at different modulation indices, load conditions. Finally, quantitative-, cost-comparisons are conducted among the state-of-art SC-MLIs to highlight the superiority of the proposed configurations.

5.2 Future scope

Based on the research carried out in this thesis, the recommendations for future research are as follows:

- Investigate the application of the presented hybridization technique to other MLIs, resulting in many other interesting topologies.
- Integrate the proposed PWM methods with capacitance voltage ripple minimization techniques for additional improvement in output voltage quality by eliminating the low-frequency voltage ripples, thereby reducing the capacitance.
- Employ the proposed MT-MLI topology with grid-connected applications such as motor control drives, dynamic voltage restores, and active filters, to name a few.
- Integrate the proposed SSHB and hybrid MLI topologies with the electric vehicle applications to check the viability and performance.
- Further investigate device-level fault-tolerant studies about the proposed topologies. Further inclusion of additional reliability constraints and other reliability functions helps in a more precisive quantification of the developed topologies.

Appendix A

CAPACITANCE CALCULATION

In capacitor-based inverters, particularly SC-based inverters, capacitance calculation plays a vital part in keeping the ripple within the permissible limit. The less voltage fluctuation in the capacitor results in lower power losses, thereby high converter efficiency (Hinago and Koizumi, 2012). Capacitance is determined by considering the capacitors' peak current, maximum discharging time interval, and permitted ripple. Time intervals (t_1, t_2, t_3,...) for each level change are marked in Figure A.1. Load current agrees with the voltage when the load is purely resistive. At this power factor, maximum discharge occurs in the capacitor due to the peak current is at the midpoint of the integration. In other words, if the capacitor is sized at unity power factor, it also maintains less ripple for other power factors. Assuming unity power factor, m_a = 1 the longest discharging time-intervals of C_B, C_{LD} from Figure A.1 is between [t_{11}, t_{14}], and [t_1 - t_2, t_3 - t_4, t_5 - t_6, t_7 - t_8] respectively. Since the output waveform follows the symmetry, negative half-cycle time intervals are the same as positive half-cycle. Similarly, due to quarter-wave symmetry, time period between [t_7, t_8] is same as [t_1, t_2] and time period between [t_5, t_6] is same as [t_3, t_4]. Further, the maximum discharge of each capacitor is calculated based on the following expressions:

$$\Delta Q_{C_B} = \int_{t_{11}}^{t_{14}} I_o \sin(\omega t) dt \tag{A.1}$$

$$\Delta Q_{C_{LD}} = 2\int_{t_1}^{t_2} I_o \sin(\omega t) dt + 2\int_{t_3}^{t_4} I_o \sin(\omega t) dt \tag{A.2}$$

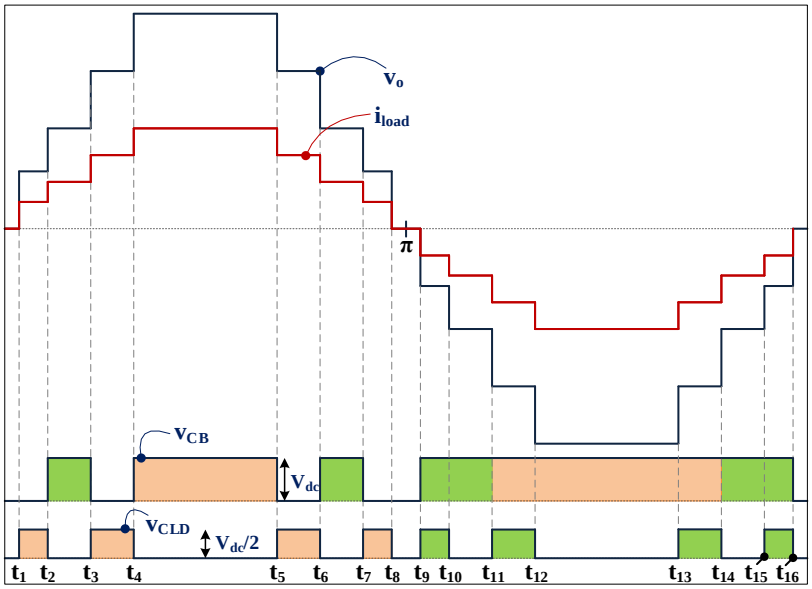


Figure A.1: Key waveforms of HNIT

In which I_o is the peak load current through the capacitor, ω is the fundamental frequency in rad/sec, and time-intervals $(t_1 - t_8)$ are represented as

$$t_1 = \frac{\sin^{-1}\left(\alpha_4/V_{ref}\right)}{2\pi f_{ref}} = 3.5440 \times 10^{-4} \text{ sec} \tag{A.3}$$

$$t_2 = \frac{\sin^{-1}\left(\alpha_3/V_{ref}\right)}{2\pi f_{ref}} = 1.0817 \times 10^{-3} \text{ sec} \tag{A.4}$$

$$t_3 = \frac{\sin^{-1}\left(\alpha_2/V_{ref}\right)}{2\pi f_{ref}} = 1.8749 \times 10^{-3} \text{ sec} \tag{A.5}$$

$$t_4 = \frac{\sin^{-1}\left(\alpha_1/V_{ref}\right)}{2\pi f_{ref}} = 2.8365 \times 10^{-3} \text{ sec} \tag{A.6}$$

$$t_5 = \frac{\pi - \sin^{-1}\left(\alpha_1/V_{ref}\right)}{2\pi f_{ref}} = 7.1634 \times 10^{-3} \text{ sec} \tag{A.7}$$

$$t_6 = \frac{\pi - \sin^{-1}\left(\alpha_2/V_{ref}\right)}{2\pi f_{ref}} = 8.1250 \times 10^{-3} \text{ sec} \tag{A.8}$$

$$t_7 = \frac{\pi - \sin^{-1}\left(\alpha_3/V_{ref}\right)}{2\pi f_{ref}} = 8.9182 \times 10^{-3} \text{ sec} \tag{A.9}$$

$$t_8 = \frac{\pi - \sin^{-1}\left(\alpha_4/V_{ref}\right)}{2\pi f_{ref}} = 9.6455 \times 10^{-3} \text{ sec} \tag{A.10}$$

Accordingly, the least value of the capacitance needed with admissible ripple per-

centage (x%) in capacitor voltage is expressed as:

$$C_n = \frac{\Delta Q_{C_n}}{x\% \times V_{C_n}} \tag{A.11}$$

The required capacitance for the 50 V source at unity power factor (30 Ω resistive load) with the voltage ripple of 5% can be calculated as

$$C_B = \frac{1}{x\% \times V_{C_B}} \int_{t_3}^{t_6} I_o \sin(\omega t) dt \tag{A.12}$$

$$= \frac{1}{0.05 \times 50} \int_{1.8749\times10^{-3}}^{8.125\times10^{-3}} 3 \sin(2\pi f t) dt \tag{A.13}$$

$$C_B = 6.352 \text{ mF} \tag{A.14}$$

$$C_{LD} = \frac{1}{x\% \times V_{C_{LD}}} \Big[2 \int_{t_1}^{t_2} I_o \sin(\omega t) dt + 2 \int_{t_3}^{t_4} I_o \sin(\omega t) dt \Big] \tag{A.15}$$

$$= \frac{1}{0.05 \times 25} \Big[2 \int_{3.544\times10^{-4}}^{1.0817\times10^{-3}} 3 \sin(\omega t) dt + 2 \int_{1.8749\times10^{-3}}^{2.8365\times10^{-3}} 3 \sin(\omega t) dt \Big] \tag{A.16}$$

$$C_{LD} = 3.866 \text{ mF} \tag{A.17}$$

Similarly the capacitance of capacitors that involved in other topologies are calculated.

Appendix B

PROOF OF SELF VOLTAGE BALANCING

Capacitors are utilized as virtual sources to generate levels in the proposed topologies. These capacitors are charged and discharged several times in a fundamental cycle. The repetition of the above process naturally regulates the capacitors to settle at their reference value to satisfy charge-balance or amp-second balance theory. A detailed derivation validating the balancing of capacitors is discussed in this appendix.

B.1 Flying capacitor

Flying capacitors in Chapter 2, Chapter 4 are discharged in a positive half cycle and charged at the same level in a negative half cycle. It can be perceived from the Figure B.1 that the FC is not contributing for the voltage levels $\pm 2V_{dc}$ and $\pm V_{dc}$. Therefore, the FC currents for $\pm 0.5V_{dc}$ and $\pm 1.5V_{dc}$ levels are derived in terms of voltage across FC (v_{FC}), load impedance (Z) as

$$i^{+}_{FC,0.5V_{dc}} = \frac{v_{FC}}{Z} \tag{B.1}$$

$$i^{+}_{FC,1.5V_{dc}} = \frac{V_{dc} + v_{FC}}{Z} \tag{B.2}$$

$$i^{-}_{FC,0.5V_{dc}} = \frac{v_{FC} - V_{dc}}{Z} \tag{B.3}$$

$$i^{-}_{FC,1.5V_{dc}} = \frac{-2V_{dc} + v_{FC}}{Z} \tag{B.4}$$

The net charge (Q) delivered/absorbed by FC over a fundamental period (t) is expressed as,

$$Q = (i^{+}_{FC,0.5V_{dc}} + i^{+}_{FC,1.5V_{dc}} + i^{-}_{FC,0.5V_{dc}} + i^{-}_{FC,1.5V_{dc}})t \tag{B.5}$$

$$= \left(\frac{v_{FC}}{Z} + \frac{V_{dc} + v_{FC}}{Z} - \frac{V_{dc} - v_{FC}}{Z} - \frac{2V_{dc} - v_{FC}}{Z}\right)t \tag{B.6}$$

$$= \left(\frac{4v_{FC} - 2V_{dc}}{Z}\right)t \tag{B.7}$$

At steady-state conditions, the net charge in a given fundamental cycle is zero. Therefore, from (B.7), the voltage across FC will be equal to half of the total dc voltage, i.e., $v_{FC} = 0.5V_{dc}$ and it is achieved without any supplementary controlling algorithm.

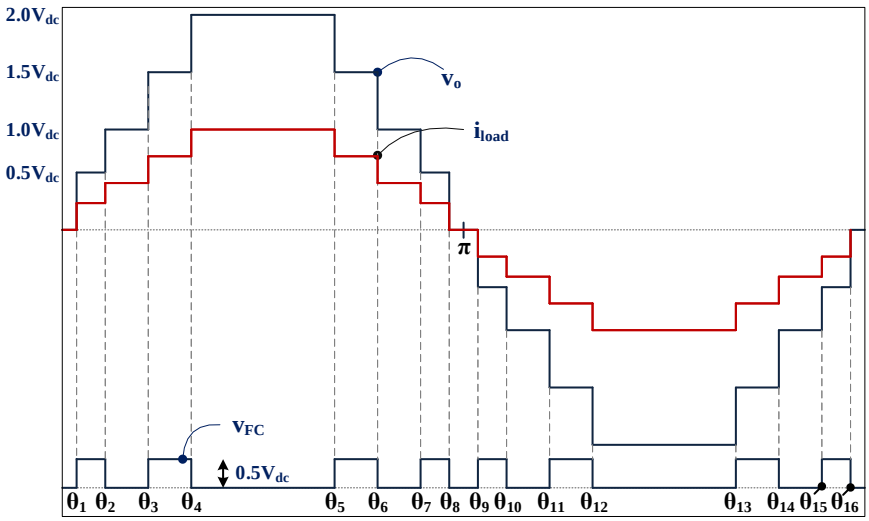


Figure B.1: Generic nine-level output voltage of a proposed inverters using fundamental switching method

Assume that the MLI is operating at unity power factor load and output waveforms are in half-wave symmetry. For a nine-level inverter, there are eight discrete intervals per cycle. FC applies a positive voltage at terminals when it is required to produce voltage levels. For the rest of the intervals, the terminal voltage of FC is zero, as shown in Figure B.1. Therefore, the total delivered energy in the first-half cycle (w_{+}) and second half-cycle (w_{-}) in terms of the output voltage (v_o), and load current (i_{load}) are expressed as

$$w_{+} = v_o \; i_{load} \sum_{n=1}^{4} \int_{\theta_{2n-1}-\phi}^{\theta_{2n}-\phi} \sin\theta d\theta \tag{B.8}$$

$$w_{-} = v_o \; i_{load} \sum_{n=5}^{8} \int_{\theta_{2n-1}-\phi}^{\theta_{2n}-\phi} \sin\theta d\theta \tag{B.9}$$

Equation (B.9) may be rewritten as

$$w_{-} = v_o \; i_{load} \sum_{n=1}^{4} \int_{\theta_{2n-1+8}-\phi}^{\theta_{2n+8}-\phi} \sin\theta d\theta \tag{B.10}$$

The energy absorbed/delivered by FC depends on the integration sign. Owing to the symmetrical nature of the output voltage, from the waveforms shown in Figure B.1, it is noticed that

$$\theta_9 = \pi + \theta_1, \theta_{10} = \pi + \theta_2, ..., \theta_{16} = \pi + \theta_8 \tag{B.11}$$

Thus, the right-hand side integral of (B.10) can be represented as

$$v_o \; i_{load} \int_{\theta_{2n-1}-\phi}^{\theta_{2n}-\phi} \sin\theta d\theta = v_o \; i_{load} \int_{\theta_{\pi+2n-1}-\phi}^{\theta_{\pi+2n}-\phi} \sin\theta d\theta. \tag{B.12}$$

From (B.8), (B.10), and (B.12) the relation can be deduced as

$$w_{+} = -w_{-} \tag{B.13}$$

Thus, the energy flowing into and from the FC is equal to the full cycle of fundamental voltage. In other words, it results in keeping the voltage across FC at desired level in all condition. This principle of energy balance stabilizes and regulates the voltage across FC naturally without any voltage and/or current sensor(s) thereby facilitate in the reduction of proposed inverter's overall design cost.

B.2 Switched capacitor

Unlike FC, SCs are charged with same magnitude of supply voltage throughout the operation. Charging and discharging of SC sub-module is portrayed in Figure B.2(a)-(c). Capacitor C charges to the source voltage V_{dc} through $\bar{S_3}$, and diode D as shown in Figure B.2(b). Load impedance does not affect the charging loop's time constant. While discharging, Capacitor is connected in additive nature with source through switch S_3 as pictured in Figure B.2(c). However, load impedance comes into the loop during discharging the capacitor. Because of the load resistance is high compared to the component parasitic resistance of components, the discharging loop's time constant increases.

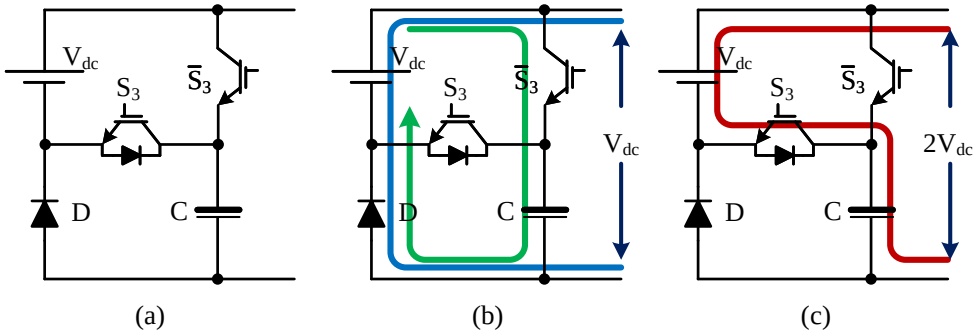


Figure B.2: Basic sub-block of the SC-MLI

The equivalent parasitic circuit for charging and discharging of SC is portrayed in Figure B.3. Due to semiconductors' parasitic resistance is meager, the charging loop's time constant ($(r_s + r_d + r_c)C = 60\times10^{-3} \times 6.3\times10^{-3} = 0.378\times10^{-3}$ sec) is very small. Here r_s, r_d are internal resistance of switch, diode, and r_c is equivalent series resistance of capacitor. Typical internal resistance of IGBT (SKM75GB123D), anti-parallel diode, and capacitor (CGS632U075R5L) are 25 mΩ, 18 mΩ and 17 mΩ, respectively. Since the internal resistance of semiconductors and capacitors is very less, capacitor charges to its final value (in five time-constants) in no time. The time constant of discharging loop ($(R + r_s + r_c)C = 30.042 \times 6.3\times10^{-3} = 189.27\times10^{-3}$ sec) is far higher compared to the charging loop ($189.27\times10^{-3} >> 0.378\times10^{-3}$). Thereby, capacitor voltages are maintained at required values even with few charging instances. It is worthy of mentioning that the capacitor voltage is kept at V_{dc} (by neglecting component voltage drop) without any additional balancing circuit, therefore, reduced control complexity.

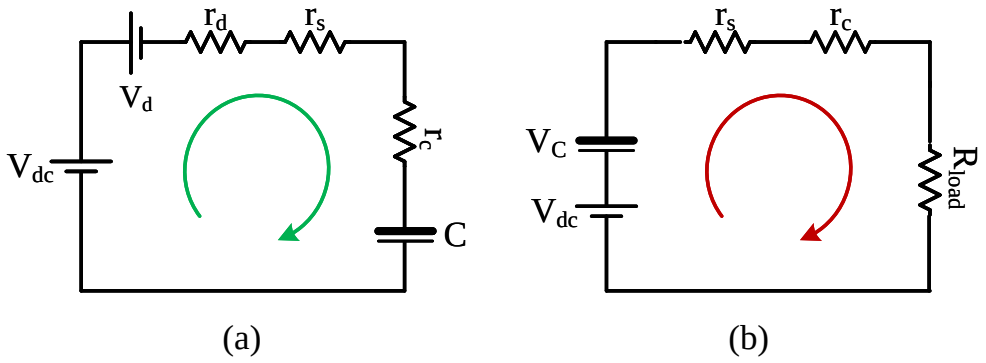


Figure B.3: Equivalent circuit of sub-module: (a) charging of C_B, (b) discharging of C_B

From A.1, A.2, and A.11, it is observed that the ripple is proportional to the charge across the capacitor. Higher the value of the load resistance or fundamental frequency $\Longrightarrow$ lower the voltage ripple due to increased time-constant of discharging loop $\Longrightarrow$ smaller the required capacitor size.

Appendix C

LOSS CALCULATION

C.1 Generalized curve fitting analysis of the power IGBT

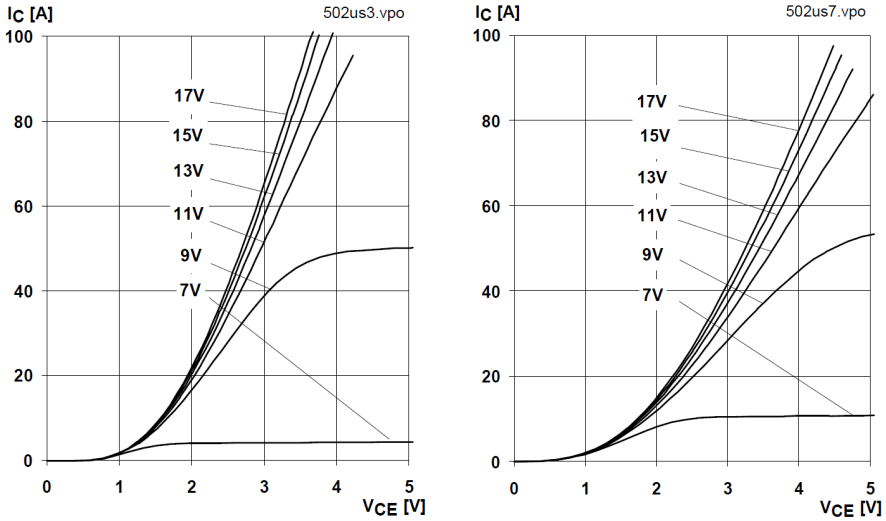
The conduction and switching loss equations are derived from the curve fitting approach, which calculates the total losses of the semiconductor device. Moreover, it has high accuracy and can be planted directly in any circuit simulator. These loss calculations are based on semiconductor data-sheet values and experimental measurements. The MLIs presented in the above chapters are built with the SKM75GB123D IGBT module. Therefore the SKM75GB123D data-sheet information is considered for further explanations.

C.1.1 Conduction loss

Conventionally, the conduction losses are calculated by placing the V_d representing forward voltage drop and a resistor R_S representing load current dependency in series with an ideal switch. Though this approach can be modeled merely in the simulator, the diodes and ideal switches are overloaded with additional parameters. Moreover, the circuit simulator should accommodate controllable resistors to build the temperature-dependent characteristics into this model. Thus, an actual procedure presented in (Drofenik and Kolar, 2005) is followed.

C.1.1.1 Calculation of the power IGBT conduction loss

The considered IGBT data-sheet (SKM75GB123D) provides characteristic curves between the collector-emitter voltage (V_{CE}) and collector-current (i_C) of the IGBT at different gate-emitter V_{GE} values. Moreover, the data sheet provided V_{CE} - i_C curves for minimum ($T_{min} = 25℃$) and maximum ($T_{max} = 125℃$) temperatures as shown in Figure C.1 individually to describe the temperature dependency.



(a) (b)

Figure C.1: V_{CE} verses i_C characteristic curves of the SKM75GB123D-IGBT switch: (a) at the minimum temperature 25℃, (b) at max temperature 125℃. (image curtsey: Semikron).

In fact, the experimental working gate-emitter potential voltage V_{GE} is equal to the 15 V. Thus, only one V_{CE} - i_C curve data is extracted from Figure C.1(a) and is mentioned in Table C.1. After that, multiply the V_{CE} with i_C to attain the power at each extracted point. This multiplication gives the power loss in terms of the collector current i_C. To achieve the approach mentioned above, i_C versus $P_{igbt,25°C}$ waveform is composed using MATLAB curve-fitting application. First, X- and Y-axes data (X-data representing i_C and Y-data representing $P_{igbt,25°C}$) are provided and then adjust the polynomial order till the error comes to the least point. The presented data has arrived at the second-order polynomial equation with a minimum error. Whereby the waveform is portrayed in Figure C.2 is achieved, and it has possessed the power loss

in (C.1).

$$P_{igbt,25°C} = 0.02365 \times i_C^2 + 1.551 \times i_C - 0.8995 \tag{C.1}$$

Table C.1: V_{CE} - i_C curve data points for V_{GE} = 15 V at T_{min} = 25°C

V_{CE}(V)	i_C(A)	$P_{igbt,25°C} = (V_{CE} \times i_C)$
0	0	0
1	1.4286	1.4286
1.5	8.5714	12.8571
2	21.4286	42.8572
2.5	40	100
3	62.1429	186.4287
3.5	82.8571	289.999

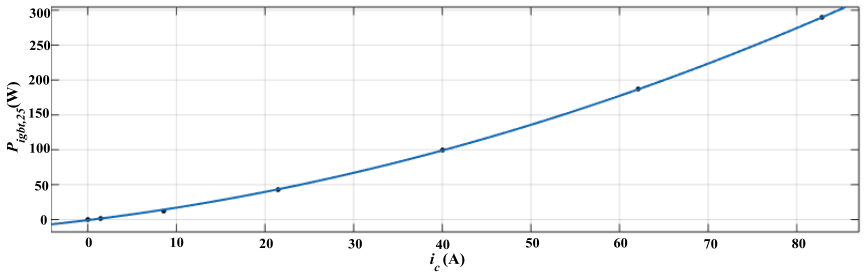


Figure C.2: Curve fitting waveform for IGBT conduction loss at 25℃ with respect to the collector current i_C.

In the similar way, the corresponding waveform of the power loss equation (C.2) at 125℃ temperature is drawn as per the Table C.2 and it has shown in Figure C.3.

$$P_{igbt,125°C} = 0.02876 \times i_C^2 + 1.914 \times i_C - 2.452 \tag{C.2}$$

The coefficients should represent the running temperature (T) to specify the temperature dependency in the conduction loss equation. The generalized temperature-dependent second-order conduction loss equation has arrived at (C.3).

$$P_{igbt}(i_C, T) = (a_0 + a_1 T)i_C^2 + (b_0 + b_1 T)i_C + (c_0 + c_1 T) \tag{C.3}$$

Table C.2: V_{CE} - i_C curve data points for V_{GE} = 15 V at T_{max} = 125° C

V_{CE}(V)	i_C(A)	$P_{igbt,125°C} = (V_{CE} \times i_C)$
0	0	0
1	2.1429	2.1429
1.5	5.7143	8.5714
2	14.2857	28.5714
2.5	25.7149	64.2873
3	40	120
3.5	55.7143	195.0001
4	72.8571	291.4284
4.5	91.4286	411.4287

These loss pertinent coefficients are derived from the coefficients of the (C.1) and (C.2) and are enlisted in Table C.3. In the considered case shown in Figure C.1 and C.4, only two operating temperatures (T_{min} = 25℃ and T_{max} = 125℃) are given, resulting in a first-order approximation. The power loss equation is in second order, but the first order approximation calculates the coefficients.

$$a_0 = \frac{P_{igbt,25°C,a} \times T_{max} - P_{igbt,125°C,a} \times T_{min}}{T_{max} - T_{min}} \tag{C.4}$$
$$= \frac{(0.02365 \times 125) - (0.02876 \times 25)}{125 - 25} = 0.0224$$

$$a_1 = \frac{P_{igbt,125°C,a} - P_{igbt,25°C,a}}{T_{max} - T_{min}} = 0.00005 \tag{C.5}$$

$$b_0 = \frac{P_{igbt,25°C,b} \times T_{max} - P_{igbt,125°C,b} \times T_{min}}{T_{max} - T_{min}} = 1.46025 \tag{C.6}$$

$$b_1 = \frac{P_{igbt,125°C,b} - P_{igbt,25°C,b}}{T_{max} - T_{min}} = 0.00363 \tag{C.7}$$

$$c_0 = \frac{P_{igbt,25°C,c} \times T_{max} - P_{igbt,125°C,c} \times T_{min}}{T_{max} - T_{min}} = -0.511375 \tag{C.8}$$

$$c_1 = \frac{P_{igbt,125°C,c} - P_{igbt,25°C,c}}{T_{max} - T_{min}} = -0.015525 \tag{C.9}$$

An (C.3) will be modified as follows by substituting all the above constants,

$$P_{igbt}(i_c, T) = (0.0224 + 0.000058 \times T)i_c^2 + (1.46025 + 0.00363 \times T)i_c \tag{C.10}$$
$$- (0.511375 + 0.015525 \times T)$$

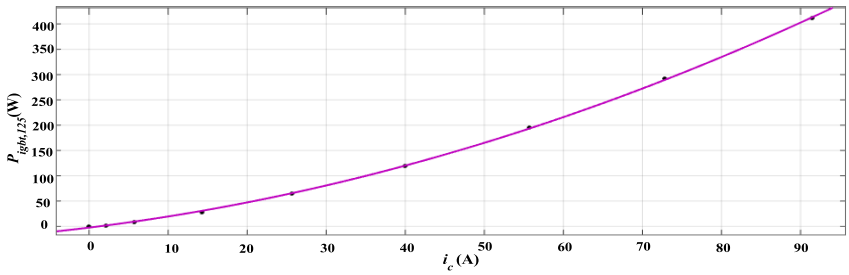


Figure C.3: Curve fitting waveform for IGBT conduction loss at 125℃ with respect to the collector current i_C.

Table C.3: Loss pertinent coefficients at $T_{min} = 25°C$, $T_{max} = 125°C$

Loss coefficient	Value	Loss coefficient	Value
$P_{igbt,25°C,a}$	0.02365	$P_{D,25°C,a}$	0.01521
$P_{igbt,25°C,b}$	1.551	$P_{D,25°C,b}$	1.245
$P_{igbt,25°C,c}$	-0.8995	$P_{D,25°C,c}$	-0.2321
$P_{igbt,125°C,a}$	0.028762	$P_{D,125°C,a}$	0.01485
$P_{igbt,125°C,b}$	1.914	$P_{D,125°C,b}$	1.06
$P_{igbt,125°C,c}$	-2.452	$P_{D,125°C,c}$	-0.8451

C.1.1.2 Calculation of the anti-parallel diode conduction loss

The anti parallel diode follows the same steps what the IGBT has done for calculating it's conduction losses.

- First, trace the corresponding diode characteristic curve V_f (forward voltage drop of the diode) versus i_f (forward current of the diode) from the data-sheet which is depicted in the Figure C.4.
- Second, trace the samples from the diode characteristic curves for minimum and maximum temperatures, it is described in Table C.4.
- Third, consider the X-axis data as $i_{f,25°C}$ ans Y-axis data as $P_{D,25°C}$ for $T_{min} = 25°C$ and fit the data into the MATLAB curve fitting application to get suitable loss equation in terms of i_f. In the same fashion, we can get the another loss equation for $T_{max} = 125°C$. The optimized diode conduction loss equations (C.11) & (C.12) and curve fitting graphs in Figure C.5 are given.

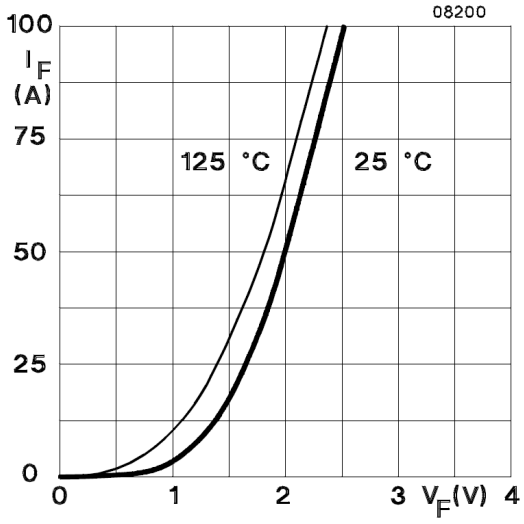
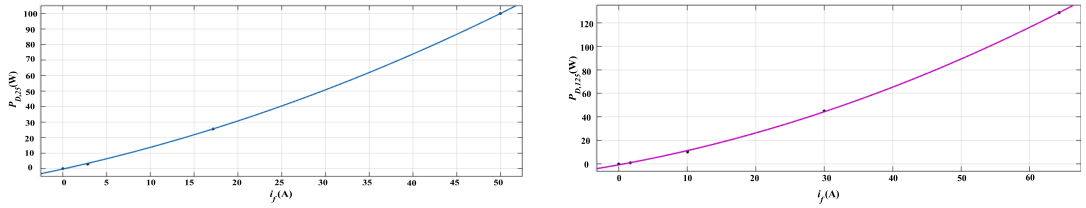


Figure C.4: Anti-parallel diode under investigation. (image curtsey: Semikron)

- Fourth, incorporate the temperature dependency in the conduction loss equation as similar to the (C.10) for this anti-parallel diode. Finally, the temperature dependent loss expression arrives at (C.13).

$$P_{D,25°C} = 0.01521 \times i_f^2 + 1.245 \times i_f - 0.2321 \tag{C.11}$$

$$P_{D,125°C} = 0.01485 \times i_f^2 + 1.06 \times i_f - 0.8451 \tag{C.12}$$



(a) (b)

Figure C.5: Diode curve fitting graphs for calculating conduction loss (P_D): (a) At the minimum temperature 25°C (b) At max temperature 125°C

Thereby, the coefficient matrix of the diode conduction loss parameter is deduced

Table C.4: V_f - i_f curve data points for $T_{min} = 25°C$ and $T_{max} = 125°C$

$V_{f,25°C}$ (V)	$i_{f,25°C}$ (A)	$P_{D,25°C}$	$V_{f,125°C}$ (V)	$i_{f,125°C}$ (A)	$P_{D,125°C}$
0	0	0	0	0	0
0.5	0	0	0.5	1.7143	0.8571
1	2.8571	2.8571	1	10	10
1.5	17.1429	25.714	1.5	30	45
2	50	100	2	64.2857	128.5714

as follows.

$$P_D(i_f, T) = (0.0153 \times T)i_f^2 + (1.2913 - 0.0019 \times T)i_f - (0.0789 + 0.0061 \times T) \tag{C.13}$$

C.1.2 Switching loss

The switching losses usually contribute a notable weight in the total power electronic device losses. Switching loss analysis is significant to estimate the junction temperature for improving the system reliability.

Table C.5: Extraction of the samples for deducing the switching factor at $T_{max} = 125°C$

i_C (A)	E_{ON} (mWs)	E_{OFF} (mWs)	E_{total} (mWs)	$K_{IGBT}(i_C)$ $\left(\frac{\mu Ws}{A}\right)$
30	4.2593	2.9630	7.2223	240.7
40	6.1111	4.0741	10.1852	254.6
50	8.1481	5.1852	13.3333	266.7
60	10.2222	6.1852	16.4074	273.5
70	12.5926	7.2222	19.8148	283.1
80	15.1111	7.9630	23.0741	288.4
90	17.9630	8.7037	26.6667	296.3

C.1.2.1 Switching loss factor calculation for the IGBT switch

The semiconductor device data-sheets are often provided the current dependency of the energy loss graphs as shown in the Figure C.6. Now we have to trace and

tabulate the total energy loss (E_{total}) samples from the Figure C.6 concerning the current waveform samples and is described in Table C.5. Herein, the ratio of the total switching energy loss ($E_{ON} + E_{OFF}$) to the current has defined as a switching loss factor ($K_{IGBT}(i_C)$) which can be approximated by a third-order polynomial curve fitting graph as also presented in Figure C.7.

$$K_{IGBT}(i_C) = \frac{E_{total}}{i_C}[\frac{\mu Ws}{A}] = 0.0001487 \times i_c^3 - 0.03366 \times i_c^2 + 3.224 \times i_c + 170.3 \tag{C.14}$$

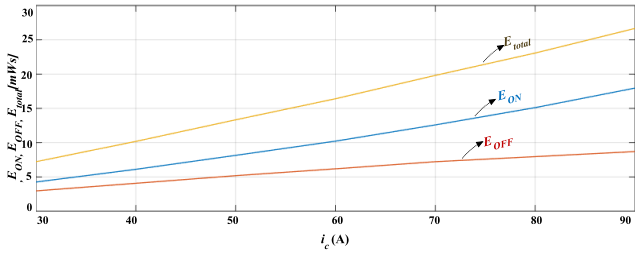


Figure C.6: Device-switching energy loss characteristic graphs of the SKM75GB123D-IGBT switch depend on collector current i_c

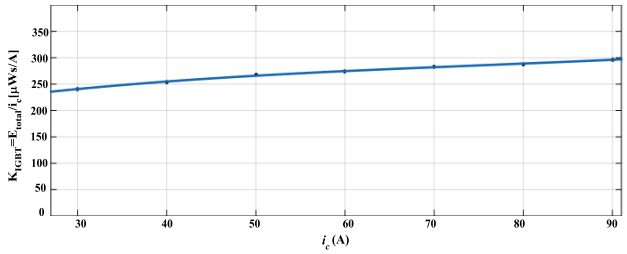


Figure C.7: The parameter $K_{IGBT}(i_C)$ for a given maximum junction temperature (T_{max} = 125°C)

C.1.2.2 Switching loss factor calculation for the anti-parallel diode

The diode turn-on energy losses are negligible so that only turn-off energy losses are considered. The diode turn-off energy loss concerning the forward current i_f is shown in Figure C.8. Herein, considered R_G = 24 Ω from the data-sheet and proceeded the above-defined steps to find the switching factor K_D. Now, the final expression is

derived and described in (C.15).

$$K_D(i_f) = \frac{E_{OFF}}{i_f}[\frac{\mu Ws}{A}] = -0.00077266 \times i_f^2 - 0.0436 \times i_f + 65.53 \tag{C.15}$$

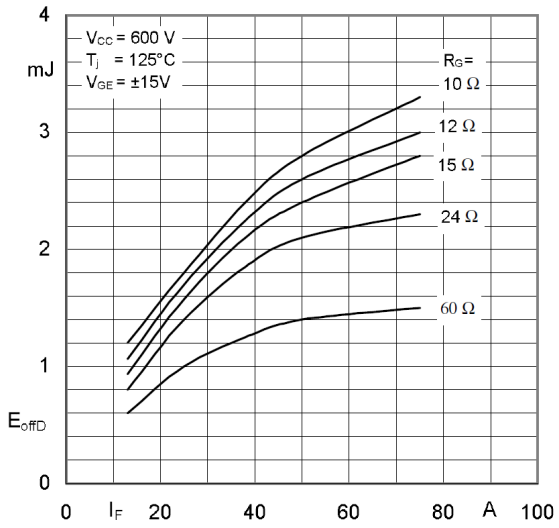


Figure C.8: Diode turn-off energy dissipation per one switching. (image curtsy: Semikron)

C.2 Capacitor loss calculation

Losses in capacitor occur due to the voltage ripple and internal-resistance of it. The ripple loss occur due to the difference between the reference voltage and capacitors' voltage while charging (Taghvaie et al., 2018). Therefore, the capacitors' voltage ripple, ΔV_{C_n} can be given as

$$\Delta V_{C_n} = \frac{1}{C_n} \int_t^{t'} i_{C_n}(t)dt. \tag{C.16}$$

Here, i_{C_n} is current through the n^{th} capacitor during $[t, t']$ interval which can be attained from Table 2.2. Thus, Capacitors' ripple loss ($P_{C_{rpl}}$) in terms of fundamental

frequency (f_{ref}), capacitance and ripple voltage can be expressed as

$$P_{C_{rpl}} = \frac{f_{ref}}{2} \sum_{n=1}^{3} (C_n \times \Delta V_{C_n}^2) \tag{C.17}$$

From (C.16), (C.17), it is evident that the ripple loss is inversely proportional to the capacitor. It means the larger the capacitor value, the higher the overall efficiency is. The total power loss is given as

$$P_T = P_{igbt}(i_C, T) + P_D(i_f, T) + K_{IGBT}(i_C) + K_D(i_f) + P_{C_{rpl}} \tag{C.18}$$

Appendix D

DESCRIPTION OF EXPERIMENTAL PLATFORM

This chapter describes the experimental setup and software used to implement the developed control strategies and a detailed description of the laboratory prototype.

D.1 Overview of the experimental platform

The generalized block diagram representation of the developed low-power experimental prototype is shown in Figure D.1. The OP4200 controller is employed which performs the control computations programmed through Matlab/Simulink. The experimental setup comprises of the following main units:

- A high performance computer for rapid-prototyping and real-time control
- OPAL-RT OP 4200 to interface driver board and computer run the program developed, control signal generation and communicating with the PC
- Interfacing cards (Isolations, dead band circuit, etc.)
- Power circuit board (IGBTs and gate drivers)
- DC voltage source
- Voltage and current measuring probes
- Load box

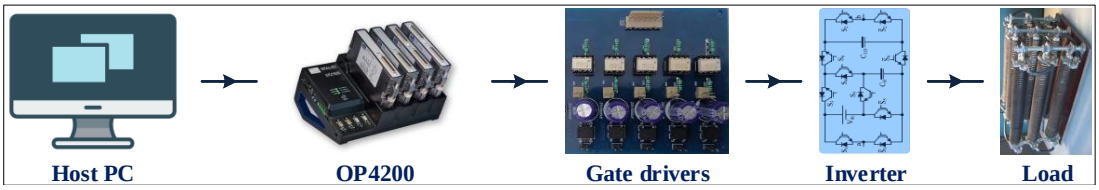


Figure D.1: Platform of the experimental setup

D.2 OPAL-RT OP4200 simulator

OPAL-RT OP4200 controller is designed to enable a rapid prototyping and real-time simulation of various engineering applications. It provides a real-time interface for connecting the external devices to the processor inbuilt. It is a full-fledged control system based on a Motorola Power PC MPC8240 processor with dual core, 64-bit floating point processor, and on-chip peripherals clocked at 1 GHz. The user has the flexibility to develop the desired model using Simulink which is further compiled for generating the appropriate C-code. The C-code so generated is dumped into the DSP controller. In the present work, the simulator has been used as the controller to provide the experimental switching signals. The following are the key specifications of the OP4200 control board:

- ARM® Cortex® A9 CPU - dual core, Xilinx Zynq® FPGA Kintex 7 125K LUT
- 1024MB DDR3L SDRAM
- CPU clock: 1 GHz
- Digital input: 32 channels, 4.5V to 50V, 40 ns typical propagation delay
- Digital output — 32 channels, 5V to 30V, 65 ns typical propagation delay
- Analog input — 16 channels, 16 bits, 500 kS/s, +/-20V, adjustable range
- Analog output — 16 channels, 16bits, 1 MS/s, +/-16V

D.2.1 Steps to execute MATLAB model through OP4200

D.2.1.1 Required settings to the system

- To call Opal-RT library files, run the **setRtLabPath.m** file in MATLAB from C:\OPAL-RT\RT-LAB\v11.2.2.108\common\bin\setRtLabPath.m.

- Copy the **.bin** file from C:\OPAL-RT\RT-LAB\v11.2.2.108\Examples \IO \Opal-RT \OP4200\ Generic_Serie_1GHz\models\OP4200_Generic_Integration_1GHz to the folder of **.mdl** file.
- In **.mdl** file, rename Plant and\or Controller's subsystem as SM_XYZ, & Scope/ Output's subsystem as SC_XYZ.
- Card pins: 1 - 17 are +ve; 20 - 36 are -ve.
- A supply of 5V DC should be provided to pins 18(+), 37(-) to digital output card (in case of use)
- Turn OFF windows firewall of the hosting PC.
- Set IP address: **192.168.10.100** and sub net mass: **255.255.255.0** (Network and internet settings - Ethernet - Change adopter options - Properties - Internet protocol version 4)
- To check whether host PC connected to the OPAL-RT controller or not, give command through run: **ping 192.168.10.101 -t**

D.2.1.2 Procedure to execute

- Once getting reply from the controller, go to OPAL-RT. If pre-created target is exists, use existed one or else create a new target (let's name TAR) with IP address **192.168.10.101**
- Create new project (let's name PRO in this case), right click on the PRO - add existing model - import from files (after importing **.mdl** file + **.bin** file only)
- Click on Edit & check configuration parameters of .mdl file (uncheck block reduction in MATLAB - Model configuration - Optimization and uncheck Signal storage reuse in MATLAB - Model configuration - Optimization - signals and parameters)(Single task)
- Click on SET & select petalinux (ARMv7-based) as target platform.
- Click on Build
- Click on assign - turn ON petalinux & choose TAR

- PRO - I/Os - new - new I/O - select OPAL-RT board - finish
- PRO - Simulation - Rebuild all
- PRO - I/Os - OPAL-RT board - Select bit stream configuration (1-AX-0001-3-11-60_eHSgen3_with _IOs-33-19) - select associated subsystem (SM_XXX)- enable corresponding output (Analog/Digital) - Save the changes.
- Drag output ports **from** PRO - model - ABC - OpInputs & OpOutputs - OpOutput **to** configuration - I/Os - OPAL-RT board - Slot (Analog\Digital) - (Channels 0 - 7)
- Go to Set & check the target platform
- Load & execute the model

D.3 The peripheral interface circuit board

Power electronic switches exhibit a finite delay time during switching ON and OFF. Thus, it is essential to introduce a short dead time termed dead-band among the power switches constituting a leg or the switches whose simultaneous switching ON leads to the shoot-through condition. The required dead band can be generated in many ways, like analog-based, dedicated digital circuits. In this work, a digital circuit with passive components based dead-band generator is developed. The minimum dead band required for the selected IGBT (SKM75GB123D) with a rating of 1200 V and 75 A is given as (Xi, 2007)

$$t_{db} = [(t_{d,Off,Max} - t_{d,On,Min}) + (t_{pdd,Max} - t_{pdd,Min})] \times 1.2 \tag{D.1}$$

where, $T_{d,Off,Max}$ = the maximal turn-off delay time (D.2)

$T_{d,On,Min}$ = the minimal turn-on delay time (D.3)

$T_{pdd,Max}$ = the maximal propagation delay of the driver (D.4)

$T_{pdd,Min}$ = the minimum propagation delay of the driver (D.5)

1.2 = safety margin (D.6)

Referring to (Toshibha, 2019) and (Semikron, 2009), the minimum value of t_{db} is computed to be

$$t_{db} = [(380 - 44) + (500 - 150)] \times 1.2 = 823.2 \text{ ns} \tag{D.7}$$

The values of R_d and C_d is computed using (D.7) as $t_{db} = R_d \times C_d$. Taking the nearest values as 100 Ω and 10 nF results in a dead band of 1 μs. The value of the input resistance or buffer resistance (R_b) is computed using the forward current (I_F), input forward voltage (V_F) and "H" level pulse (V_H) as $R_b = \frac{V_F - V_H}{I_F} \approx 1$ kΩ.

Gate drivers are an essential part of the power circuit and are responsible for providing the required source and sinking current of the gate to the source capacitance of the power switch. Since the prototype is built by utilizing multiple semiconductor switches, the grounds of all the gate drivers are isolated to avoid a short circuit. Regarding this, a multi-winding transformer with one input and multiple output ports is used. The value of R_{gs} is calculated to limit the maximum output current of the driver IC to a safe value, i.e., 1.5 A for TLP250. Hence, the computed value of $R_{gs} = \frac{15}{1.5} = 10$ Ω. Each SKM75GB123D module houses two IGBTs in series. This module facilitates the realization of any MLI topology (motto of this work) smoothly with a minimum effort to make suitable external connections using connecting wires. The GW INSTEK GDP-025 high voltage differential Probes and CC-65 current clamping meter are employed for sensing the voltages and currents, respectively. The overall hardware setup with other associated units is shown in Figure D.2.

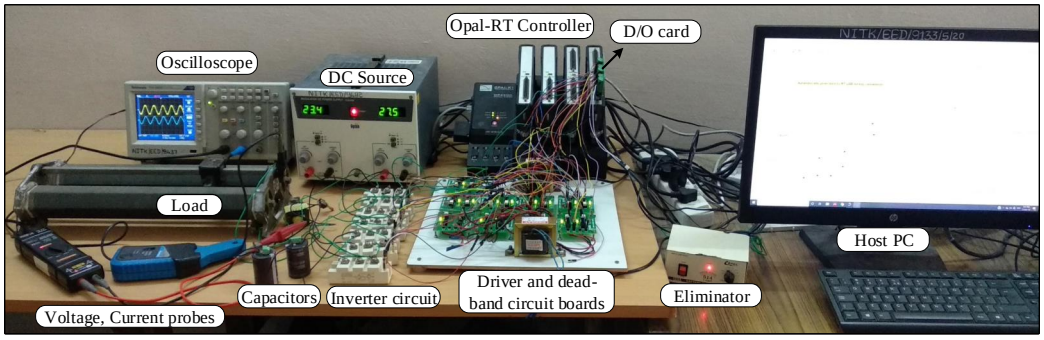


Figure D.2: Laboratory setup

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Publications based on the thesis

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