INVESTIGATION ON MULTI-CELL AND HYBRID MULTILEVEL INVERTERS WITH MINIMUM NUMBER OF DC SOURCES

Thesis

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DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled Investigation on Multi-cell and Hybrid Multilevel Inverters with Minimum Number of DC sources which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to *certify* that the Research Thesis entitled Investigation on Multi-cell and Hybrid Multilevel Inverters with Minimum Number of DC sources submitted by J Venkataramanaiah (Register Number: EE15F02) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

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Abstract

From the energy saving perspective, it is essential to adopt highly efficient DC to AC conversion (inverter) system for high power and medium voltage applications. Indeed the conventional two-level inverters cannot handle high power system unless series/parallel arrangements of semiconductor switching devices are used. However, these reformations have severe problems such as misfiring the gating pulses, voltage unbalances between the series connected devices and so on. Again to get rid of these problems, large snubber capacitors and resistors (passive elements) are connected to each switch for compensating transient voltages and static charge balance. Nevertheless, these passive elements cause a higher switching loss and relatively long switching time. On the other hand, total harmonic distortion of the output voltage waveform of traditional two-level inverters is one of the severe problems as the power ratings of the devices goes high. In this critical situation, the multi-level inverters (MLIs) are successfully introduced to overcome all the issues as mentioned earlier for medium and high power applications.

Ever since the inception of MLIs, cascaded H-bridge (CHB), neutral point clamped (NPC) and flying capacitor converters are among the earliest topologies that are deemed to be well-established. Each of them has advantages and disadvantages. An NPC-MLI requires additional clamping diodes for its extension whereas, CHB-MLI and flying capacitor MLI needs many isolated DC sources to generate a multistep output and multiple capacitors respectively. Since then, many derivatives and refinements to these classic topologies have been proposed. The motivation for this research work stems out from the demand to generate a substantial number of voltage levels while keeping the device count as low as possible. Therefore, by taking advantage of the basic MLI configurations, a few schemes emanating as a result of combining two or more MLIs in part or fully, referred to as hybrid MLIs are proposed. The offered solutions exhibit considerable topological improvements with reduced control complexity.

In the present thesis, we have mainly concentrated on designing a novel hybrid multilevel inverter which can provide an inbuilt isolation for grid-

connected, FACTS devices and standalone applications. This MLI can attain nineteen level output waveform with only 12 semiconductor switches. Moreover, it can be extended to n number levels where the switch count is further reduced enormously. In addition to that, a new PWM switching technique is introduced to refine the harmonic profile of the proposed MLI'output voltage waveform. The new PWM can efficiently operate at a very low switching frequency. Thereby, the switching losses of the proposed configuration are minimised drastically.

Later, we have kept consistent efforts to derive a new power circuit from our first proposed configuration. Herein the device count is further reduced from 12 to 10 switches to produce the same nineteen level output waveform. In addition to that, an innovative controlling approach is implemented which is a simple fundamental switching strategy so-called 'FSQS'technique. Moreover, the switching technique can achieve the least harmonic distorted output voltage waveform, and it can be applied to any topology and 'n'number of output levels.

On the other hand, motor drive applications always prefer the efficient MLIs without any transformer involvement in their structures. In fact, most of the power drives are still running with traditional MLIs where the part count is a significant limitation. Thereby we designed a new MLI topology which can attain the modularity with less circuit complexity. It has been named as a multi-cell MLI where the power cell is built asymmetrically. In fact, the part count of the proposed configuration is an appreciable rate compared to the traditional and recent MLIs for the equivalent level generations.

In the end, the thesis is devoted to design three unique configurations and two new modulation techniques to address the full range of MLI applications. All developed configurations and schemes are simulated extensively in MATLAB/Simulink. After that, the topologies are verified experimentally by advanced DSP controller and OPAL-RT (Real Time) Simulator on a prototype setup for recording the corresponding output voltage, current, and the THD results.

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List of Abbrevations

AC	Alternating Current
ACHB	Asymmetrical Cascade H-bridge
APOD	Alternative Phase Opposition Disposition
CHB	Cascade H-bridge Inverter
CMLI	Cascaded Multilevel Inverter
CRNGO	Cold Rolled Grain Oriented
D	Diode
DC	Direct Current
DC-MLI	Diode Clamped Multilevel Inverter
FC	Flying Capacitor
FFT	Fast Fourier Transform
FSQS	Fundamental Sine Quantised Switching Technique
GTO	Gate Turn-off Thyristor
HMLI	Hybrid Multilevel Inverter
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated-Gate Commutated Thyristor
LS-SPWM	Level Shift Sinusoidal Pulse Width Modulation
MLI	Multilevel Inverter
MOB	Multi Output Boost
MV	Medium Voltage
MVR	Maximum Voltage Ratio
NLC	Nearest Level Control
NPC	Neutral Point Clamped
NR	Newton Raphson
p	Number of Basic Cells per Phase
PD	Phase Disposition
PIV	Peak Inverse Voltage
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
Q	Quantisation Interval
SCHB	Symmetrical Cascade H-bridge
SHE	Selected Harmonics Elimination

SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
Tr	Transformer
VA	Volt Ampere
VSI	Voltage Source Inverter
V_{CE}	Voltage Drop Across the Collector and Emitter Terminals of the IGBT
V_{GE}	Voltage Drop Across the Gate and Emitter Terminals of the IGBT
i_C	Collector Current of the IGBT

Chapter 1

INTRODUCTION

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1.1 Introduction

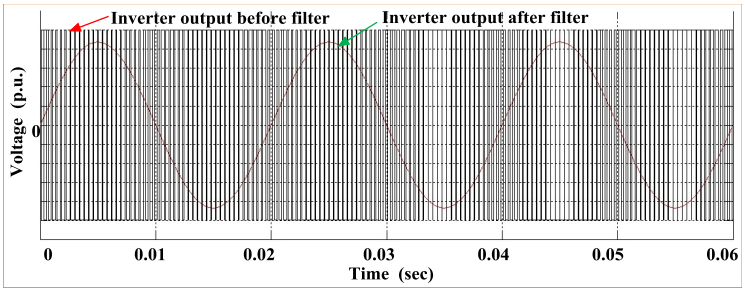
The current chapter presents an introduction to the thesis, including research background, technical and physical features of the traditional multilevel inverters. Following a critical review on newly configured multilevel inverters, and features of the existing control techniques are presented. In the end, the research objectives and organisation of the thesis are included.

1.2 Research background

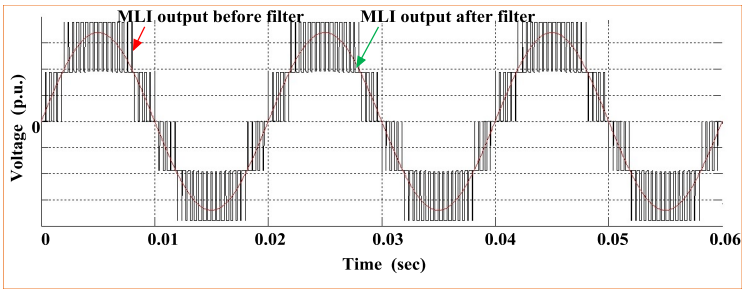
The increasing demand for electrical energy has been harshly depleting the fossil fuels in worldwide. In fact, two prominent ways are observed in the literature to increase the life of fossil fuels for the future generations. Primarily, the existing energy resources have to be utilised efficiently. Secondly, government and private sectors should come front to provide financial and technical support for the renewable energy resources (photo-voltaic, geothermal energy, wind and nuclear power) to generate the electrical power. Technically, when the power converters run at high efficiency, then the power consumption comes down. However, the two-level inverter can generate only a square waveform at its output terminals where the large size filters are required to improve the quality of waveform by suppressing the harmonics. Therefore it cannot be an optimal solution to the high power conversion systems, though, the semiconductor switches are arranged in a series/parallel combinations. Under these circumstances, identifying a suitable solution for medium voltage and high power applications become easy by adopting the multilevel inverter. The traditional inverter (two-level) and multilevel waveforms are depicted in Figure 1.1.

1.3 Technical and physical features of the traditional multilevel inverters

In the late 1980s, a novel configuration (Nabae et al., 1981) is introduced to do the same function where the normal two-level inverter has been doing for long years, i.e., treated as a first multilevel inverter. The characteristics like handling high magnitude voltages with reduced device stresses, fewer power losses (both switching and



(a)



(b)

Figure 1.1: Typical output voltage waveforms: (a) Traditional two-level inverter voltage waveform, (b) Multilevel inverter voltage waveform.

conduction losses), improved power quality by synthesis ac voltage from several different voltage levels on the DC bus. These are the main reasons for their widespread acceptance in all possible industrial applications. In fact, any MLI can be configured with a combination of input capacitors, isolated DC voltage sources, power semiconductor devices, inductors and transformers to create a multistep output voltage waveform with variable and controllable amplitude, frequency and phase (Rodriguez et al., 2002). A few such arrangements are considered as the classical MLIs and discussed briefly as under.

1.3.1 Diode clamped multilevel inverter (DC-MLI)

A DC-MLI is essentially composed of two traditional 2L inverters stacked one over the other and are fed by series connected capacitors (Nabae et al., 1981). The clamping diode needs different voltage ratings for different inner voltage levels. The DC-MLI is also called 'neutral point clamped (NPC) inverter', because the mid-voltage level is defined as the neutral point level. A 5L three-phase power circuit configuration is shown in the Figure 1.2. In fact, only half of the total switch count required

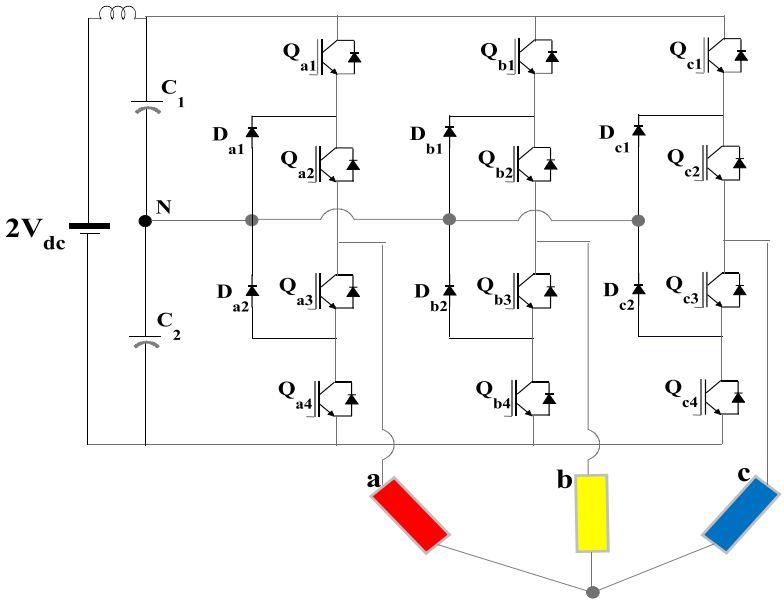


Figure 1.2: Circuit configuration of 5L DC-MLI.

unique triggering pulses, whereas the remaining switches receive inverted gate signals to avoid the DC-link short circuit. In addition to that, the DC-MLI can be extended to higher power rating and more output voltage levels by adding additional power switches and clamping diodes. As the number of output voltage levels increases, the required number of clamping diodes increases dramatically. Thereby, a complex control system is required to control the DC-link capacitor unbalance, which hindered the application of the DC-MLI to a higher number of levels (> 5) by the industries. However single DC supply is one of the biggest assets of this structure for n number of levels.

1.3.2 Flying capacitor multilevel inverter(FC-MLI)

The FC topology is slightly similar to the DC-MLI, with the main difference that the clamping diodes are replaced by flying capacitors(Meynard and Foch, 1992),as shown in Figure 1.3. Similar to a DC-MLI, it also requires only two gating pulses per leg. However, the complementary device positions are not the same. In comparison to a DC-MLI, FC has a modular structure which enables its extension to a higher number of levels effortlessly. This also adds an extra degree of freedom to control the converter with the help of many available redundant states. But the load is

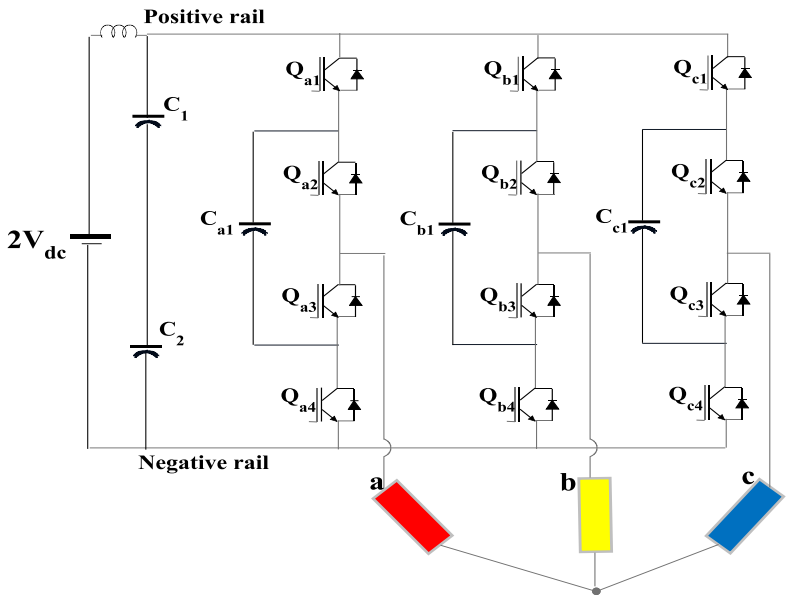


Figure 1.3: Circuit configuration of 5L FC-MLI.

not directly connected to the neutral of converter to create zero voltage level in FC configuration. Thereby the zero level is attained by connecting the load to either positive or negative rail through the flying capacitor and polarity could be the opposite with respect to the DC link.

1.3.3 Cascaded H-bridge multilevel inverter (CHB-MLI)

A CHB-MLI is devised by connecting two or more 5L Three-phase H-bridge inverters as shown in Figure 1.4 (Hammond, 1995). Each H-bridge can generate three different voltage levels ($0, V_{\mathrm{dc}}$, and $-V_{\mathrm{dc}}$). The output voltage is synthesised by adding each of the isolated DC voltage sources resulting in the generation of a stepped output voltage with a step size of value equal to the magnitude of the connected DC sources. It is one of the highly regarded MLI as far as modularity, device count, and scalability are considered. Furthermore, soft switching techniques can be used to reduce switching losses and device stresses. The three traditional converters have unique features and challenges. Moreover, adopting a suitable control technique plays a vital role in the quality of the multilevel waveform (Rodriguez et al., 2009, Malinowsk-Gopakumar et al., 2010, Leon et al., 2011). All these factors attract a wide-range applications such as traction (Stynski et al., 2009), power-quality devices (Varschavsky et al.,

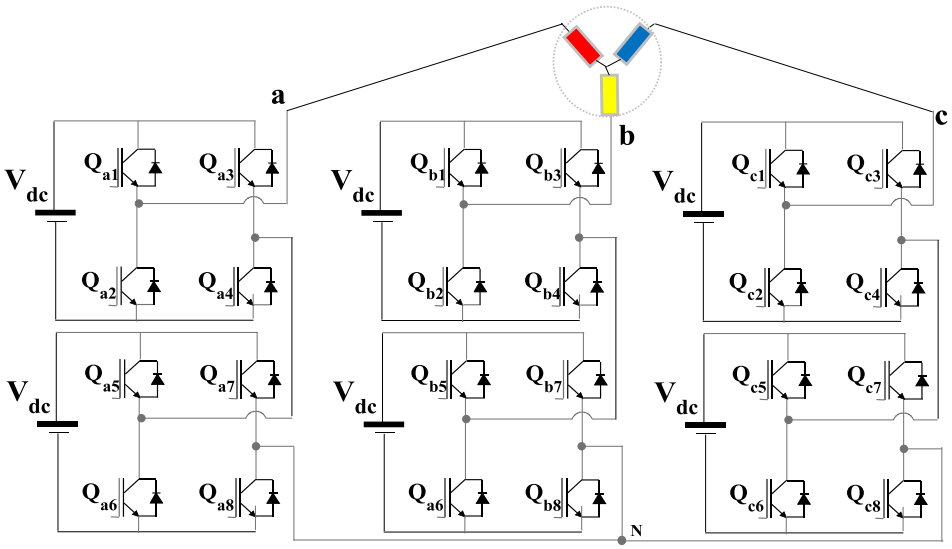


Figure 1.4: Circuit configuration of 5L CHB-MLI.

2010), renewable energy utilisation (Islam et al., 2014), energy transmission (Nami et al., 2015), automotive (Pereda and Dixon, 2012), uninterruptible power supplies (Cortés et al., 2009), industrial drives (Rodriguez-Bernet, 2007), mining (Kouro et al., 2007b), marine propulsion (Apsley et al., 2009), MRI systems (Sabate et al., 2004) and so on.

1.4 Investigation on recently examined MLI configurations

1.4.1 Symmetrical MLIs

When all the isolated DC sources have the same magnitudes to the multilevel inverter, then that will be treated as a Symmetrical MLI (SMLI). Over the years, tens of the SMLI community topologies are proposed in the literature. Initially, the authors(Mcmurray, 1971, Marchesoni et al., 1990) attempted to connect two H-bridges in series for producing five level stepped waveform, and it has become famous for high-frequency and low-voltage applications (Hammond, 1995). The present subsection gives priority to expose well established symmetrical structures and their characteristics regarding device count, cost, modularity, and redundancy in voltage

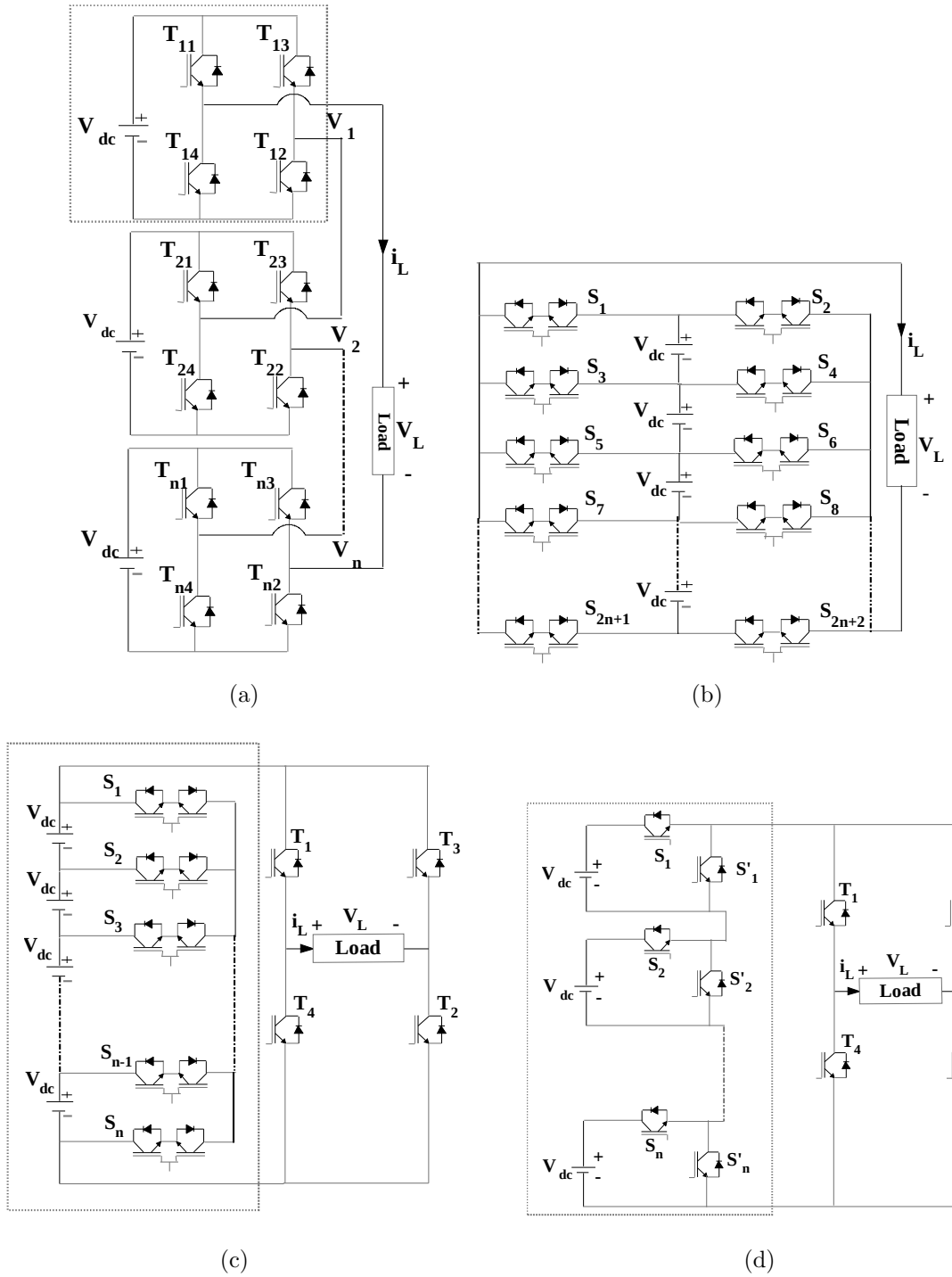
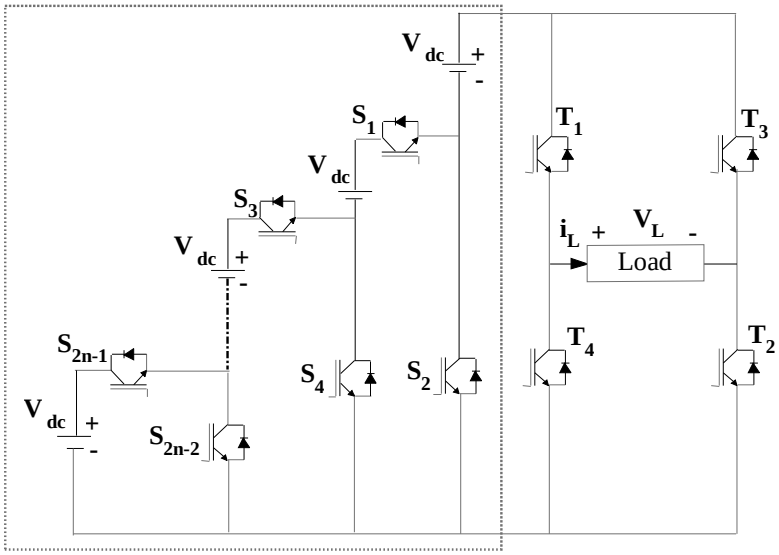


Figure 1.5: (a) Symmetrical CHB-MLI, (b) Common emitter bidirectional switch based MLI, (c) Reduced bidirectional switch based MLI, (d) Unidirectional switch based MLI.

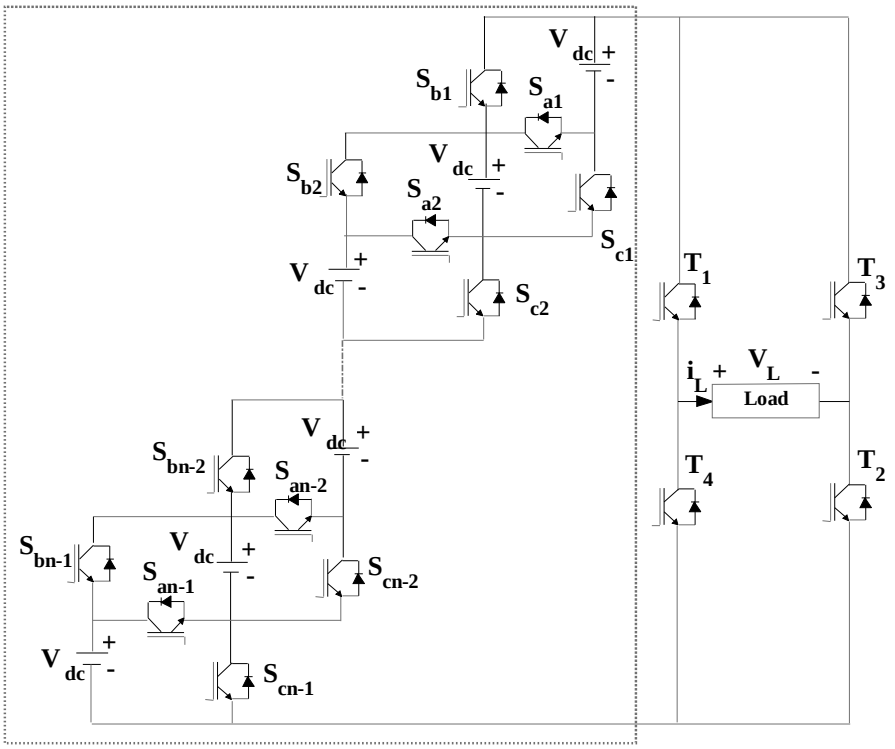
vectors.

All SMLIs are originated from the CHB-MLI (Lai and Peng, 1996) which is shown in Figure 1.5(a). Structurally, equal input magnitudes of the H-bridges are connected in series where the control and protection units of H-bridges became modular for reducing the manufacturing costs. Further, the number of load voltage levels depends on the number of DC sources given by the following equation: $N_L = 2N_{DC} + 1$. In fact, the MLI has been installing medium voltage rating switches to accomplish high voltage waveforms since the cost of the inverter always compromises the switch ratings. Furthermore, the redundant states of the CHB-MLI made to approve of doing the program fault tolerant operations in telecommunication systems, production environments, transportation systems, and medical systems (Franquelo et al., 2008). On other hands, CHB cannot be recommended for adopting LS-PWM technique (Khomfoi and Aimsaard, 2009), and also its installation space and control complexity increases due to rising in the device count for higher output levels.

Next, (Babaei et al., 2007) proposed a new MLI for the dynamic voltage restorer (DVR) applications is shown in Figure 1.5(b). The basic cell of the topology is a composite of an input DC source and four quadrant switching components. Each power cell can generate three levels. However, it does not have the potential to create more levels than Figure 1.5(a) with limited IGBT switches since the two switches are internally arranged in the common emitter configuration. In addition to that the topology not suited for fault-tolerant applications due to lack of redundant states. Afterwards (Babaei, 2008) proposed a new topology with reduced bidirectional switches as shown in the Figure 1.5(c). It is composed of two separate parts. One is level generated part, and another one is polarity part. The level part can only create positive and zero voltage levels while the polarity generator gives full load voltage waveform with simple H-bridge. On the contrary, the presented topology cannot be extended to higher voltage magnitude levels, because the switches in polarity part are not able to withstand the sum of all DC voltage magnitudes. Subsequently, (Babaei and Hosseini, 2009) suggested an advanced topology with only unidirectional switches as shown in the Figure 1.5(d) for medium voltage commercial applications like uninterrupted power supplies. Herein basic power cell builds with only one DC source (equal to V_{dc}), and two unidirectional power switches S_1 and S_2. Nevertheless, abnormal voltage stress among the switches results in loss of modularity. These issues play an important role in the cost and realisation of the inverter. The recommended topology by (Choi and



(a)



(b)

Figure 1.6: (a) Prior H-bridge cell based symmetrical MLI, (b) A single-phase MLI using switched series/parallel DC voltage sources.

Kang, 2009, Lee and Kang, 2008) is displayed in Figure 1.6(a). It is so called 'prior H-bridge cell-based multilevel inverter'. Herein, level created part has smaller switch count for the same applications. But, the level part cannot provide all individual DC input magnitudes across output terminals. Therefore, it fails to provide equal load sharing and also not recommended for asymmetric configurations. (Hinago and Koizumi, 2010) proposed a topology where the DC sources are switched to series and parallel combinations as shown in Figure 1.6(b). Design-wise, it has enough flexibility to share the load among input sources and synthesises output levels by activating very few power switches for meeting electric vehicle drive applications. The significant limitation is that a zero voltage cannot be synthesised with level part of the circuit and polarity region is no longer operated in fundamental switching frequency. Thereby, all existed modulation techniques cannot be adaptable for controlling this configuration.

Authors (Waltrich and Barbi, 2010) introduced a novel configuration based on the synthesis of power cells from two inverter legs which are connected in series as shown in Figure 1.7(a). Each power cell in the circuit employs two isolated DC voltage sources and switches with half power ratings. An extra DC supply is the only difference between the CHB-MLI and the proposed configuration, remaining all the feature of the CHB-MLI has existed in the topology. Thereby, it is considered as an alternative for CHB-MLI applications. Although author developed a three-phase version, it can also be realised in a single-phase system. Later on, (Kangarlu et al., 2012) suggested a new topology exhibited in Figure 1.7(b) which can be obtained all positive and negative levels and extended to n number of levels. The fundamental frequency switching technique is implemented to control the topology. Further, in the multi-level unit, only two switches are unidirectional and remaining switches are bidirectional. Therefore, the number of gate drive circuits is low, as compared with the aforesaid symmetrical topologies, except the Figure 1.7(b) topology where the same number gate drive circuits existed. Next, (Babaei et al., 2012) came up with a modified symmetric structure as shown in Figure 1.7(c). The configuration structurally has two parts, the part-1 creates only positive levels of the load voltage waveform (i.e., level creator), and the part-2 adopts a simple H-bridge whose switch ratings are excessive for producing the negative polarity waveform (i.e., polarity generator). The part-1 switches assembled such a way that input DC supplies should be disjoined with each other. Later on, (Ebrahimi et al., 2012) suggested a novel modular MLI as shown

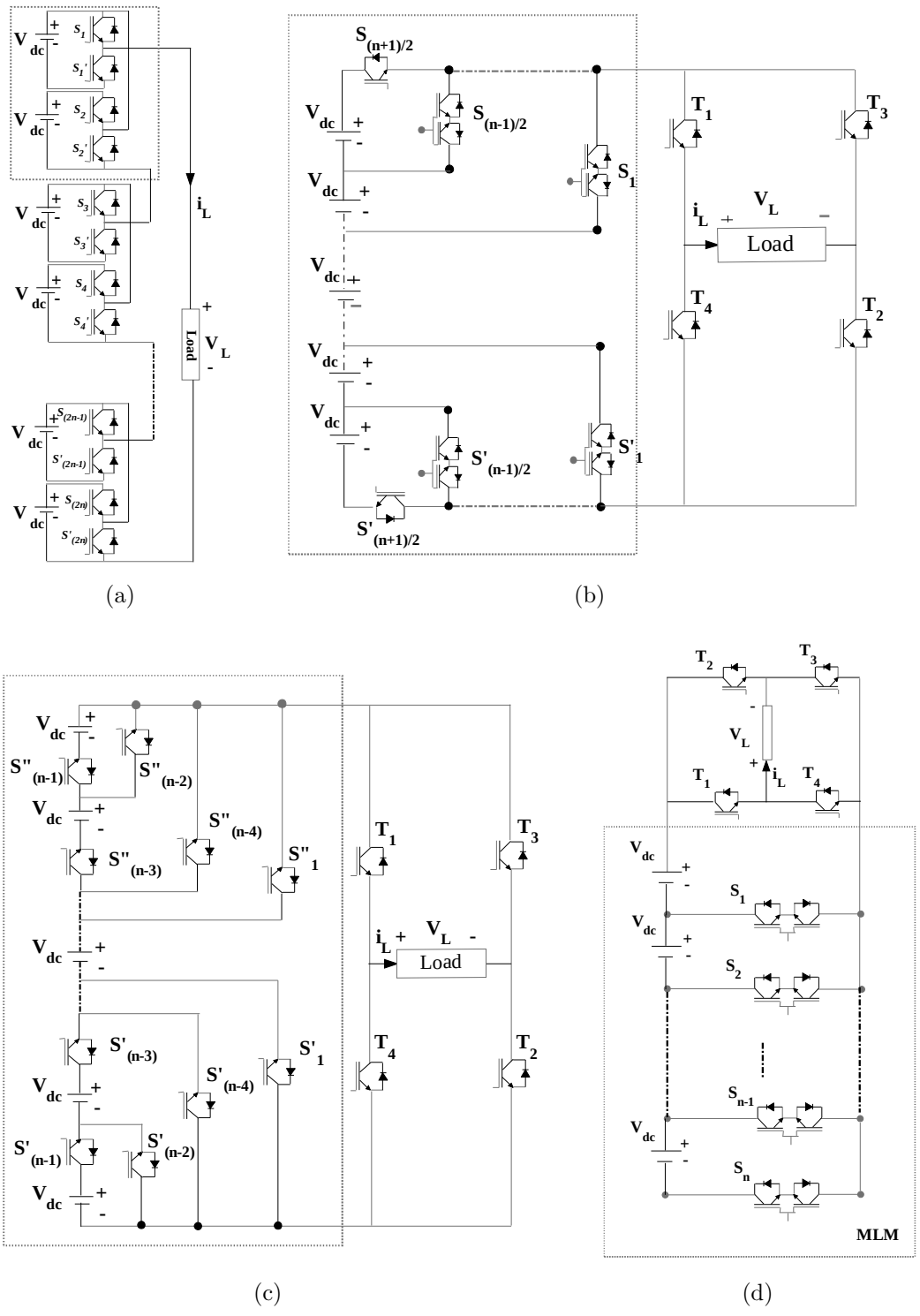


Figure 1.7: (a) Symmetrical MLI using power cells with two inverter legs in series, (b) Symmetrical MLI with reduced power components, (c) Symmetrical MLI using only unidirectional switches, (d) Symmetrical modular MLI.

in Figure 1.7(d). Though the circuit structurally imitates working principle of the above-said topology, the level creator is a unique arrangement which is a unification of four-quadrant switches and isolated DC sources. The presented topology is free from nonuniform voltage stresses by employing four-quadrant switches. Nevertheless, an equal load sharing among the input DC sources is unattainable due to lack of more switching combinations.

Authors (Kangarlu and Babaei, 2013) found a suitable solution for high voltage application by introducing an innovative topology as shown in Figure 1.8(a), which came under the 'cross switched multilevel inverter family'(Nami et al., 2013, Babaei and Farhadi Kangarlu, 2011). This structure can extend to any number of voltage levels. A strength of the configuration is to incorporate a moderate voltage rating switch to avoid the polarity part of the structure. Similarly, (Liao and Lai, 2011) presented a simplified five-level inverter topology for distributed energy resources-based micro-grid applications which is demonstrated in Figure 1.8(b). In construction point of view, it comprises of floating input DC sources connected in reverse polarities through power switches. In literature, this kind of structures is famous as a cross-connected sources-based multilevel inverter(CCS-MLI). It is constructed with less switch count and low switching losses. However, the authors not attempted to discuss the feasibility of structure to the higher level (more than five levels). Later on (Gupta and Jain, 2012b) introduced a generalised structure for CCS-MLI which can attain any number of output voltage levels, but still, equal load sharing among the input DC sources and fundamental frequency switching are not possible if levels exceed five (Gupta and Jain, 2014). By keeping this in mind, (Alishah et al., 2014) suggested the finest symmetrical structure with least device count, compact size, and cost-effective version. It is shown in Figure 1.8(c). Herein, two parts jointly worked to generate the desired output voltage waveform. Additionally, the switches and power diodes are arranged elegantly. However, it requires different ratings of power switching devices. Next, (Mokhberdoran and Ajami, 2014a) proposed a novel topology shown in Figure 1.8(d). The basic block has six power switches, eight power diodes, and two DC-sources. The number of conducting switches in the current path is lower to attains the lowest power losses.

Next, (Babaei et al., 2015) proposed a new single-phase MLI as shown in Figure 1.9. It is also known as developed cascaded MLI. Herein, an additional dc input source is needed to get the first voltage level (V_1) ought to primary cells were not

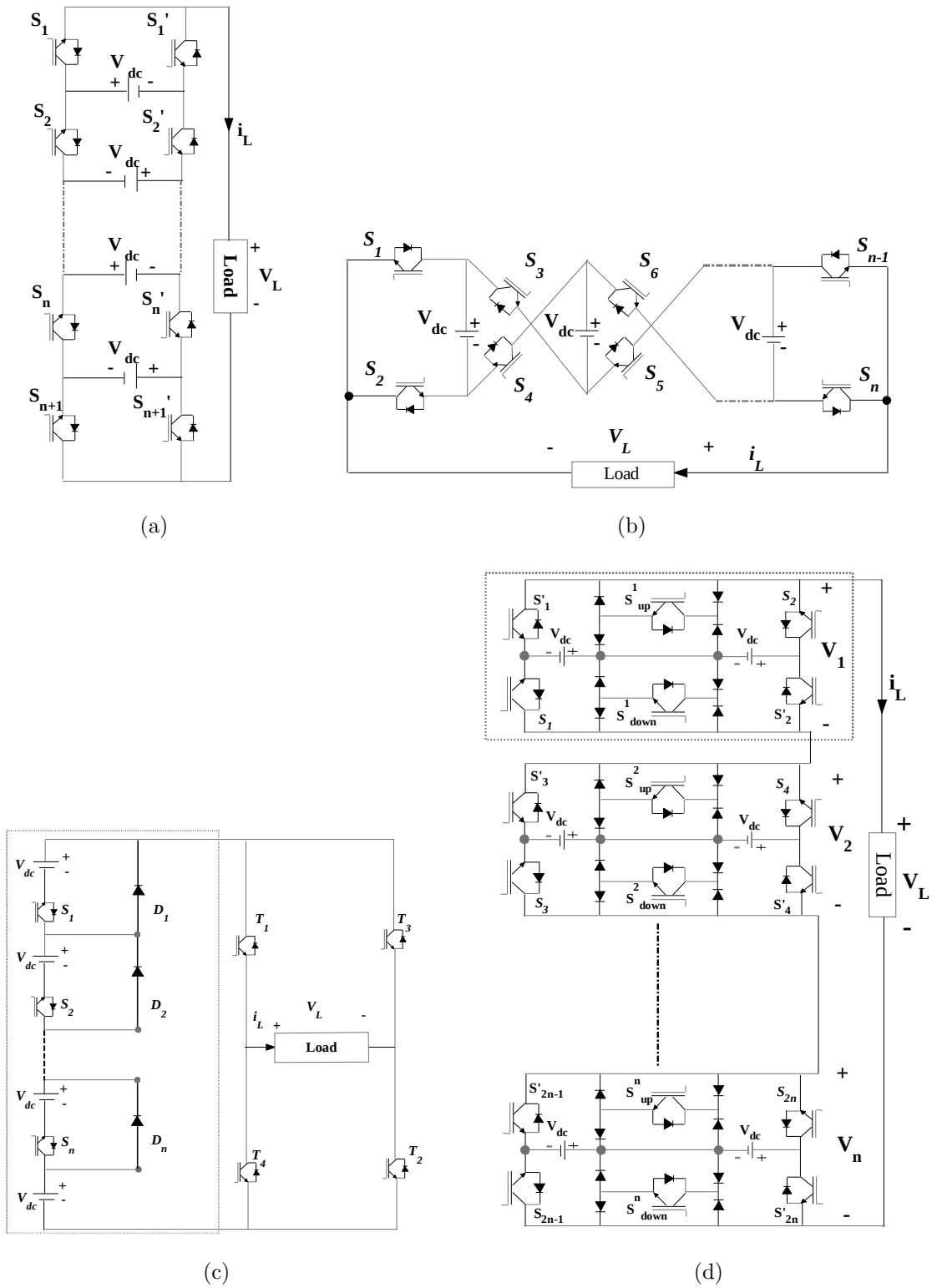


Figure 1.8: (a) Cross-switched symmetrical MLI, (b) Cross connected structure MLI, (c) Symmetrical MLI with lowest number of switches, (d) New cascaded symmetrical MLI.

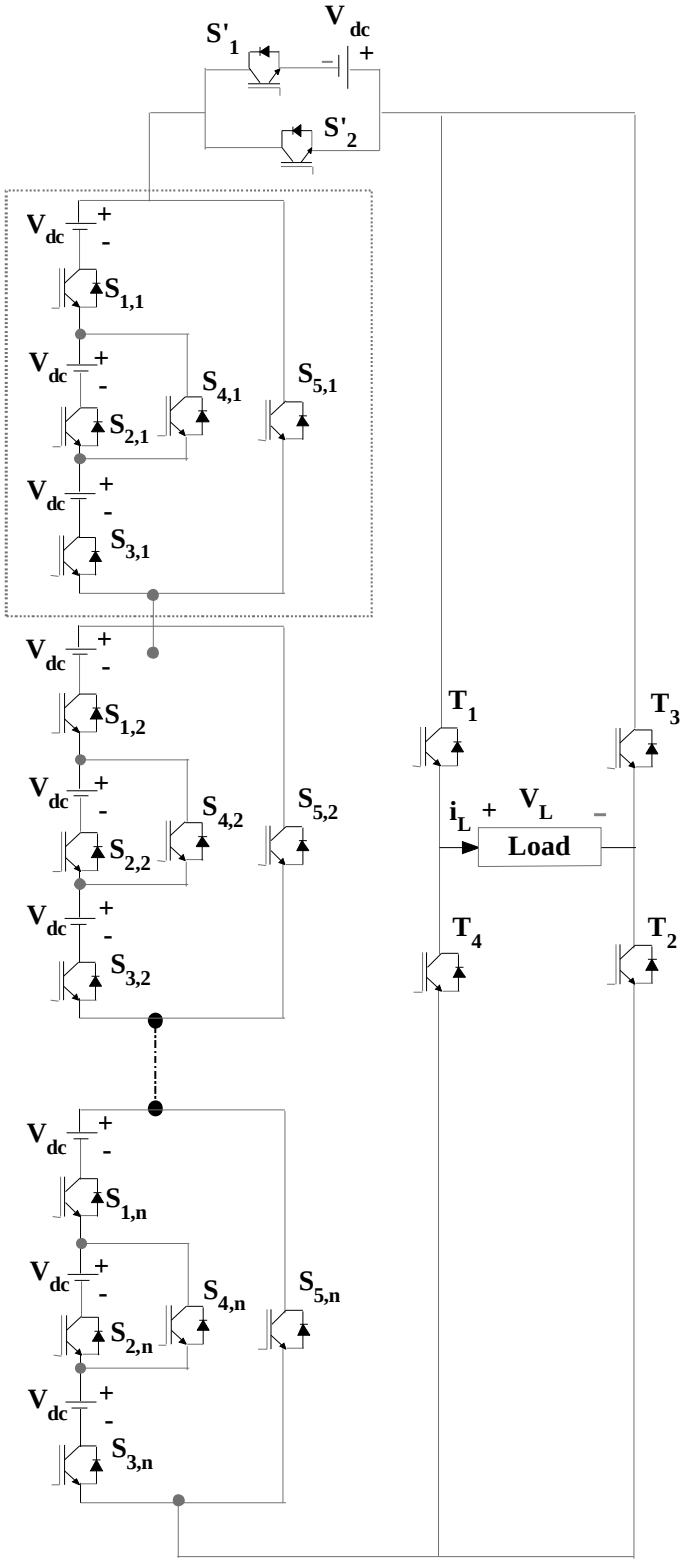
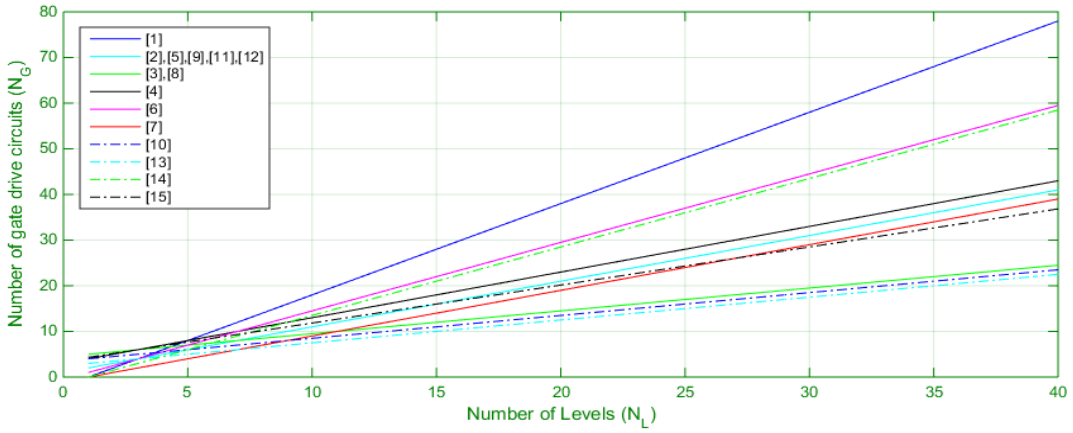


Figure 1.9: Novel structure in symmetrical MLI

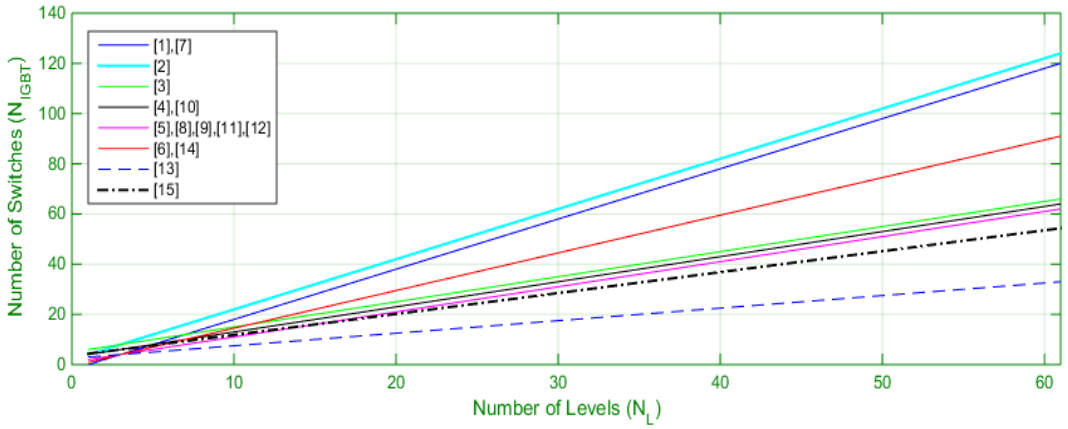
able to create the first output level. The renewable energy sources such as photovoltaic (PV) panels, fuel cells, and energy storage elements (capacitors or batteries) contributes the necessary isolated DC input sources. If these would be the input DC voltage sources, then an each DC source should have a DC-DC converter to balance the voltage magnitudes. If not, the inequalities among them induce an unpredicted harmonics in the output voltage waveform. There is another option to provide the individual DC links by using transformers (Peng et al., 1996).

1.4.1.1 Summary of symmetrical MLIs

The subsection is assigned to analyse the most popular symmetrical configurations. The component-based study for all the topologies are reported in Table 1.1, and a significant investigation of the N_L, N_{IGBT} and N_{DC} is demonstrated in Figure 1.10. From the study of these, we can conclude that the most effective suggested topology is presented by (Alishah et al., 2014), apart from that, the configurations proposed by (Lai and Peng, 1996) and (Babaei et al., 2007) have become the famous circuits when they resolve voltage unbalanced and reduced device count issues. In fact, two configurations described above demanded the highest gate driver circuits, and semiconductor switches respectively as the number of levels moving high.



(a)



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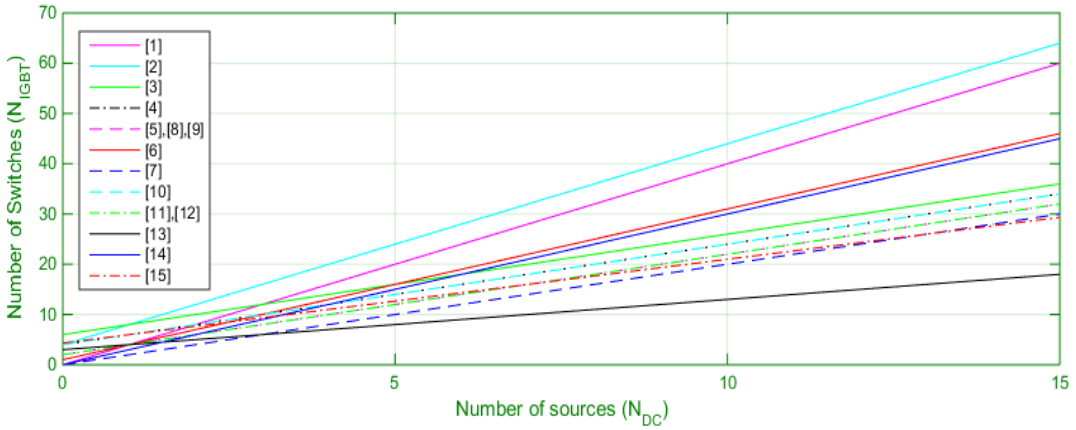


(c)

Figure 1.10: (a) The total number of steps (N_L) versus the total number of gate drivers (N_G), (b) The total number of steps (N_L) versus the total number of switching components (N_{IGBT}), (c) The total number of input DC supplies (N_{DC}) versus the total number of switching components (N_{IGBT}).

Table 1.1: Component details of symmetrical multilevel inverters

	Multilevel inverter type														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N_{DC}	n	n	n	n	n	n	$n = 2p$	n	n	n	n	n	$n = 1 + p$	$n = 2p$	$n = 1 + 3p$
N_L	2n+1	2n+1	2n+1	2n+1	2n+1	2n+1	2p+1	2n+1	2n+1	2n+1	2n+1	2n+1	2p+3	4p+1	6p+3
N_{IGBT}	4n	2(2n+2)	2(n+3)	2(n+2)	2(n+1)	3n+1	2n	2(n+1)	2(n+1)	2(n+2)	2(n+1)	2(n+1)	n+3	3n	(5n+13)/3
N_G	4n	2n+2	n+5	2n+4	2n+2	3n+1	4p	n+5	2n+2	n+4	2n+2	2n+2	n+3	6p	5p+6
$V_{L,max}$	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	$(2p)V_{dc}$	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	$(p+1)V_{dc}$	$(2p)V_{dc}$	$(3p+1)V_{dc}$

1. Lai and Peng (1996)
2. Babaei et al. (2007)
3. Babaei (2008)
4. Babaei and Hosseini (2009)
5. Choi and Kang (2009)
6. Hinago and Koizumi (2010)
7. Waltrich and Barbi (2010)
8. Kangarlu et al. (2012)
9. Babaei et al. (2012)
10. Ebrahimi et al. (2012)
11. Kangarlu and Babaei (2013)
12. Gupta and Jain (2012b)
13. Alishah et al. (2014)
14. Mokhberdoran and Ajami (2014a)
15. Babaei et al. (2015)

1.4.2 Asymmetrical MLIs

As discussed in the 1.4.1 section, an 'n' equal DC voltage magnitudes can offer '$2n+1'$ distinct output voltage levels. However, there are many challenges have to be addressed, for example, the converter size, installation area, cost, and also implementing the control techniques became difficult for higher levels. These significant issues are addressed with asymmetrical topologies in the literature where the all DC source magnitudes of the circuit are not the same. This section is devoted for doing a comprehensive investigation on asymmetrical MLIs regarding structure, charge balancing, modularity, feasibility, and algorithms which can determine magnitudes of DC sources.

Authors (Manjrekar et al., 1998, 2000) had proposed first asymmetrical MLI configuration as shown in the Figure 1.11(a). It is operated with non-identical input DC sources in a binary fashion see in Table 1.2. Thus it is named as binary asymmetrical MLI. Herein, the topology can achieve $2^{n+1}-1$ distinct voltage levels with only 'n'cascaded H-bridges or 'n'individual supplies. In other sense, it shows better performance compared to symmetrical MLI for the same number of switching components and DC buses. Next, (Mueller and Gran, 1998) proposed a single-phase leg for the quasi-linear MLI as shown in the Figure 1.11(b). For a given output voltage, more than one combination of switching states can exist, and voltage levels dramatically increased in this configuration. Additionally, maximum voltage ratio (MVR) is constant despite the output voltage level, leads to getting small MVR for higher levels which is always preferable for better MLI.

After a period of time, (Lai and Shyu, 2002) introduced a trinary MLI shown in Figure 1.11(c). It attains more output levels than the configurations as mentioned earlier for achieving a better quality of output voltage waveform and the corresponding selection of input DC sources is described in Table 1.2. In practical, the MVR is getting unreasonable because of high input DC magnitudes. The high DC values mainly rise the power ratings of the rest of devices and the voltage imbalance also exists due to the different selection of input values. However, the power devices are operated at the lower switching frequency to diminish the switching losses in this configuration. Next, (Babaei et al., 2007) came up with a new asymmetrical topology which is depicted in Figure 1.11(d). There, the circuit was operating with a new algorithm which can determine the DC voltage sources as shown in Table 1.2, and it attains n^2+n+1 output voltage levels by suitable toggling of switches for 'n'unequal

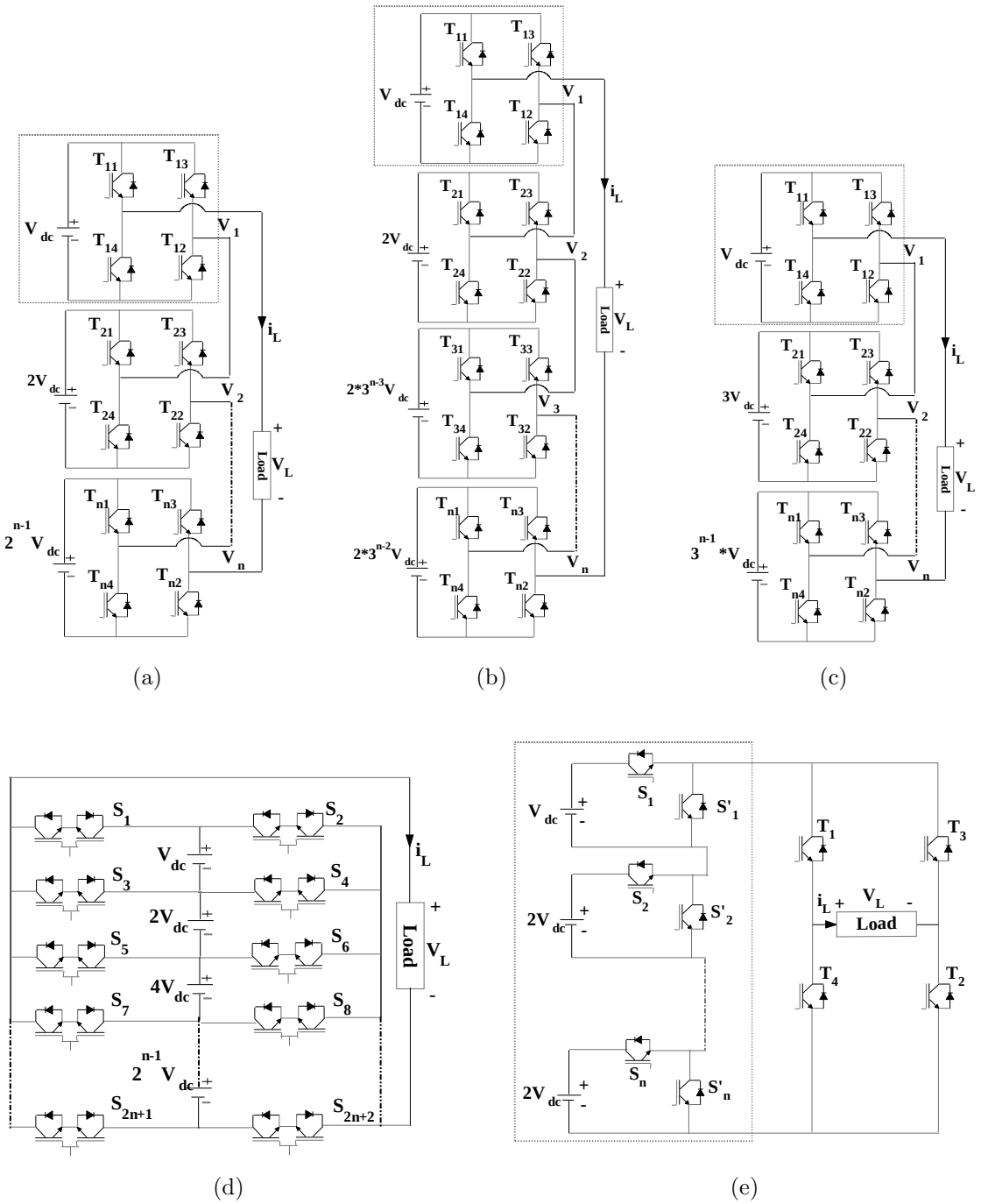
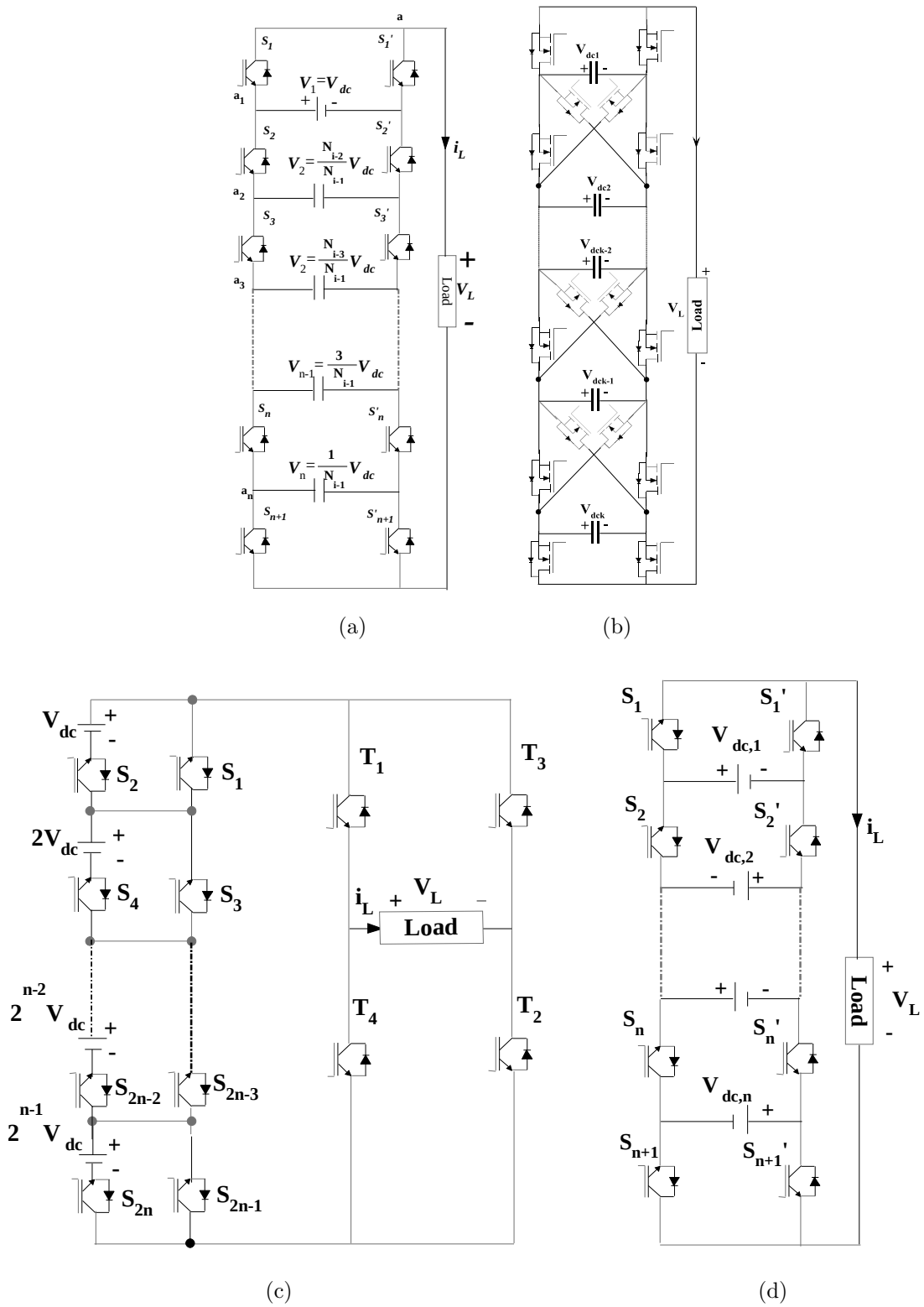


Figure 1.11: (a) Binary asymmetrical MLI, (b) Quasi linear MLI, (c) Trinary asymmetrical MLI, (d) Common emitter bidirectional switch based asymmetrical MLI, (e) Unidirectional switch based asymmetrical MLI in binary fashion.



(a) (b)

(c) (d)

Figure 1.12: (a) Cross switched asymmetrical MLI, (b) Cross connected structure asymmetrical MLI, (c) Binary novel asymmetrical MLI, (d) A new asymmetrical CCS-MLI.

DC voltage sources and 2(n+1) bidirectional switches. In the configuration, some of the output levels were skipped across the output terminals due to lack of subtraction (For example getting of V_3 - V_1 level is not feasible by the circuit). However, only four IGBT switches will conduct for every current path at any instant of time that leads to low conduction losses. The authors could verify 147-levels with the proposed topology. Consequently, (Babaei and Hosseini, 2009) proposed another novel archetype as shown in Figure 1.11(e) consists of a series connected sub-MLI blocks associated with reduced number of IGBT switches for synthesising N_L at the phase output terminals. Furthermore, all the basic units have equal DC magnitudes except the first unit to accomplish charge balance control among the input supplies, and the standing voltage of the switches is less compared to earlier topologies. Of course (Babaei and Hosseini, 2007, Laali et al., 2010) proposed some of the charge balancing techniques for cascaded H-bridge asymmetrical topologies, and in the presented topology, polarity generator (H-bridge) modulated at a low switching frequency to get rid of switching losses (Du et al., 2006).

Later on, MLI research families had given much interest to design the least device count MLIs by the proper selection of input DC values. Authors (Ounejjar et al., 2011) also proposed an asymmetrical flying capacitor (packed U cell) MLI as shown in Figure 1.12(a). They have reported an unusual method to ascertain the values of voltages across the capacitors as specified in Table 1.2. In this configuration, V_1 is the principal DC-bus, produced from AC supply and suitable control techniques regulate the remaining DC voltage levels across the capacitors V_2, V_3... V_n. Thus accessories of the input DC components like an excessive number of transformers and diode bridge rectifiers not required which consequently depreciate the production cost. However, the circuit undergoes from a common drawback manifested at low modulation indices, where the input capacitors not adequately charged due to lack of connection between the main DC bus and the capacitors.

Then after, (Gupta and Jain, 2012a) proposed a novel MLI topology which can be synthesised additive combinations of the input DC levels with fewer power devices shown in Figure 1.12(b) similar to (Mueller and Gran, 1998)'s configuration. In addition to that, all possible subtractive combinations also achieved with an appropriate modulation scheme. This topology was ascertained as an alternative for the CHB-MLI applications (Zeng et al., 2010, Tolbert and Peng, 2000, Sirisukprasert et al., 2003, Liu and Luo, 2005, Cheng et al., 2006, Rodriguez-Bernet, 2007). The

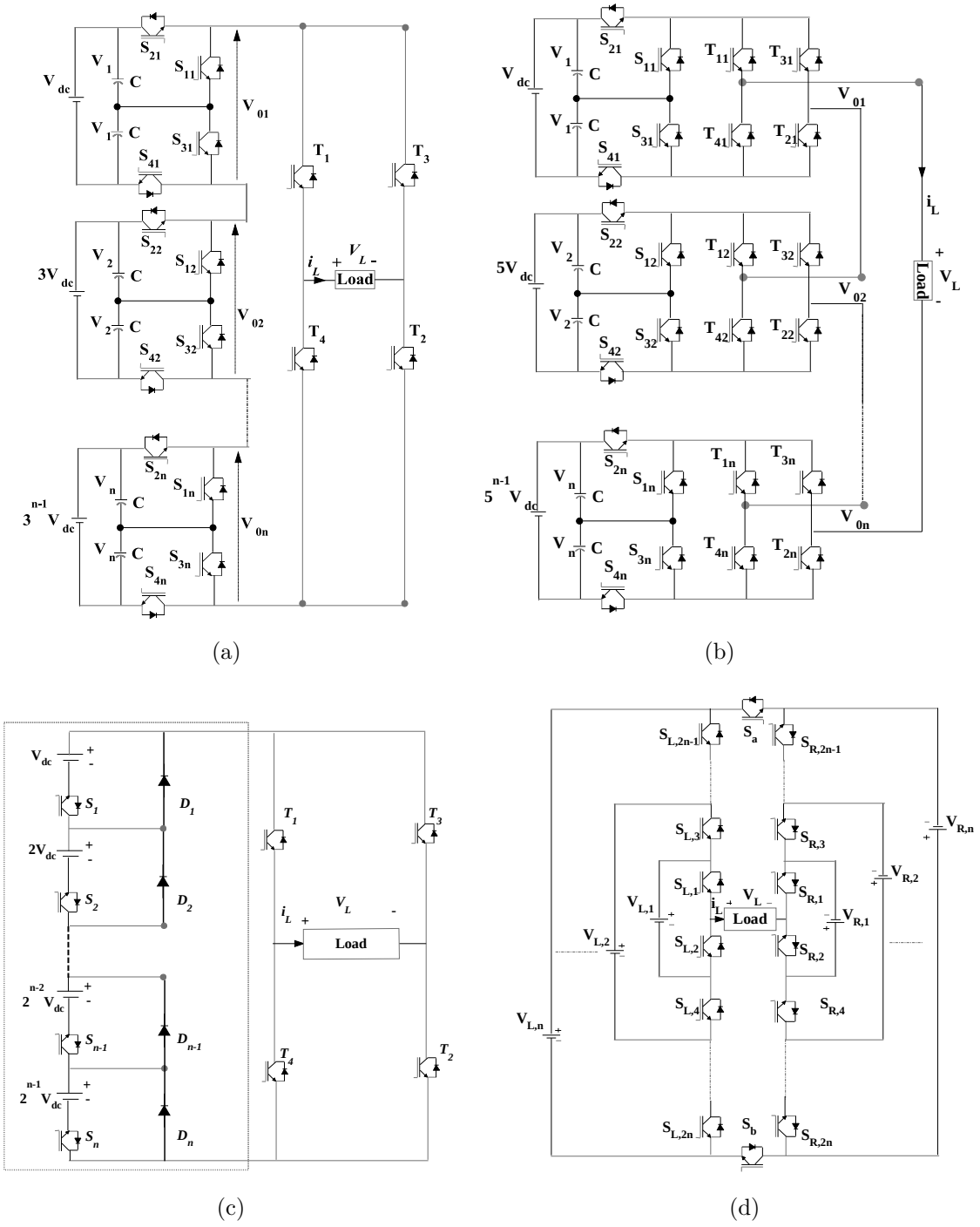


Figure 1.13: (a) Trinary asymmetrical MLI for high power applications, (b) Penta asymmetrical MLI, (c) Asymmetrical MLI with least number of switching devices, (d) Advanced H-bridge asymmetrical inverter.

circuit produces $2^{2n}-4n+1$ redundant states which drive an active voltage balancing. However, all possible voltage levels did not have redundant states.

The Figure 1.12(c) is an another novel asymmetrical MLI presented by (Babaei et al., 2012). This configuration constituted of two parts; level creates unit and H-bridge unit. Herein, the number of devices in the current path is considerably lower than that of the other conventional topologies which lead to diminishing voltage drop across the semiconductor devices. But, it requires DC voltage sources with different values which to be a challenging issue. The asymmetrical topology must be able to bypass or conduct the DC voltage sources separately for creating all the desired voltage levels. They have reported a 15-level asymmetrical inverter whose output voltage THD is 4.63%.

After that, (Gupta and Jain, 2014) did investigations for employing commonly used asymmetric selections (binary, trinary) for CCS-MLI as shown in Figure 1.12(d). But the structure does not synthesis all additive and subtractive combinations of the input DC magnitudes for implementing binary or trinary choices of the individual DC supplies. Therefore the authors kept a great effort to develop a new algorithm for selecting the proper individual supplies which can synthesise a multilevel waveform with a maximum number of levels and equal step size. The primary development of this topology is that the number of power devices is lesser than conventional circuit. The algorithm is followed by equations 1.1 & 1.2 for 'n'number of input DC sources. For even number of sources:

$$V_{dc,j} = \begin{cases} (2j-1) * V_{dc} & ; \quad 1 \leq \quad j \quad \leq \quad n/2 \\ 2 * (n+1-j) * V_{dc} & ; \quad (n+2)/2 \quad \leq \quad j \quad \leq \quad n \end{cases} \tag{1.1}$$

For odd number of sources:

$$V_{dc,j} = \begin{cases} (2j-1) * V_{dc} & ; \quad 1 \leq \quad j \quad \leq \quad (n+1)/2 \\ 2 * (n+1-j) * V_{dc} & ; \quad (n+3)/2 \quad \leq \quad j \quad \leq \quad n \end{cases} \tag{1.2}$$

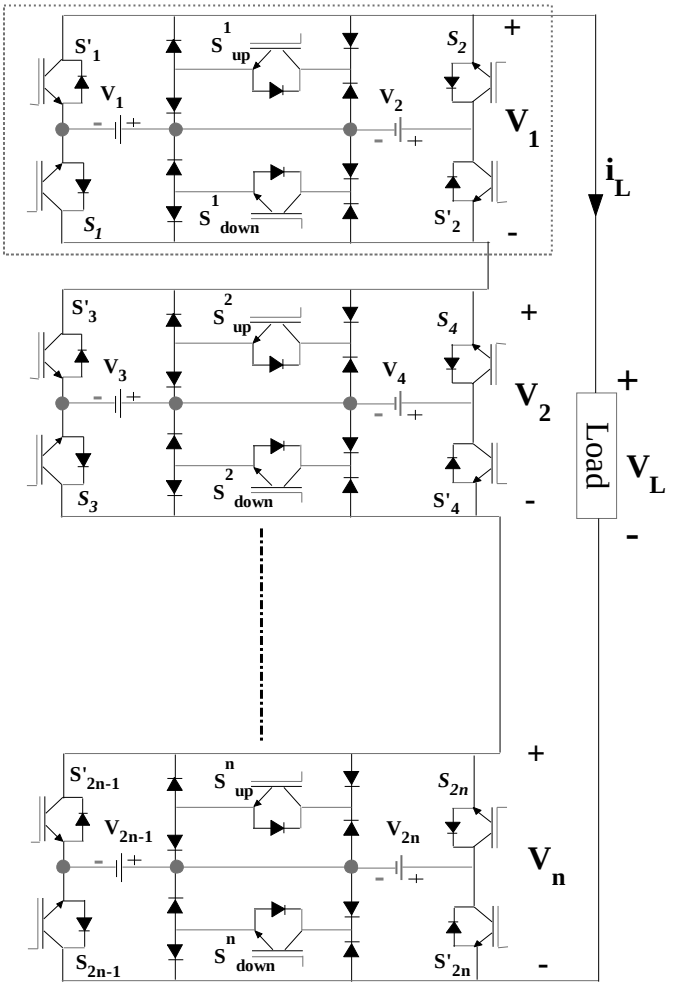
To the same asymmetrical family, (Babaei et al., 2014b) introduced two new cir-

cuits with a reduced number of independent voltage sources as shown in the Figure 1.13 (a) and (b). Herein, the required number of DC sources are lesser than conventional topologies which can observe from the Table 1.3, particularly at high voltage levels. However cascaded cells are not the same which leads to the loss of modularity. Moreover, the conduction losses are higher in the Figure 1.13 (b) than (a).

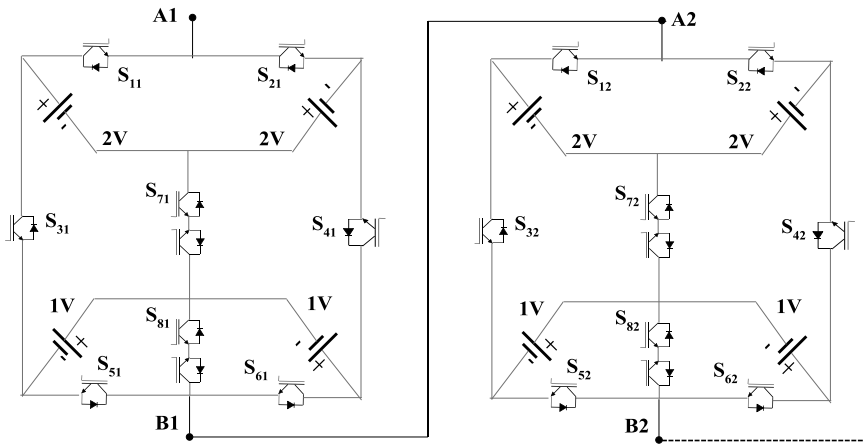
Later, (Alishah et al., 2014) proposed an MLI which produce the highest number of levels with the smallest count of IGBTs and gate drive circuits as shown in Figure 1.13 (c). Therefore, this topology overcomes the cost and control complexity issues and improves the overall reliability and efficiency. For this asymmetric structure, the DC source values are considered according to the algorithm mentioned in Table 1.3. After that, (Alilu et al., 2013) suggested an advanced H-bridge inverter with single DC source and two unidirectional switches per each H-bridge module. On observing, if the magnitudes of DC sources are equal then output voltage levels are reduced to three, or else the values of DC voltage sources different to get extra voltage levels without increasing switches. This design is further extended by (Babaei et al., 2014a) as depicted in Figure 1.13 (d), with a new algorithm for assigning input DC voltage values. One of the critical defects of this topology is that the wide variety of magnitudes of the DC voltage sources.

Authors (Mokhberdoran and Ajami, 2014a) presents a generalised asymmetrical topology using basic blocks as depicted in Figure 1.14 (a). The fundamental block consists of six semiconductor switches, eight independent diodes and two DC links whose magnitudes are unequal. Herein, anti-parallel diodes and independent diodes are responsible for conducting a backward current caused by the inductive load. The presented archetype is verified with three distinct algorithms as displayed in Table 1.3. The normalised peak inverse voltage of proposed topology has higher than CHB topology, and the circuit delivers an incredible power loss.

Next fascinating configuration is introduced by (Samadaei et al., 2016), which is known as Envelope Type (E-Type) module is shown in Figure 1.14 (b). It can generate both positive and negative levels without using any H-bridge circuit at its output terminals. Moreover, it can be easily modularized, and each unit can deliver 13-levels with just 10-IGBT switches. Efficiency and THDv% of the proposed circuit is reported as 96.56% and 3.46% sequentially.



(a)



(b)

Figure 1.14: (a) New cascaded asymmetrical MLI, (b) Envelop type asymmetrical MLI.

1.4.2.1 Summary of asymmetrical MLIs

The most referred asymmetrical MLIs are discussed in this subsection. The choice of input DC values of the listed topologies is given in Table 1.2 and 1.3. The Figure 1.15 exposes the lowest switch count configuration (Babaei et al., 2014a) for a given number of levels, the least IGBT count MLI circuit for a given N_{DC} (Alishah et al., 2014), and the highest output level configuration with the minimum input DC sources (Babaei et al., 2014b).

1.4.3 Hybrid MLIs

The pursuit of a synergistic approach which combines the distinct semiconductor switches, topologies and modulation strategies to optimise the power processing of the overall system of the converter. This type of converters is very popular with the name of Hybrid Multilevel Inverter [HMLI]. In the literature, an enormous HMLIs have been presented for two decades. Firstly, (Jinghua and Zhengxi, 2008) were attempted merely on hybrid modulation strategies for standard HMLI topologies. But the author did not describe the novel hybrid configurations concerning semiconductor switches and structural behaviour. Therefore the current section is entirely dedicated to analysing the recent HMLIs and Hybrid modulation strategies.

Authors (Manjrekar et al., 1998, 2000) proposed a novel hybrid seven-level converter using two distinct H-bridges connected in cascade fashion as shown in Figure 1.16 (a). Herein one H-bridge is developed by GTO/IGCT (large blocking voltage switch), and another H-bridge is built with IGBT (high switching frequency switch) (BinWu, 2006). Thereby it can achieve proper harmonic profile of an output waveform for high voltage applications. However, each bridge has an isolated DC-source along with unusual switching frequency leads to loss of modularity and increase the manufacturing cost, and also the circulating current passes within the bridges during the modulation depth region around 37% to 78% (Lund et al., 1999). Thus it had limited commercial applications (Abu-Rub et al., 2010). Nevertheless, (Rech and Pinheiro, 2007) were kept their effort to overcome those difficulties with their novel topology which is depicted in Figure 1.16 (b). In structure point of view, each cell had distinct topologies (like a two-, three- and five-level blocks) connected in series and operated with generalised modulation strategy (Lund et al., 1999, Wang et al., 2004, Lipo and Manjrekar, 1999). Here, the circulating energy among the cells has reduced

Table 1.2: Component details of asymmetrical multilevel Inverters

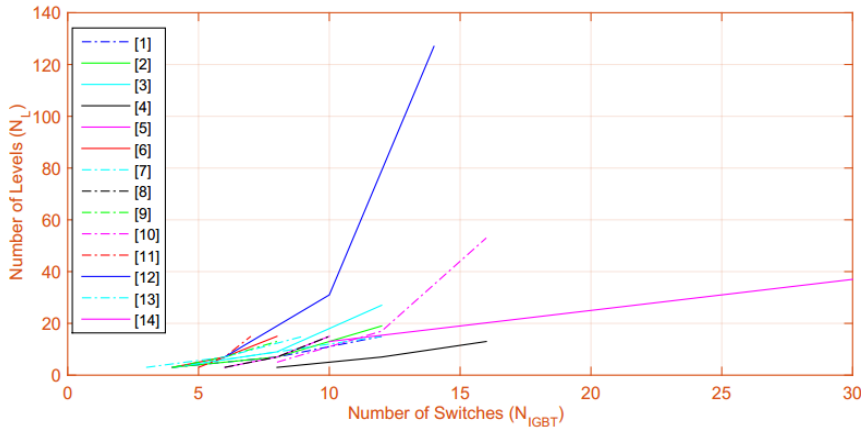
Type of MLI	$\mathbf{N}_{DC}$	$\mathbf{N}_{L}$	$\mathbf{N}_{IGBT}$	$\mathbf{N}_{G}$	$\mathbf{N}_{mcps}$	$\mathbf{V}_{O,max}$	$\mathbf{V}_{dc,(j)}(j = 1, 2, ...n)$
1	n	$2^{(n+1)}$-1	4n	4n	2n	$(2^n$-1)* V_{dc}	$2^{j-1} * V_{dc}$
2	n	$2*3^{(n-1)}$+1	4n	4n	2n	$3^{(n-1)}$* V_{dc}	$V_1 = V_{dc}$ $V_j = (2 * 3^{j-2}) * V_{dc}$ $(j = 2, 3, ...n)$
3	n	3^n	4n	4n	2n	$(3^n$-1)* $V_{dc}/2$	$3^{j-1} * V_{dc}$
4	n	n^2+n+1	4(n+1)	2(n+1)	4	$(2^n$-1)* V_{dc}	$2^{j-1} * V_{dc}$
5	n	4n-1	2n+4	2n+4	n	(2n-1)* V_{dc}	$V_1 = V_{dc}; V_j = 2 * V_{dc}$ $(j = 2, 3, ...n)$
6	n	$2^{(n+1)}$-1	2(n+1)	2*(n+1)	n+1	$\sum_{j=1}^{n} V_j$	$V_1 = V_{dc}$ $V_j = \frac{N_L^{n-j}}{N_L^{n-1}} * V_{dc}$ $(j = 2, 3, ...n)$
7	n	6n-3	4n	4n	n+1	$\sum_{j=1}^{n} V_j$	$V_j = 3 * V_{dc}; V_n = V_{dc}$ $(j = 1, 2, ...(n-1))$
8	n	$2^{(n+1)}$-1	2n+4	2n+4	n+2	(2^{n-1})*V_{dc}	$2^{j-1} * V_{dc}$
9	n	n^2+n+1	2(n+1)	2(n+1)	n+1	n(n+1)*$V_{dc}/2$	-

1. Manjrekar et al. (2000)
2. Mueller and Gran (1998)
3. Lai and Shyu (2002)
4. Babaei et al. (2007)
5. Du et al. (2006)
6. Ounejjar et al. (2011)
7. Gupta and Jain (2012a)
8. Babaei et al. (2012)
9. Gupta and Jain (2014)

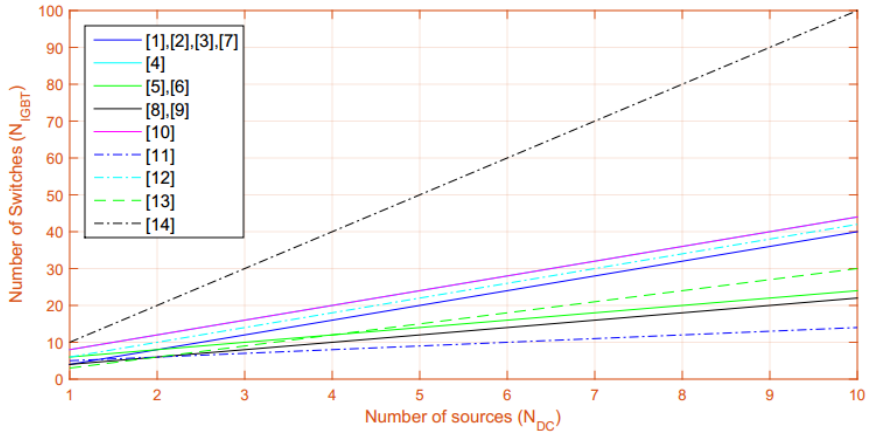
Table 1.3: Component details of subsequent asymmetrical multilevel inverters

Type of MLI	$\mathbf{N}_{DC}$	$\mathbf{N}_{L}$	$\mathbf{N}_{IGBT}$	$\mathbf{N}_{G}$	$\mathbf{N}_{mcps}$	$\mathbf{V}_{O,max}$	$\mathbf{V}_{dc,(j)}(j = 1, 2, ...n)$
10	n	2*$3^{(n)}$-1	4(n+1)	4(n+1)	2n+2	(3^{n-1})*V_{dc}	$3^{j-1} * V_{dc}$
11	n	$2^{(n+1)}$-1	n+4	n+4	n+2	(2^{n-1})*V_{dc}	$2^{j-1} * V_{dc}$
12	2p	$2^{(n+1)}$-1	2n+2	2n+2	2p+1	$3 * 5^{p-1} * V_{dc}$	$V_{L,j} = 5^{j-1} * V_{dc}$ $V_{R,j} = 2 * 5^{j-1} * V_{dc}$ $(j = 1, 2, ...p)$
13	2p	$5^{n/2}$	3n	3n	2p	$\frac{5^{p}-1}{2} * V_{dc}$	$5^{j-1} * V_{dc}$ $(j = 1, 2, ...p)$
	2p	$2^{(n+1)}$-1	3n	3n	2p	$(4^{p}$-1)*V_{dc}	$2^{j-1} * V_{dc}$ $(j = 1, 2, ...2p)$
	2p	$7^{n/2}$	3n	3n	2p	$\frac{7^{p}-1}{2} * V_{dc}$	$7^{(j-1)/2} * V_{dc}$; j = odd $2 * 7^{(j-1)/2} * V_{dc}$;j = even
14	4p	3n+1	2.5n	2n	5p	20p	$V_1 = V_2 = 2 * V_{dc}$ $V_3 = V_4 = V_{dc}$

10. Babaei et al. (2014b)
11. Alishah et al. (2014)
12. Babaei et al. (2014a)
13. Mokhberdoran and Ajami (2014a)
14. Samadaei et al. (2016)



(a)



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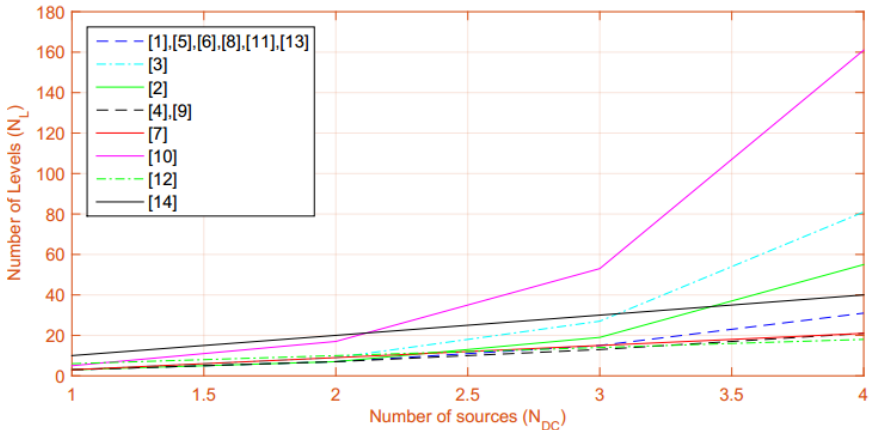
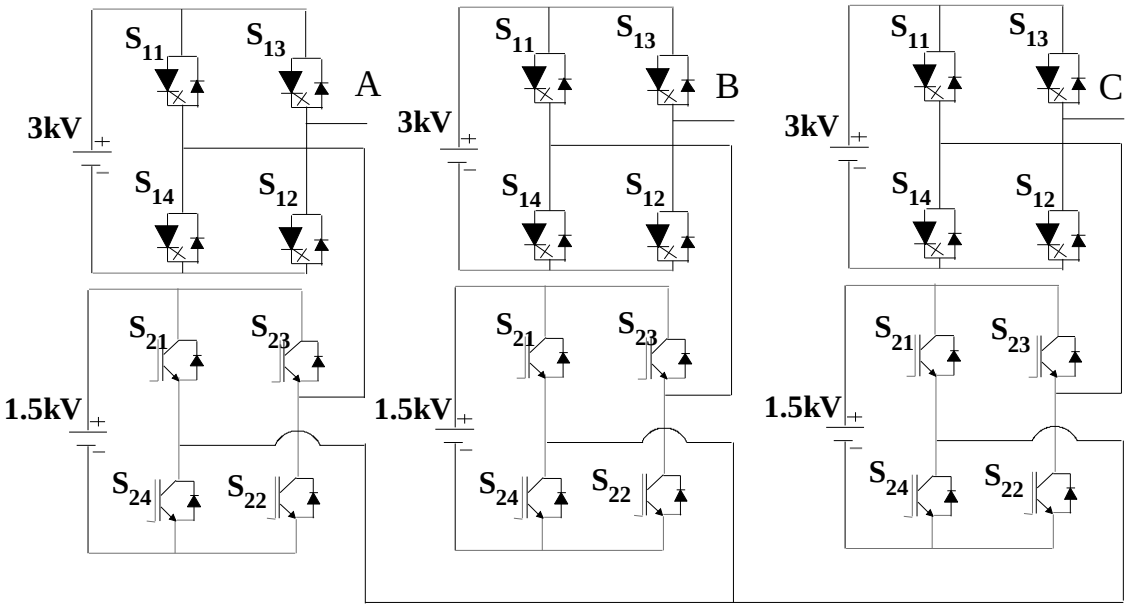
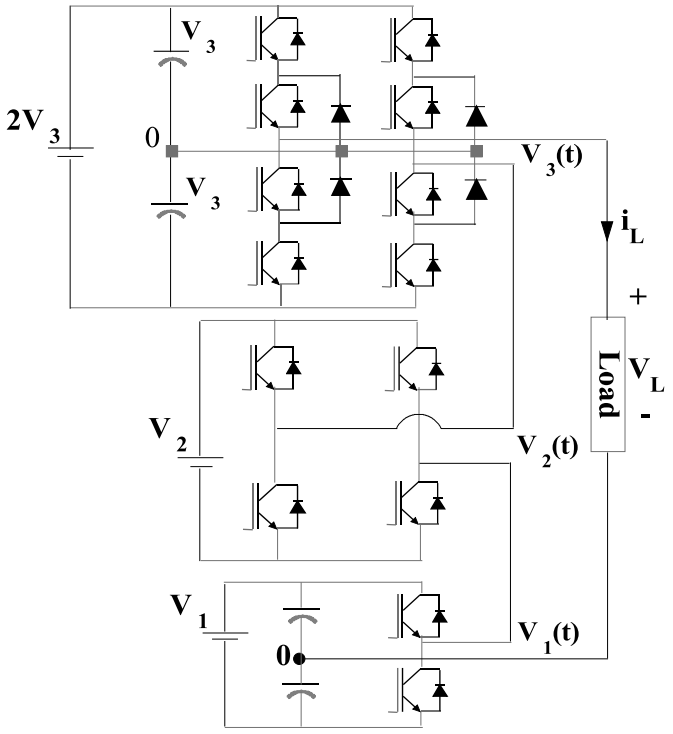


(c)

Figure 1.15: (a) The total number of switching components (N_{IGBT}) versus the total number of steps (N_L), (b) The total number of input DC supplies (N_{DC}) versus the total number of switching components (N_{IGBT}), (c) The total number of input DC supplies (N_{DC}) versus the total number of steps (N_L).

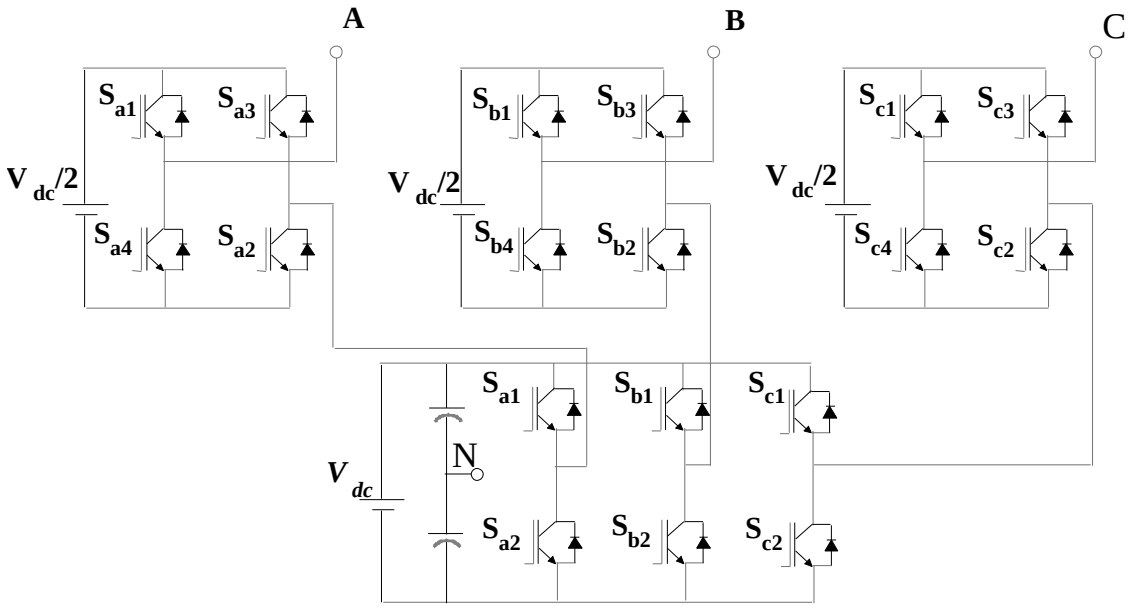


(a)

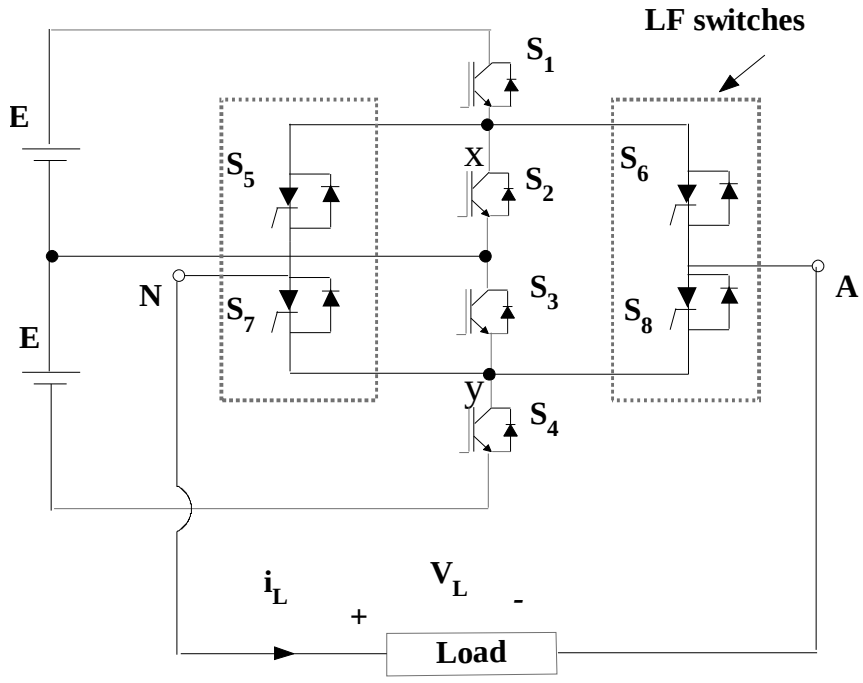


(b)

Figure 1.16: (a) Seven level hybrid inverter with distinct switching devices (b) Distinct structure based HMLI



(a)

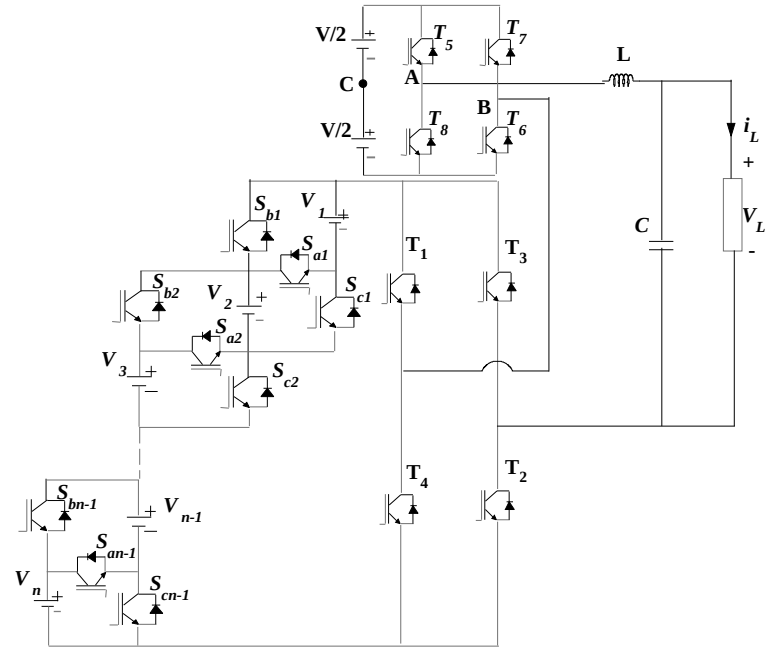


(b)

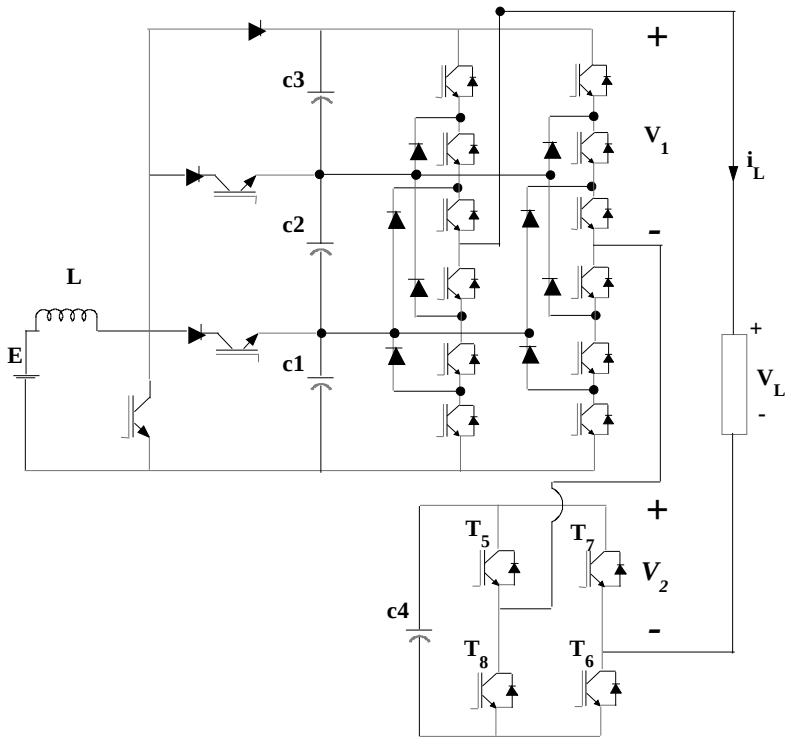
Figure 1.17: (a) Three phase five level cascaded HMLI, (b) Novel symmetrical HMLI.

without affecting the number of levels of the output waveform since third cell (highest power cell) was functioning at lesser than the load voltage. However, few significant parameters such as efficiency, weight/ volume, harmonic distortion factor and circuit three-phase extendability were not addressed. Later on, (Khomfoi and Aimsaard, 2009) were proposed a 5-level three-phase configuration as shown in Figure 1.17 (a). It consists of two types of inverters to optimise the output voltage waveform. One is standard three-phase inverter generates a square waveform, and another inverter is a normal H-bridge which gives a three-level PWM voltage waveform. In fact, the topology was investigated at different modulation indices. Therefore it is much suitable for a broad range of voltage control applications like a traction drives. Comparatively, it has a reduced number of power switches to perform the same function than the Figure 1.16 (a) circuit. Thus, it is an alternative to the topology presented by (Manjrekar et al., 1998). However, it was facing the circulating energy issues between the two parts.

After that (Ruiz-Caballero et al., 2010) introduced a novel symmetrical HMLI (insulated DC supplies of equal value) for both, single and three-phase systems. A single-phase version is depicted in Figure 1.17 (b). If it extended to the three-phase system, then 15-levels and 9-levels are attained at the phase and load voltage waveforms consequently. Herein the switches S_5 to S_8 are connected in an H-bridge fashion which is responsible for generating positive and negative voltages, and then switches S_1 to S_4 are switched at proper modulation pattern to produce the desired load voltage waveform. It has similar potential to generate $2N_{dc} + 1$ levels across the load terminals as stated in (Peng, 2000). In fact, this class of converters is very much appropriate for MV networks. The extraordinary merit of this architecture is a less number of input sources. Nevertheless, it has not been discussed the existence of an asymmetrical HMLI structure. Later (Hinago and Koizumi, 2010) were offered a HMLI is shown in Figure 1.18 (a). Here two distinctive topologies were joined in series and driven by a hybrid switching techniques (Liu et al., 2008, Zhang et al., 2001). These unusual topologies are studied individually in earlier subsections. Compare to symmetrical CHB inverter, the series-parallel conversion inverter has lesser number of switching devices which modulated at a fundamental frequency, but H-bridge cell is operating at high frequency. In fact, it is extendable to higher levels with fewer devices. Then the same kind of approach was continuing with two different conventional MLI configurations (diode clamped MLI and cascaded H-bridge MLI) by

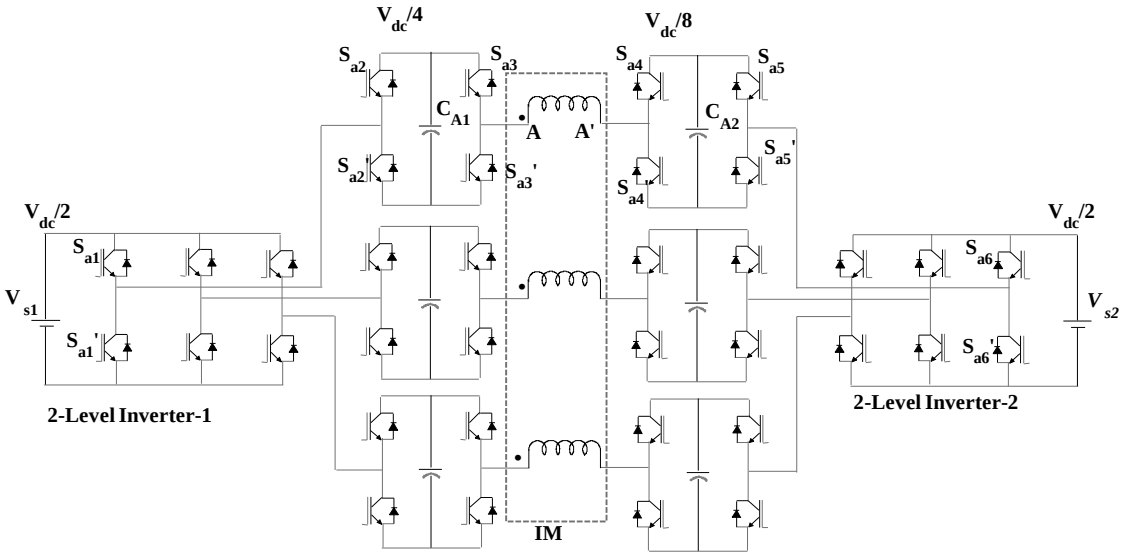


(a)



(b)

Figure 1.18: (a) A single-phase HMLI using switched series/parallel DC voltage sources, (b) HMLI with series connection of DC-MLI and CHB-MLI.



(a)

Figure 1.19: Double side CHB inverter connected hybrid nine level inverter

(Nami et al., 2011) and see in Figure 1.18 (b). Herein an input of DC-MLI is supplied by multi-output boost (MOB) converter. This arrangement determined asymmetrically instead of symmetrical fashion to get more output voltage levels which result in better THD and smaller filter size with the same number of switching components. However, these circuits have to concentrate to overcome the limitations such as loss of modularity, control complexity, and increased manufacture cost for higher levels.

A fascinating HMLI topology for industrial drive applications is presented by (Rajeevan et al., 2011). This circuit consists of two three-phase traditional inverters (two-level) supplied by isolating input DC-sources and six H-bridge inverters as shown in Figure 1.19. It has few exciting features such as the elimination of triplen harmonics in the winding currents, and reduction in switching losses since high voltage inverter (three-phase two-level inverter) operates at the minimum switching frequency. It also has potential to work in a three-level mode in case of any switch failure in H-bridges. However, the topology needs a highly complicated control strategy to balance the capacitor voltages of an each H-bridge when the levels are moving high.

In fact, (Babaei et al., 2012) presented two novel MLI topologies which are realised by symmetric and asymmetric input DC-sources, shown in Figure 1.7 (c) and 1.13 (b) sequentially. In these arrangements, H-bridge switches T_1 - T_4 have to tolerate

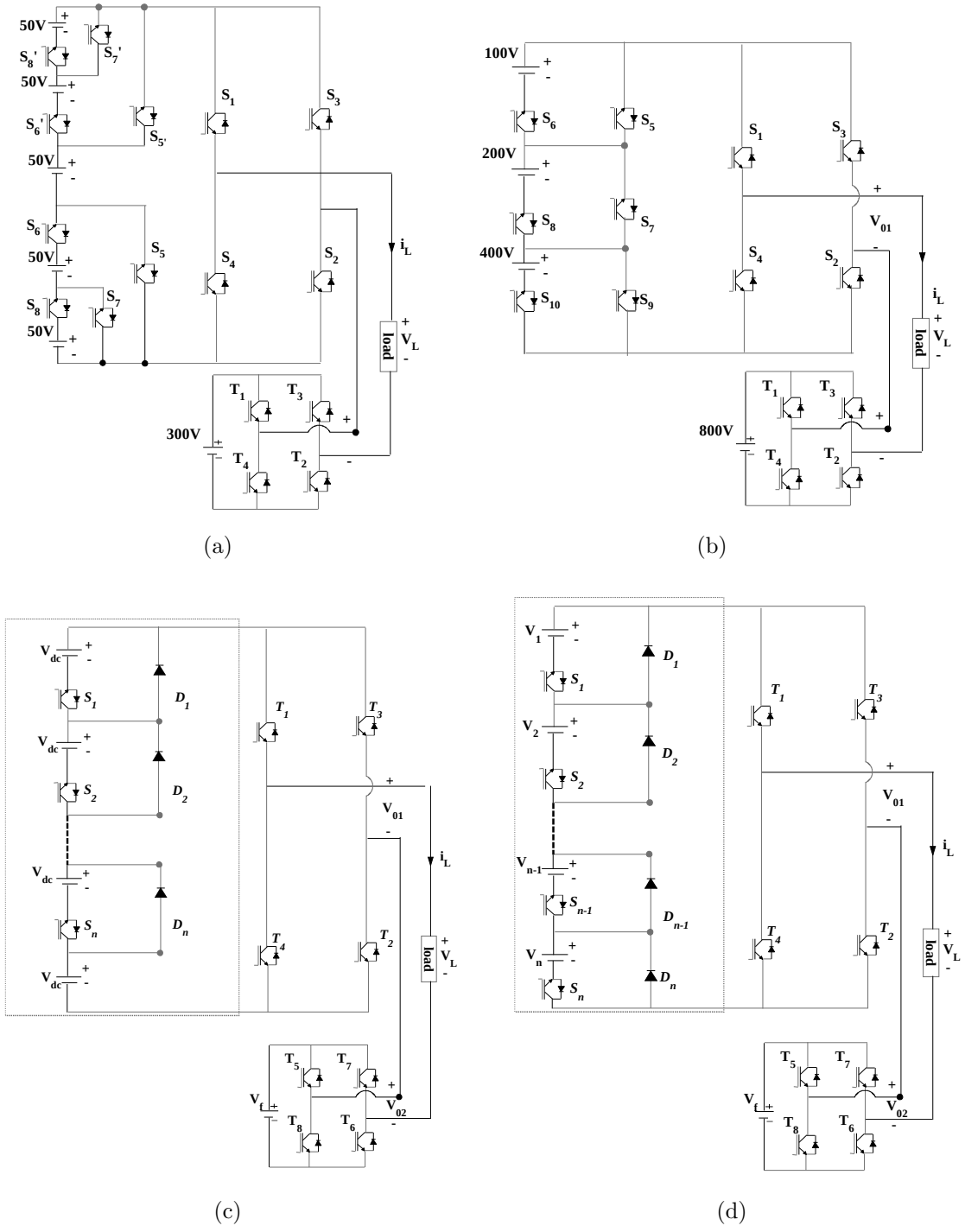


Figure 1.20: (a) Series connection of symmetric and H-bridge based HMLI, (b) Series connection of asymmetric and H-bridge based HMLI, (c) A novel HMLI with symmetric structure (d) A novel HMLI with asymmetric structure.

a voltage equal to the sum of all the input DC sources thereby the topologies are restricting for higher voltage levels. To mitigate this issue, the same authors were suggested new HMLIs by minor correction as shown in Figures 1.20 (a) and 1.20 (b). It is worth noting that the presented two HMLIs can run at all switching techniques. Moreover, the H-bridge switches are working at diminished voltage ratings. Therefore, the hybrid topologies are suitable for high voltage networks. Despite, this configuration demands a large number of input transformers and rectifier circuits for three-phase and high-level systems. After that (Alishah et al., 2014) also suggested the modified circuits as similar as (Babaei et al., 2012) suggestions which are depicted in Figure 1.20 (c) and 1.20 (d). These HMLIs can generate the highest number of output voltage levels with the least device counts than all other the disputed HMLIs.

1.4.3.1 Summary of Hybrid MLIs

All the listed HMLI topologies are analysed individually and comparatively. Each HMLI circuit addresses a specific problem such as device count, switching losses, and applications,...etc. The benefits and limitations of every HMLI are presented in Table 1.4 and 1.5. Herein, the component comparison among all HMLIs is not feasible since the configurations are unevenly designed.

1.4.4 Single DC-source MLIs

In fact, most of the MLIs demand more input DC-sources, that means a large number of input transformers and rectifier circuits have to be built to provide the separate DC-sources. Thus, an installation area, overall cost, and efficiency of the MLI are harshly affected. Therefore, the researchers have been focused on minimising the input setup by using only one DC-source. The subsection gives a deep insight of the all single DC-based MLIs.

Authors (Soto et al., 2003) were introduced a single DC-based five-level configuration consisting of two H-bridge cells and two interface inductors. Here, the inductors are connected between the positive rails of the two H-bridges and negative rails of two H-bridge separately as shown in Figure 1.21 (a). Moreover, it can be extended to higher levels by adding extra H-bridge cells along with interfacing inductors. The significant feature of this circuit is the back to back energy transformation. But the switches have to withstand for high currents. Next, a converter has employed

Table 1.4: Features of the HMLIs

Ref	Benefits	Limits
[1]	• It improves the power quality by generating a higher number of steps with given H-bridge modules. • It can run at higher VA rating with the minimum switching losses than conventional cascaded MLI.	• Higher switching stresses. • Isolated asymmetrical DC-sources are needed.
[2]	• It is a generalised HMLI circuit. • It can minimise the circulating energy among the series-connected cells.	• It is an intricate circuit design when the topology forced to a higher level.
[3]	• It has lesser switching devices than standard cascaded MLI to get optimised voltage levels. • It is fit for renewable applications.	• Charge balance and circulating energy issues are profoundly affecting the entire system if any malfunction happens in DC source selection.
[4]	• It can improve an output voltage waveform with low harmonic distortion and smaller filter size. • It needs lessened insulated DC-sources.	• The requirement of semiconductor devices is more as like CHB-MLI.

1. Manjrekar et al. (2000)
2. Rech and Pinheiro (2007)
3. Khomfoi and Aimsaard (2009)
4. Ruiz-Caballero et al. (2010)

Table 1.5: Features of remained HMLIs

Ref	Benefits	Limits
[5]	• The switching device count is comparatively lower than symmetrical CHB-MLI. • Compact in size and quickly extended to a higher level.	• Loss of modularity. • It needs a large number of separate DC-supplies.
[6]	• It can achieve higher output voltage resolution and lesser control complexity.	• The cost of the entire circuit is more since the high utilisation of clamping diodes and rectifiers.
[7]	• It has lower switching losses.	• It has complicated charge balancing problem when the output levels are moving high.
[8]	• It is more suitable for higher voltage networks.	• It is not promising to apply the voltage balance control techniques. • Few switches shouldn't be able to withstand the rated output voltage which leads to restricting the high voltage applications.
[9]	• It can possess the highest output levels with the least number of switching devices.	• It is used in only unidirectional power flow applications.

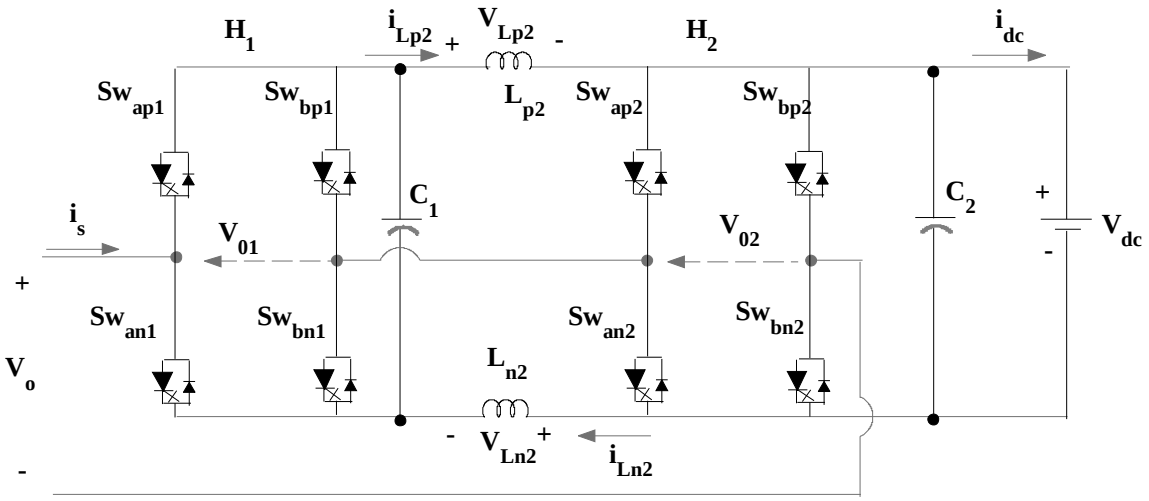
5. Hinago and Koizumi (2010)

6. Nami et al. (2011)

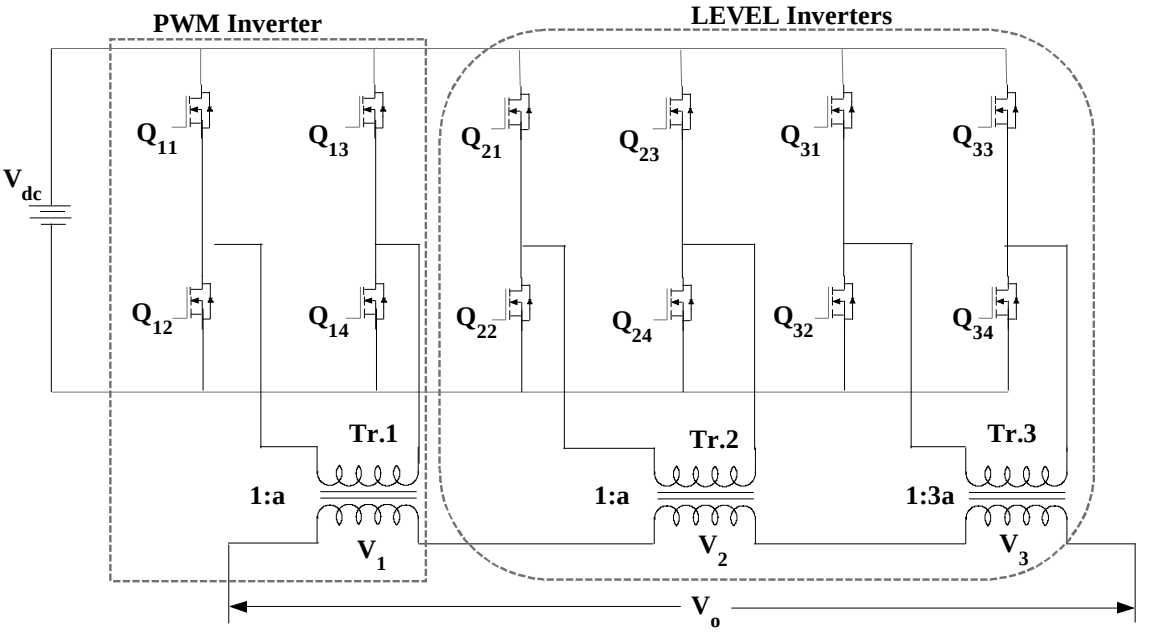
7. Rajeevan et al. (2011)

8. Babaei et al. (2012)

9. Alishah et al. (2014)



(a)



(b)

Figure 1.21: (a) A new cascaded MLI with single non-isolated DC link, (b) Cascaded single-phase transformer MLI configuration.

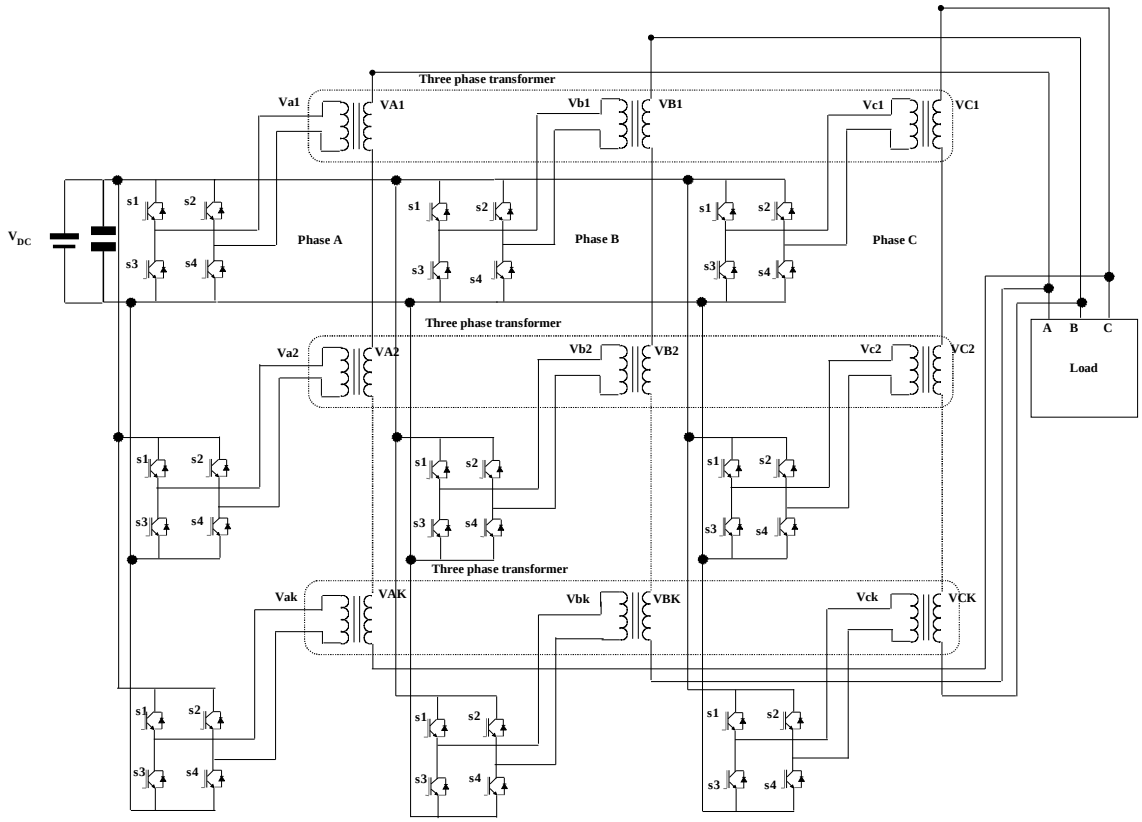


Figure 1.22: Single DC-source CHB-MLI by employing low-frequency three-phase transformer.

cascaded transformers to design a single DC circuits (Kang et al., 2005). The main modification compared with the standard multilevel arrangements is that the configuration is functioned with only one DC source, and two distinct parts of the converter as depicted in Figure 1.21 (b) based the operating frequency of the individuals. The first part is accomplished with PWM switching strategy and rest of the part is functioned at the fundamental frequency. Moreover, each H-bridge output is connected to the primary windings of linear transformers. Thereby the galvanic isolation between input DC source and the load is provided which makes the converter to surrender to the photo-voltaic applications. However, using bulky transformers poorly results in size and efficiency of the inverter. Later, (Suresh and Panda, 2010) kept their excellent effort in designing three-phase MLIs by using three-phase transformers as shown in Figure 1.22. The proposed CHB system with three-phase transformers has low complexity regarding additional components for high-quality output waveforms than previous transformer based archetypes. Besides, the efficient cost function quan-

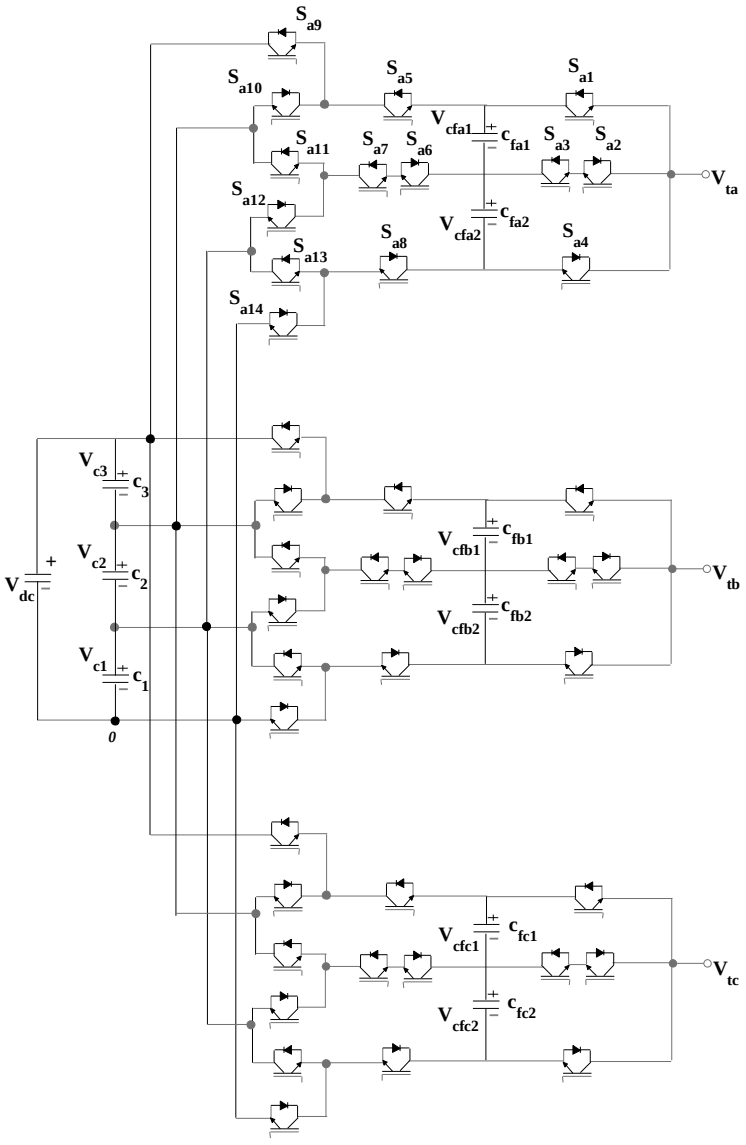
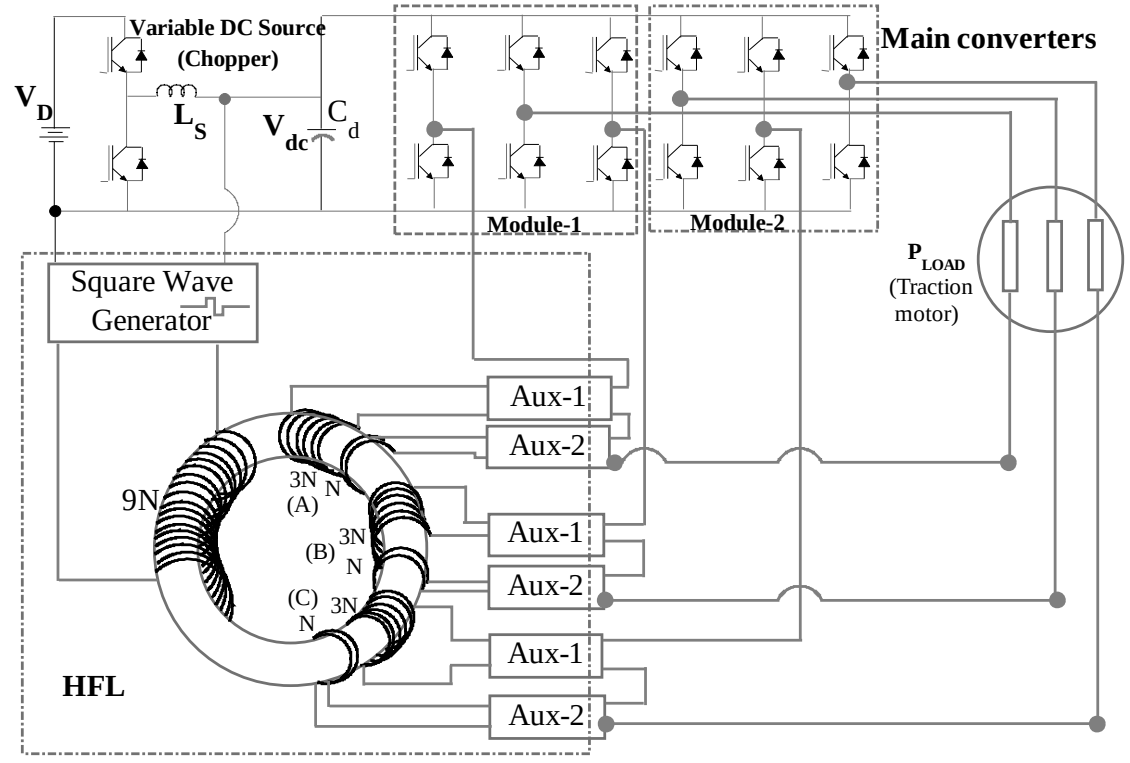


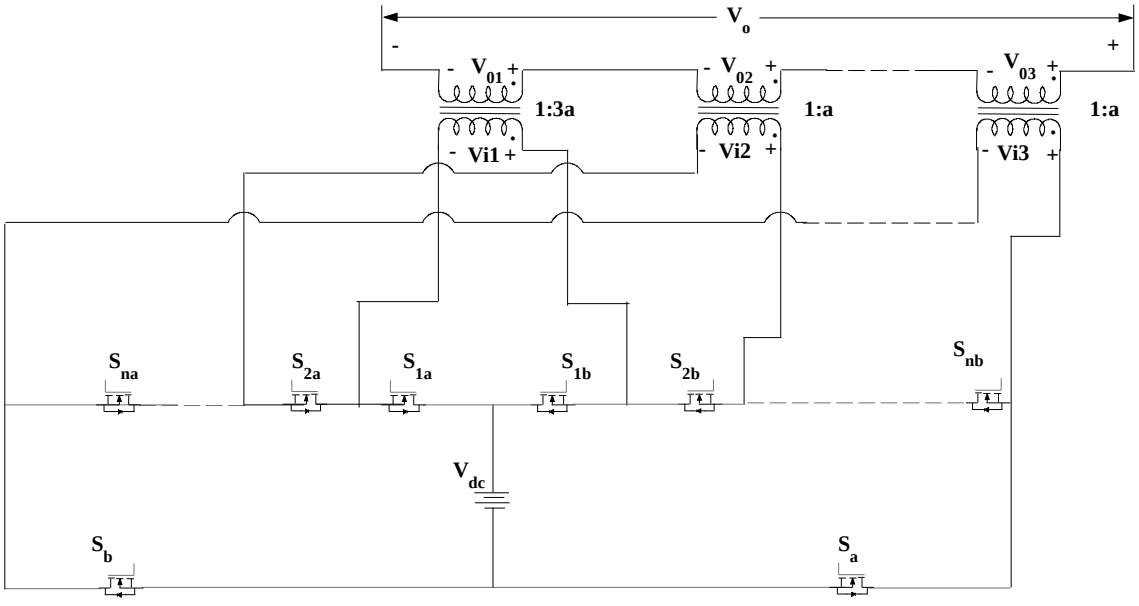
Figure 1.23: Active neutral point clamped MLI using single DC supply.

tified by concerning filter-size and total harmonic distortion. Further, three primary control methods for the CHB topology, namely (i) fundamental switching technique, (ii) selective harmonic elimination PWM (SHEPWM) and (iii) SPWM methods were implemented to this new circuit. In fact, handling the heavy elements (3 three-phase transformers) is a hectic job. The authors (Saeedifard et al., 2012) presented a new idea of Charge balancing capability by using an Active Neutral Point Clamped (ANPC) to higher levels. Further, a new space vector modulation (SVM)-based con-

trol approach is implemented to balance the input capacitor voltages. The proposed circuit is a seven-level converter (see Figure 1.23), and it has been evaluated for various operating conditions. Moreover, it requires a higher number of switching devices, i.e., 14 per phase and it is higher than a counterpart seven-level hybrid configuration (Manjrekar et al., 2000) which utilises only eight semiconductor devices per Phase. Next, (Pereda and Dixon, 2012, 2011) suggested a simple high-frequency link (HFL) for EV applications see in Figure 1.24(a), and this investigation has initiated to utilise toroidal transformer in MLI with appropriate modulation amendment. The recommended switching strategy decreases the size of the HFL from 20% to less than 2% of the power transferred to the machine. Even though individual H-bridges of the presented system will not transfer any power to the load, remaining inverter behave like series-active filters. Afterwards, (Banaei et al., 2012a) were come up with cascaded transformer reduced switch inverter (CTRSI) as shown in Figure 1.24(b). Herein, every transformer produces 3-levels with two semiconductor switches. The direction of the single DC source alters with the help of two switches for all the transformers. In fact, (Kang et al., 2005) were developed a circuit with H-bridges which is a union of the four switches. Thereby, the proposed inverter topology can attain a high-quality output voltage with the minimum semiconductor switches. However, it uses switches with higher current rating than the MLI illustrated in (Kang et al., 2005) and it is one of the significant defects of the circuit. Then after, (Sepahvand et al., 2013) proposed an option to substitute capacitors in places of DC sources of the H-bridge cells, and entire design has run on only one real DC source. This arrangement is shown in Figure 1.25. With this design, the cost-effective converter can be developed. But it offers severe impediment, i.e., capacitor voltage balancing. A new algorithm has proposed with the phase-shift modulation PWM method to overcome the voltage balancing issue. The proposed control technique has very flexible regulation when an inverter is supplying a contaminated load (highly inductive load). Later on, (Tsang and Chan, 2014) proposed a new three-phase multilevel inverter with single DC-source. The topology organises a combination of cascaded H-bridges and standard two-level inverter; this arrangement is shown in Figure 1.26(a). The proposed configuration generates a multilevel output voltage with less number of switching components. The authors verified the proposed version with a 19-level three-phase inverter. For the verification of 19-level inverter, author utilised four H-bridges and one standard three-phase inverter. Herein, the author used only one real source, and rest of them

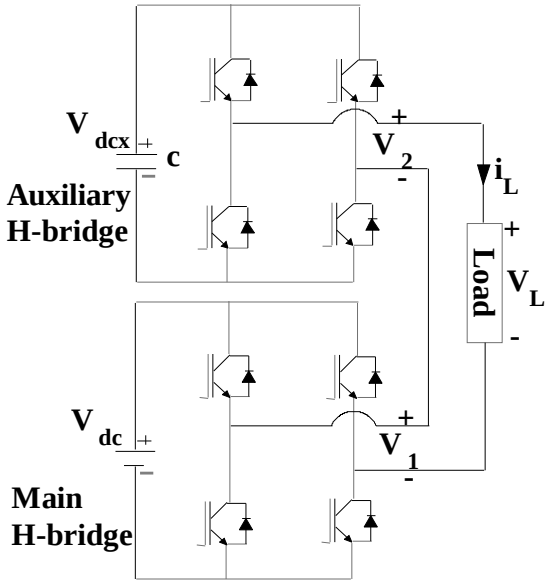


(a)



(b)

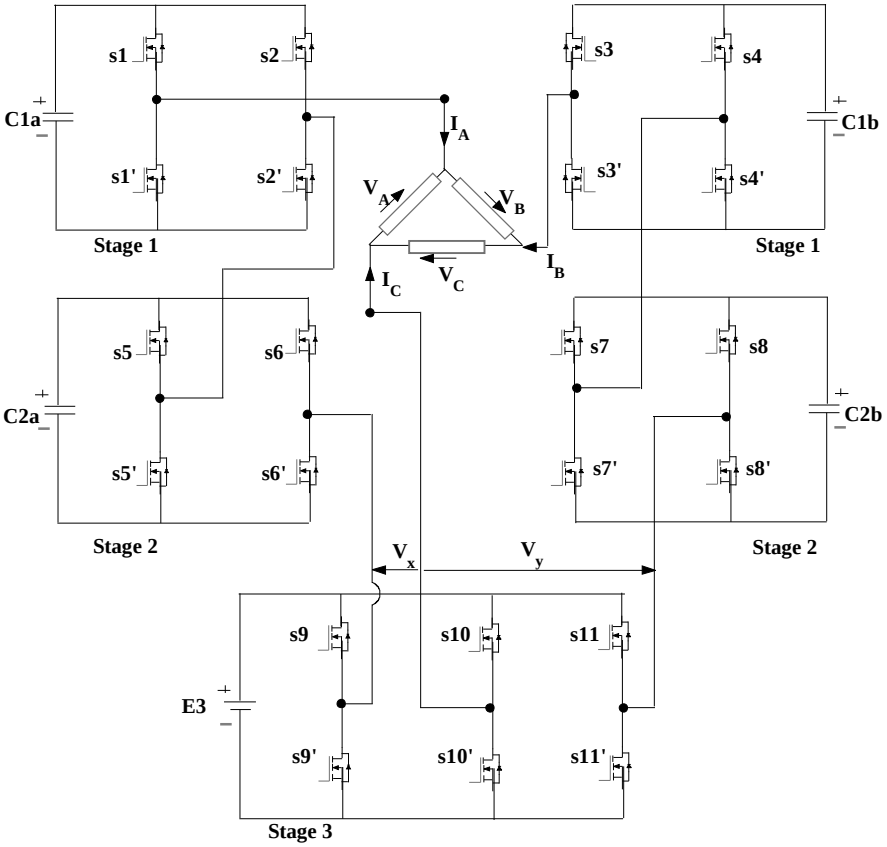
Figure 1.24: (a) A DC source asymmetric MLI with high-frequency link, (b) Cascaded transformer MLI with single input supply.



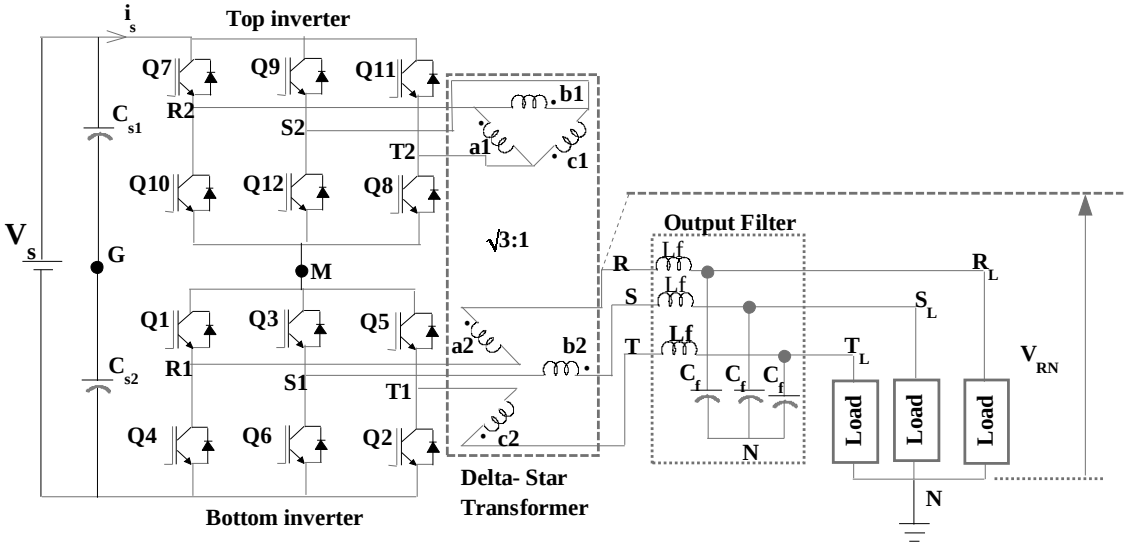
(a)

Figure 1.25: Cascaded H-bridge MLI by employing single DC and capacitors

are replaced with capacitors. This approach is similar to ref. (Sepahvand et al., 2013). However, the design is entirely different comparing with ref. (Banaei et al., 2012a). Even though it is a cost-effective model, the capacitor voltage balancing is difficult. To the same three-phase systems particularly for medium power application, (Araujo-Vargas et al., 2014) suggested a new archetype as depicted in Figure 1.26(b). The three-phase elements such as transformers and standard two-level inverter are built the circuit. Moreover, it could run with a neutral point clamped inverter in place of the conventional two-level inverter. Thus it gives flexibility for choosing appropriate inverter with three-phase transformers leads a quite simple production. A unique switching strategy is implemented with a simple 16-bit micro-controller to verify the presented topology, but the efficiency is slightly lower compared with other techniques. Thereupon (Choi and Kang, 2015) implemented a seven-level PWM inverter with single DC source. This arrangement is shown in the Figure 1.27(a). In fact, a unification of cascade H-bridges, diodes, active switches, series capacitors and single DC source is the presented configuration. Nevertheless, when the energy storage elements (like capacitors) are involved in the circuit, then voltage balancing issues will arise. Of course, the author carefully addresses this issue with a new control



(a)



(b)

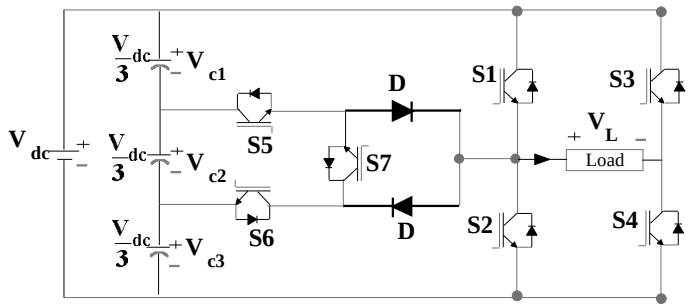
Figure 1.26: (a) Three phase single DC MLI with the minimum switches, (b) A single DC source seven level inverter.

algorithm. But still, it has the limited applications owing to the maximum voltage ratio (MVR) is one.

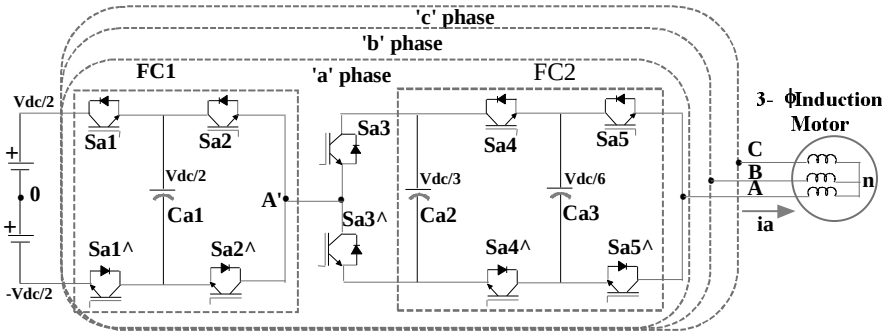
Next, (Sanjeevan et al., 2015) suggested an algorithm which works for every sampling instant to correct the capacitor voltage magnitude irrespective of the load power factor and modulation index (MI) for their new hybrid seven-level inverter as shown in Figure 1.27(b). The MLI employs two sets of three-level flying capacitor units cascading with H-bridge modules per phase. Furthermore, a voltage balancing technique is suggested based on the pole voltage redundancies of the inverter. Subsequently, a new MLI has arrived for four-pole induction-motor drive applications in the same family (Kumar and Sivakumar, 2015), see the Figure 1.27(c). Here, the circuit uses a small magnitude supply, but it leads a consequence of a severe power balancing issues. However, the authors addressed this issue; additionally, they suggested a modified SPWM approach to minimise the output zero-sequence voltages, which drops between the motor phase windings and power electronic switches.

1.4.4.1 Summary of single DC-source MLIs

Most of the single DC configurations are running with substantial transformers, inductors, and capacitors. The size and number of passive components have become more for three-phase systems. If the single DC structures configured without bulky devices, the topologies could be significantly used in power industries.



(a)



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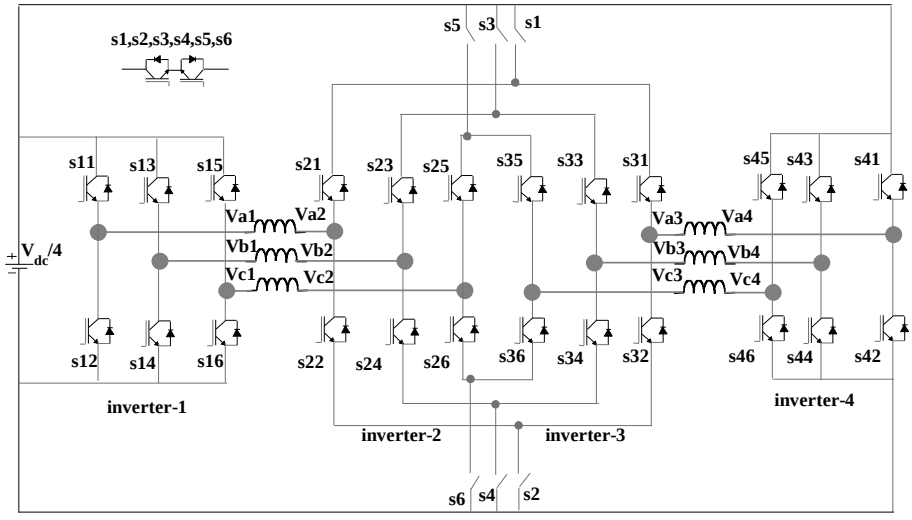

(c)

Figure 1.27: (a) Seven-Level PWM inverter employing series connected capacitors, (b) Reduced common mode voltage single DC seven level inverter, (c) A quad two-step inverter with single DC-source.

Table 1.6: Applications of available symmetric, asymmetric, hybrid and single DC-source based MLIs

Applications	Symmetric MLIs	Asymmetric MLIs	Hybrid MLIs	Single DC-source MLIs
power conditioning active filters	[1,2]	[8,9]	[19,20]	[25]
Hybrid electrical vehicles	[3]	[10]	[21,7]	[26,27,28]
FACTs controllers	[1,4]	[4,8,11]	[20]	[29]
Back to back frequency link systems	[Not Recommended(NR)]	[NR]	[22]	[29]
Renewable energy systems	[All]	[All]	[19,20,23]	[30,31,32,33]
HVDC	[1,5]	[12,13,10,8,11,14]	[9,18]	[NR]
Motor drives	[NR]	[NR]	[24,12,22]	[34,35]
Transportation	[5]	[15,16,17]	[19]	[26,36,37]
Telecommunication	[6]	[17,18]	[9]	[25]
Medical apparatus	[7]	[18]	[12]	[25]

1. Lai and Peng (1996)
2. Waltrich and Barbi (2010)
3. Choi and Kang (2009)
4. Babaei et al. (2007)
5. Mokhberdoran and Ajami (2014a)
6. Ebrahimi et al. (2012)
7. Hinago and Koizumi (2010)
8. Babaei et al. (2014b)
9. Babaei et al. (2012)
10. Lai and Shyu (2002)
11. Mokhberdoran and Ajami (2014b)
12. Manjrekar et al. (2000)
13. Choi and Kang (2015)
14. Samadaei et al. (2016)
15. Gupta and Jain (2012a)
16. Ounejjar et al. (2011)
17. Du et al. (2006)
18. Alishah et al. (2014)
19. Rech and Pinheiro (2007)
20. Khomfoi and Aimsaard (2009)
21. Ruiz-Caballero et al. (2010)
22. Rajeevan et al. (2011)
23. Nami et al. (2011)
24. Manjrekar et al. (1998)
25. Choi and Kang (2015)
26. Pereda and Dixon (2012)
27. Pereda and Dixon (2011)
28. Sepahvand et al. (2013)
29. Soto et al. (2003)
30. Kang et al. (2005)
31. Suresh and Panda (2010)
32. Saeedifard et al. (2012)
33. Banaei et al. (2012a)
34. Sanjeevan et al. (2015)
35. Kumar and Sivakumar (2015)
36. Tsang and Chan (2014)
37. Araujo-Vargas et al. (2014)

1.5 Research motivation

Although many MLI topologies from distinct categories (standard configurations to single DC source based MLIs) are reported in the literature, only a few of them are commercially manufactured and utilised. In fact, the manufacturers are considered the crucial factors such as an equipment cost, device count, maximum voltage blocking capability of the switches, reliability, protection, packaging, modularity, efficiency, and lifespan while making the device as per customer demand. Table 1.6 thoroughly dedicated for specifying the applications of each topology which have been investigated so far. The next important research area is a modulation technique which has been much attracting the research community for long years. In recent past, a huge number of modulation techniques are observed for controlling switching-states and balancing the isolated input supplies (or capacitors) of the pertinent topologies. However, choosing an appropriate switching strategy for a particular application and configuration is a challenging job.

On this line, the researchers are still working to investigate the new MLI configurations to synthesise possible topological variations for enhancing the structural and operational behaviour of the selected emerging converter families. Additionally, they have been aiming at developing suitable control strategies for switching the established MLI structures with a smooth operation. In fact, industries and academicians are always seeking the economical solution for any customer requirements and demands. From the technical point of view, there is still scope for further reduction in the device count of the existed topologies. Moreover, if the converters are running with efficient control algorithms provides additional privileges in terms of implementation and extendability. Based on these criterions, the following objectives are framed in such a way that the proposed MLI topologies should satisfy all the kinds of applications with the reduced part count. After that, the new control schemes with a simple methodology are also introduced for enhancing the operation and control of the newly proposed archetypes.

1.6 Thesis objectives

The main objectives of this thesis are:

1. To develop a new hybrid multilevel inverter using modified carrier SPWM switching technique.

2. To propose and verify a novel 19-Level inverter using an effective fundamental switching strategy.

3. To introduce a new multi-cell based CMLI with nearest level control technique.

1.7 Thesis organization

There are five chapters and two appendices in this thesis document. The outline of this thesis is highlighted in Figure1.28.

Chapter 1: Presents a brief introduction to state-of-the-art MLI topologies and in particular, critically reviews the MLIs with reduced part count and their associated intricacies concerning symmetric, asymmetric, hybrid and single DC structural configurations.

Chapter 2: Proposes hybrid 19L-MLIs which have reduced power circuit complexity. Besides, a modified level shift pulse width modulation technique is introduced to trigger the power IGBTs of the converter. Detailed simulation and experimental studies are carried out to validate the proof of controllability of the proposed topologies and its associated control system. Furthermore, the detailed loss analysis and comparison in terms of the number of power switches, DC sources, and their ratings are deliberated in detail.

Chapter 3: Proposes a single-phase cascaded transformer configuration which has further reduced power circuit complexity than chapter-2 presented topology. A simple fundamental switching strategy is developed so-called fundamental sine quantised switching strategy. Simulation and experimental results are exemplified to validate the proposed system. The proposed topology and control strategy is verified through experimentally for different quantisation interval magnitudes. The possible extensions of the proposed control algorithm for a higher level three-phase MLI are also described. Finally, a comprehensive comparative study with other well-established MLIs is included.

Chapter 4: In this chapter, a multicell MLI with reduced part count is proposed. A detailed simulation of a 25-level system with the nearest level control algorithm is elucidated. Following a thorough comparison with other MLIs, the results are presented.

Chapter 5: Summarizes the significant thesis contributions and includes some discussions on possible future research.

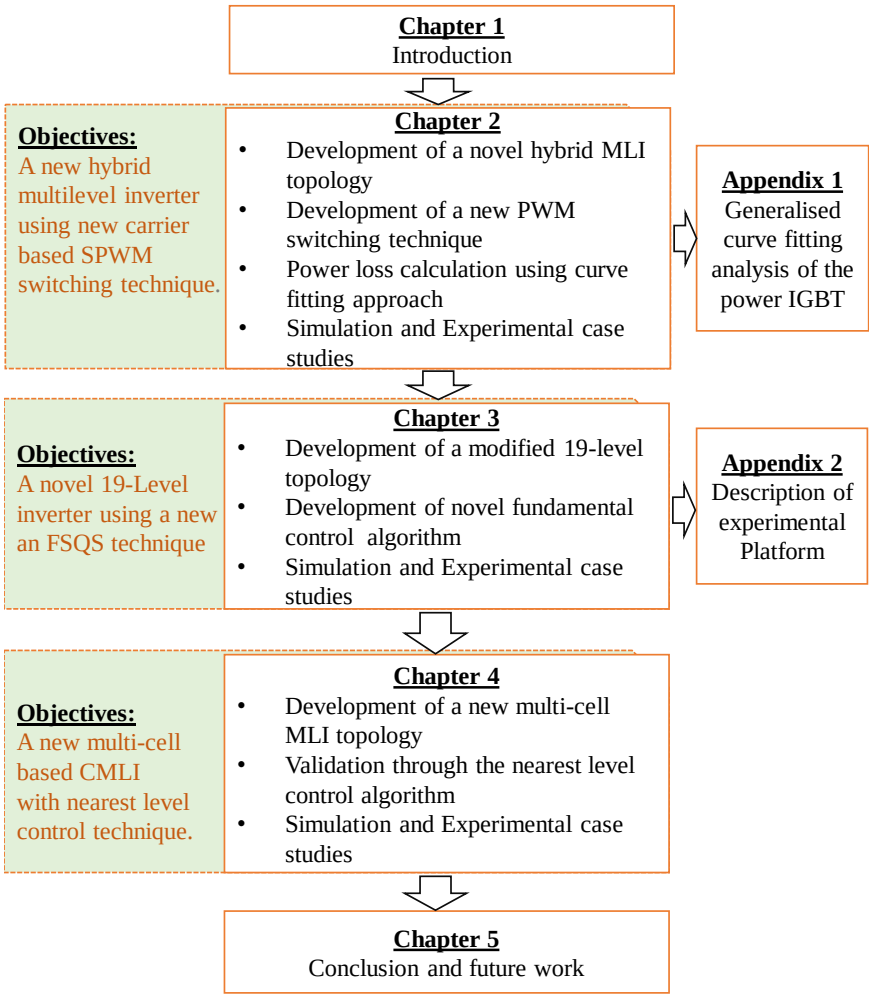

Figure 1.28: The outline of the thesis

Chapter 2

A NEW HYBRID MLI USING MODIFIED CARRIER SPWM TECHNIQUE

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2.1 Introduction

This chapter introduces a novel single-phase cascaded transformer MLI controlling with a level shift sinusoidal PWM (LS-SPWM) technique. It is a cost-effective solution for high voltage and medium power applications since the circuit has built with the least number of switching devices which further causes a cost reduction and reliability enhancement to the converter. Next, this chapter presents the level shift PWM approach accompanying a modified carrier for shifting and improving the dominant harmonics and the RMS value of output waveform consequently. Besides, the losses namely conduction, switching, core, iron and thermal losses are investigated to reveal the uniqueness of the present topology.

Firstly, the topological details of the proposed topology are described in detail followed by the new carrier-based PWM technique. Secondly, a total loss investigation of the converter is studied. Finally, the performance of the proposed topology is validated with MATLAB-Simulink software and the experimental setup.

2.2 The proposed 19-level inverter configuration synthesis

Figure 2.1 shows the schematic representation of the proposed nineteen level inverter. It has two parts as per the circuit concern, one called as Bridge-A & other named as Bridge-B. The Bridge-A develops the voltage waveform having three levels, and the Bridge-B is a low voltage bridge establishes a seven-level PWM waveform. The principal idea under the utilisation of the transformers [Bridge-A transformer (Tr-a) and Bridge-B transformer (Tr-b)] in both bridges is to accomplish a maximum number of levels without using additional switches and separate DC sources leading to the better efficiency, reliability and economic improvement. The considered switches are insulated-gate bipolar transistors (IGBTs) with an anti-parallel diode for allowing the current in both directions and block the voltage on only one side, and it is typically a bidirectional-unipolar semiconductor switch. The purpose of the anti-parallel diode (D) in the circuit to allow the negative current of the switch, and the IGBT (sw) is permitting the positive current. Regarding the input DC supply, the magnitude of source V_1 should be twice the magnitude of source V_2. In fact, the magnitude determination of the DC sources and transformer ratios (1:2 and 1:1)

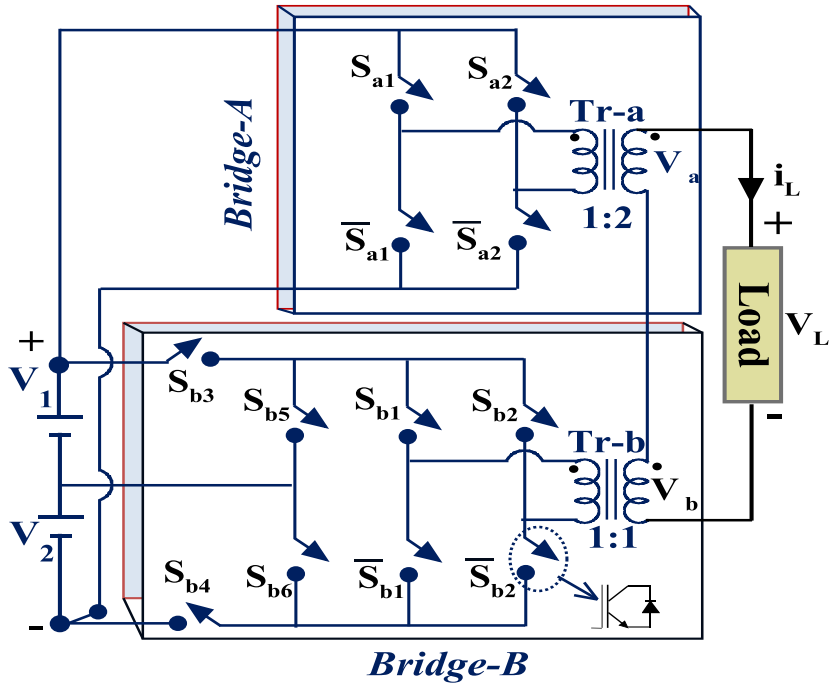


Figure 2.1: The diagrammatic presentation of the proposed nineteen level inverter

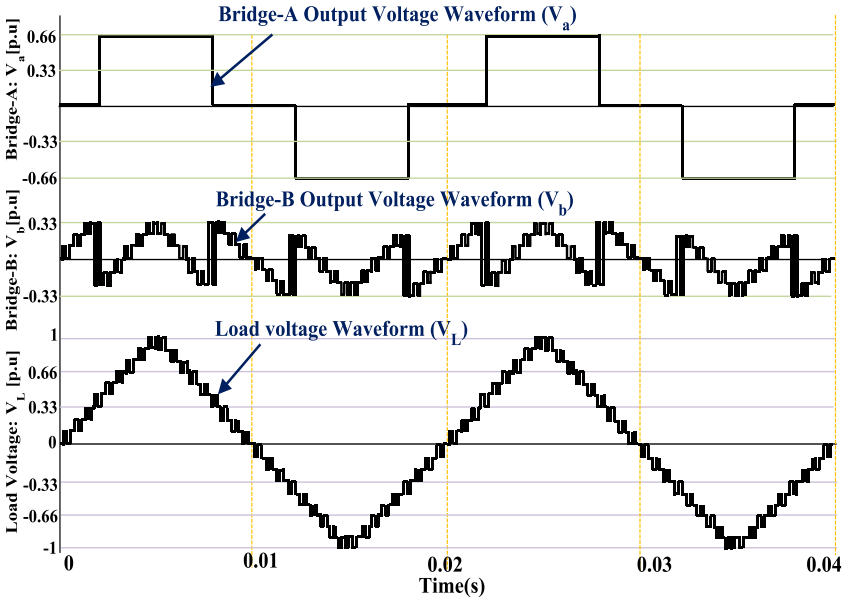


Figure 2.2: Key voltage waveforms of the 19-level topology

plays a vital role in realising the more number of output voltage steps. Moreover, the load and secondary currents of the transformers should be the same. Because, the secondaries of two transformers are shorted by the load. The Figure 2.2 presents a key output voltage waveforms of the Bridge-A, Bridge-B, and load voltage. Here the interesting fact stands on an appearance of the all current waveforms, i.e., load, primary and secondary currents of the transformers accomplishes 19-level waveforms. If that elaborates in detail, the actual Bridge-A output voltage (V_a) is a quasi-square waveform means three-level waveform and the corresponding primary and secondary current waveforms possess 19-levels. Similarly, the Bridge-B output voltage (V_b) is an uneven waveform (7-level), though the associated primary and secondary current waveforms accommodate 19-levels. It insists that in some of the switching states of the converter produces the positive operating voltage and negative currents or vice versa rather than the same polarity of operation in between the voltage and current waveforms of the transformers. The individual switching states of the proposed topology are exposed in Table 2.1. Let us consider V_{dc} is equal to the magnitude of V_2 (input DC source).

- First state: this level is designated as 1L, switches S_{a1},S_{a2} of Bridge-A and S_{b1}, , $\bar{S}_{b2}$, S_{b4} and S_{b5} of Bridge-B are ON, Thus, the load voltage V_L=0+V_2=V_{dc}.

- Second state (2L): Switches S_{a1}, S_{a2} of Bridge-A are involved to short the transformer-A primary windings and S_{b1}, $\bar{S}_{b2}$, S_{b3} and S_{b6} of Bridge-B are ON, then V_1 DC source is connected to the Bridge-B, Thereby, voltage across the load becomes V_L=0+V_1=2V_{dc}.

- Third state (3L): Switches S_{a1} and S_{a2} of Bridge-A are involved to short the transformer-A primary windings and then S_{b1}, $\bar{S}_{b2}$, S_{b3} and S_{b4} of Bridge-B are ON, afterthat V_1 and V_2 DC sources are connected to the Bridge-B to get the load voltage V_L=V_1+V_2=3V_{dc}.

- Fourth state (4L): from this state the Bridge-A starts to share the load power. Switches S_{a1}, $\bar{S}_{a2}$ of Bridge-A and $\bar{S}_{b1}$, S_{b2}, S_{b3} and S_{b6} of Bridge-B are ON, thus, the load voltage V_L=2(V_1+V_2) + (-V_1) = 6V_{dc} - 2V_{dc} = 4V_{dc}. The Bridge-A output peak voltage magnitude is bounced from 3V_{dc} to 6V_{dc} since the turns ratio of Tr-a is contemplated as 1:2.

- Fifth state (5L): Switches S_{a1},$\bar{S}_{a2}$ of Bridge-A and $\bar{S}_{b1}$, S_{b2}, S_{b4} and S_{b5} of Bridge-B are ON, Thus, the load voltage V_L=2(V_1+V_2) + (-V_2) =6V_{dc} - 1V_{dc}=5V_{dc}.

- Six state (6L): Switches S_{a1},$\bar{S}_{a2}$ of Bridge-A and S_{b1}, S_{b2} of Bridge-B is activated to attains the load voltage V_L=2(V_1+V_2) + 0 = 6V_{dc}.

- Seventh state (7L): Switches S_{a1},$\bar{S}_{a2}$ of Bridge-A and S_{b1},$\bar{S}_{b2}$, S_{b4}, S_{b5} of Bridge-B are ON, Then the voltage across the load is V_L=2(V_1+V_2) + (V_2)= 6V_{dc} + 1V_{dc}= 7V_{dc}.

- Eighth state (8L): Switches S_{a1},$\bar{S}_{a2}$ of Bridge-A and S_{b1},$\bar{S}_{b2}$, S_{b3}, S_{b6} of Bridge-B are ON, Thus, voltage across the load is V_L=2(V_1+V_2) + (V_1)= 6V_{dc} + 2V_{dc}= 8V_{dc}.

- Ninth state (9L): Switches S_{a1},$\bar{S}_{a2}$ of Bridge-A and S_{b1},$\bar{S}_{b2}$, S_{b3}, S_{b4} of Bridge-B are ON to possess the load voltage V_L=2(V_1+V_2) + (V_1+V_2) =6V_{dc} + 3V_{dc}= 9V_{dc}.

- Zeroth State (0L): this state can achieve in different combinations, herein, switches S_{a1} and S_{a2} of Bridge-A and S_{b1}, S_{b2} of Bridge-B are ON to generate zeroth load voltage state.

Similarly, the negative states (from -1L to -9L) of the load voltage waveform are achieved with an appropriate switching. Herein, Bridge-B operated at PWM mode, and Bridge-A is modulated with the fundamental frequency. The primary intention behind the operation is to reduce overall conduction and switching losses of the proposed topology. Later, the circuit can be extended to 'N' number levels in two possible ways. The first possible way is by adding additional DC sources in Bridge-B symmetrically. In this case, the number of voltage levels (N_L) is related to the number of DC sources (N_{DC}) which is given in equation 2.1.

$$N_L = 6N_{DC} + 1 \tag{2.1}$$

Another way is to choose the magnitudes of the DC supplies in the following asymmetrical method, where all DC sources are twice the magnitude of the K^{th} DC source (V_K). i.e., $V_1 = V_2 = ...= V_{(K-1)} = 2V_K$. For this arrangement, the number of levels is given by an equation 2.2.

$$N_L = 12N_{DC} - 5 \tag{2.2}$$

Table 2.1: Switching states of the positive 19-level waveform of the topology

V_L	S_{a1}	S_{a2}	V_a	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	V_b
1L	sw	D	0	sw	0	0	sw	D	0	1L
2L	sw	D	0	sw	0	sw	0	0	D	2L
3L	sw	D	0	sw	0	sw	sw	0	0	3L
4L	sw	0	6L	0	D	D	0	0	sw	-2L
5L	sw	D	6L	0	D	0	D	sw	0	-1L
6L	sw	D	6L	sw	D	0	0	0	0	0
7L	sw	0	6L	sw	0	0	sw	D	0	1L
8L	sw	0	6L	sw	0	sw	0	0	D	2L
9L	sw	0	6L	sw	0	sw	sw	0	0	3L
0	sw	D	0	sw	D	0	0	0	0	0

2.3 Proposed switching scheme

The stated switching criterion originates from the Level Shift Pulse Width Modulation (LS-PWM) technique family. According to the phase position of the carrier waveforms, the LS-PWM are classified into three types so-called Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD). Among the three varieties, the POD is a strong competitor to the other approaches (Tolbert and Habetler, 1998). Later, the triangle and ramp carrier waveforms are widespread in all carrier-based PWM techniques, but high carrier frequency (f_{cr}) is considered to curtail the lower order harmonics. On the contrary, for higher f_{cr} values, the switching and EMI issues are severely affecting the operation and control of the converter. Hence, the carrier frequency is negotiated as a significant factor to address the problems described above. By keeping this in mind, a new carrier waveform is proposed to override the traditional carriers for suppressing lower order harmonics. In the present section, the demonstration of proposed technique is explained in detailed. Let's consider a carrier waveform with too higher frequency and the 50 Hz fundamental sine reference signal (V_{ref}). It is noted that the reference waveform is visible as a constant DC signal to the carrier waveform at a high carrier frequency. Always the number of carriers depends on the output level count, e.g., 'N_L'levels needs 'N_L-1'carriers. Thus, 18-carrier signals are considered to perform the POD technique for the proposed 19-level configuration as portrayed in Figure 2.3. In fact, any multilevel voltage waveform mathematically expressed in terms of DC offsets, fundamental and its sideband harmonics, carrier harmonics and its sideband harmonics (McGrath and Holmes, 2002).

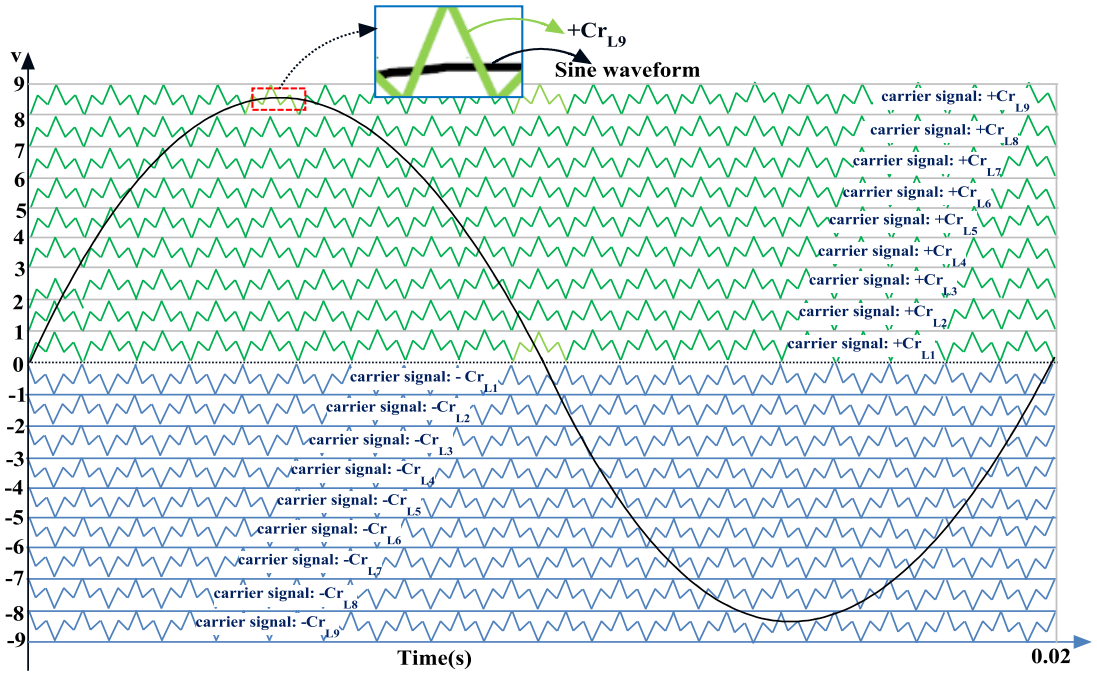


Figure 2.3: Schematic arrangement of the POD-PWM strategy with proposed carrier and sinusoidal reference waveforms

$$\begin{aligned} \mathrm{V(t)} = \frac{A_{00}}{2} &+ \sum_{q=1}^{\infty} A_{0\mathrm{q}} \cos(q\omega_0 t) + B_{0\mathrm{q}} \sin(q\omega_0 t) \\ &+ \sum_{p=1}^{\infty} A_{\mathrm{p}0} \cos(p\omega_c t) + B_{\mathrm{p}0} \sin(p\omega_c t) \\ &+ \sum_{p=1}^{\infty} \sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty} A_{\mathrm{pq}} \cos(p\omega_c t + q\omega_0 t) + B_{\mathrm{pq}} \sin(p\omega_c t + q\omega_0 t) \end{aligned} \tag{2.3}$$

The coefficients of equation 2.3 are obtained for the general PWM strategy by calculating the double Fourier integral of

$$A_{pq} + jB_{pq} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} V(y,z) e^{j(py+qz)} dydz \tag{2.4}$$

where $y = \omega_c t$, $z = \omega_0 t$.

The equation 2.3 is evident that the carrier shape can mathematically decide the

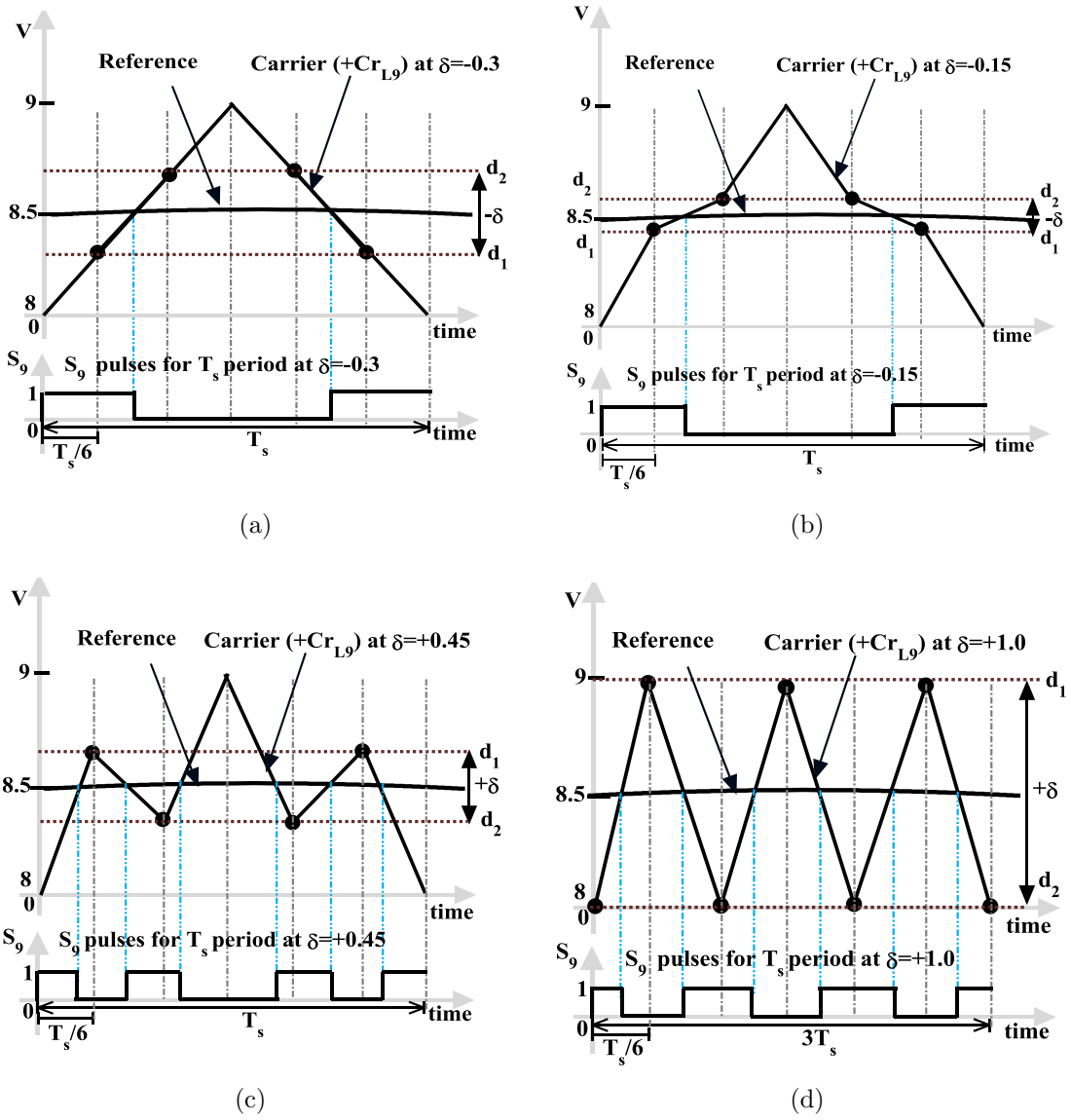


Figure 2.4: Developing S_9 pulse train for the proposed carrier constraints (a) m_f =20 and delta =-0.3; (b) m_f =20 and delta =-0.15; (c) m_f =20 and delta =+0.45; (d) m_f =60 and delta =+1.

existence of the harmonics in the multilevel output waveform. Hence, the present work concentrates on designing a novel carrier that to from the conventional carrier (Triangular) without changing the frequency and peak to peak magnitude.

Consider the triangle waveform with the frequency $1/T_s$ and splits equally into six parts by the time scale $T_s/6$ which is shown in Figure 2.4 (a). The carrier and reference waveforms consider in Figure 2.4 (a) can generate the positive 9^{th} level corresponding pulses called S_9. Similarly, other carrier waveforms shown in Figure 2.3 are compared with a reference waveform to produce relevant pulses for the dismissed output levels. The positive slope of the carrier (first halftime period of the triangle) intersects the voltage magnitude lines d_1 and d_2 at the $T_s/6$ and $2T_s/6$ timing instants. The difference between the two crossover points is noted as Delta (δ).

$$Delta(\delta) = d_1 - d_2 \tag{2.5}$$

Whenever the magnitude of δ varies, the number of pulses and width of the chops will be altered accordingly. It can be demonstrated in the following figures, Figure 2.4 (a), (b),(c) and (d). Primarily, the polarity of the δ arrives -0.3 in Figure 2.4 (a) which exactly represents a triangle carrier signal. The association of the carrier and reference waveforms delivers pulse train S_9 with only two pulses. Regarding the second case $\delta = -0.15$ attains the same chops, but a width of pulses are different see in Figure 2.4 (b) . In the third instant, the δ becomes a positive ($\delta = +0.45$) value. Furthermore, the number of hitting instants with reference waveform is also higher leading to get more chops without changing the carrier frequency (that is still $1/T_s$ only) is shown in Figure 2.4 (c). In the same way, if the carrier functions at $\delta = 1$ then its frequency becomes triple as shown in Figure 2.4(d) and also the shape is very close to a triangle. The number of chops per carrier period depends on the polarity of the delta. It means S_9 attains more pulses for positive δ values rather than the negative values. Furthermore, the positive delta decreases harmonic content as well as raises the fundamental magnitude of the output voltage.

An implementation of the proposed POD-PWM strategy to trigger bridge-A and bridge-B of the stated configuration is depicted in Figure 2.5. The gating pulses of the 19-level converter are accomplished with eighteen carrier waveforms. Moreover, the positive nine carrier waveforms (from $+Cr_{L1}$ to $+Cr_{L9}$) are out of phase with the negative nine waveforms (from $-Cr_{L1}$ to $-Cr_{L9}$). But, all these carrier wave-

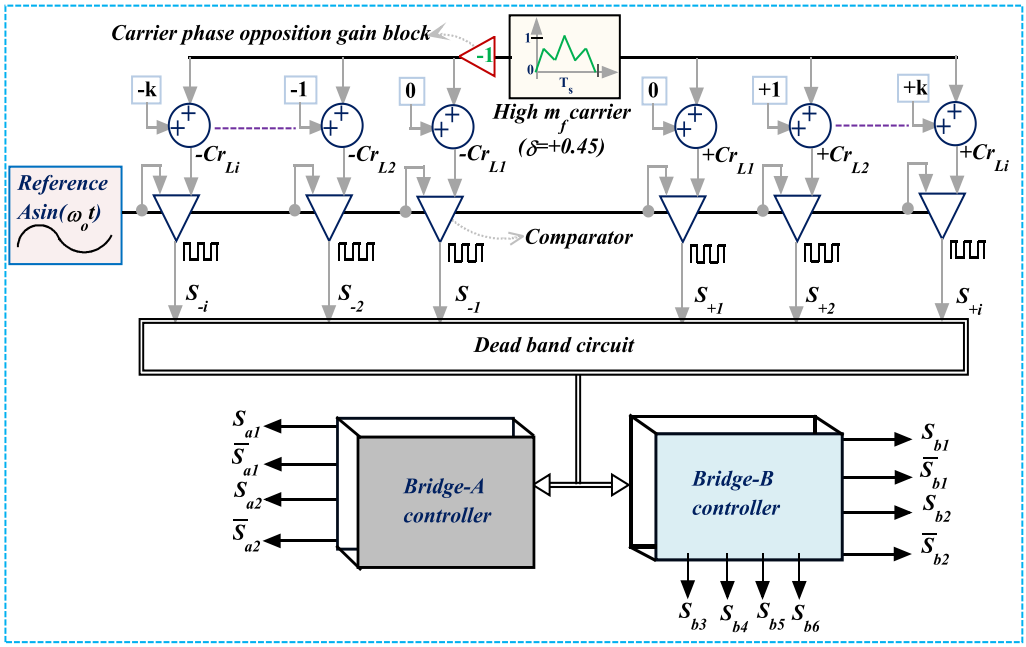


Figure 2.5: The process of implementing the developed switching technique for proposed nineteen level topology

forms are established with only one waveform. From the comparator which compares the fundamental sinusoidal reference waveform with the proposed carrier waveforms provides initial driving pulses ($-S_9$ to $+S_9$). Later, the dead band circuit is allotted to avoid the shoot through faults between the complementary switches. Finally, the actual pulse trains of the bridges (S_{a1}, S_{a2}, S_{b1},S_{b2}, etc.) are developed by proper logical combination among the initial driving pulses.

The Table 2.2 describes an effect of the factors like % THD, peak magnitude (V_p) and dominant harmonic (n) of the 19-level output voltage waveform by changing delta magnitudes with 0.15 variation. While investigating all these cases, the amounts of significant parameters are chosen as Modulation index (m_a) = 1, Frequency modulation index (m_f) = 20, Input DC sources $V_2 = 36V$, and $V_1 = 72V$. Finally, three remarkable cases are found at $\delta = -0.3, 0.45\&1$.

- Case 1 ($\delta = -0.3$): This case is treated as conventional carrier-based PWM technique since the carrier shape a triangle. The fundamental peak of load voltage (V_p) is 327.7V, and the dominant harmonics are 21^{st} and 19^{th} orders at 1 kHz switching frequency.

Table 2.2: The performance of the proposed MLI by varying the delta magnitude

δ	$\%THD$	$V_p(V)$	$h_{domin}(n)$	Shape of the Carrier
-0.3	5.97	327.7	21,19	$Triangle\,(m_f = 20)$
-0.15	5.66	328	21,19	-
0.15	5.05	328.1	21,19	-
0.3	5.13	327.2	21,61	-
0.45	**5.29**	**326.3**	**61,59**	$Proposed\,(m_f = 20)$
0.6	5.37	325.5	59,61	-
0.75	5.50	325	59,61	-
0.9	5.64	324.4	59,61	-
1	5.67	324.8	59,61	$Triangle\,(m_f = 3 \times 20)$

- Case 2 ($\delta = 0.45$): In this case, output waveform achieves better THD than case-1, i.e., 5.29%, and the carrier frequency is still 1 kHz. Moreover, the dominant harmonics are shifted to 61^{st}, 59^{th} order.

- Case 3 ($\delta = 1$): It also treated as a traditional carrier-based PWM technique since the carrier shape is a triangle. Even though the given carrier frequency is 1 kHz, the switching frequency becomes triple since the delta magnitude is +1. Besides, the V_p value is lesser than case-2, and switching stresses are also high.

Lastly, it is observed that the carrier waveform presented in case-2 has prominent features like (i) reduction in switching and conduction losses (P_{sw} and P_c), (ii) improves the FFT spectrum, (iii) rise in peak magnitude of the load voltage and (iv) diminish the filter size. Therefore the system becomes more efficient than the implementing with a traditional LS-SPWM schema.

2.4 Power loss calculation

The converter is an assemble of transformers and IGBT switches. Normally, the transformer yields an eddy current and hysteresis losses when it is subjected to an alternative flux. However, a thin laminating and high-grade silicon core can depreciate the transformer losses. Likewise, a semiconductor switch generates a switching and conduction losses. All the losses are studied to find the complete loss profile of the MLI for arranging the proper cooling system.

2.4.1 Conduction losses of the semiconductor devices

The conduction and switching losses of the semiconductor switches are reported in this section to analyze the performance of the suggested converter. Usually, the loss analysis of the switch can be done in multiple ways, but numerical circuit simulation method is widely accepted since a practical switch data-sheet carries the evaluation process. The proposed configuration is built with SKM75GB123D IGBT switches, if the positive current is flowing through the switch, then the IGBT is shorted or else an anti-parallel diode (D) will conduct.

The conduction loss equations of the transistor (P_{igbt}) and anti-parallel diode (P_D) are deduced from the curve fitting graphs which are illustrated in Appendix-1. The loss equations are laid out from equation 2.6 to 2.9.

$$P_{igbt,25^0} = 0.02365 \times i_c^2 + 1.551 \times i_c - 0.8995 \tag{2.6}$$

$$P_{igbt,125^0} = 0.02876 \times i_c^2 + 1.914 \times i_c - 2.452 \tag{2.7}$$

$$P_{D,25^0} = 0.01521 \times i_f^2 + 1.245 \times i_f - 0.2321 \tag{2.8}$$

$$P_{D,125^0} = 0.01485 \times i_f^2 + 1.06 \times i_f - 0.8451 \tag{2.9}$$

Where i_f is a diode forward current and i_c is a transistor collector current. Basically, the switch losses are depended on the temperature, and thereby the conduction losses are also affected by a junction temperature (T) leading to revise the coefficients of the equations in terms of junction temperature. It is evident that the data sheet of the switch should provide two temperatures (min and max) based I-V curves. Otherwise, the temperature dependent loss analysis will not be possible. At last, the coefficients are determined from the first order approximation system (Drofenik and Kolar, 2005), and final equations presented as follows

$$\begin{aligned} P_{igbt}(i_c, T) = {} & (0.0224 + 0.000058 \times T)i_c^2 + (1.46025 + 0.00363 \times T)i_c \\ & - (0.511375 + 0.015525 \times T) \end{aligned} \tag{2.10}$$

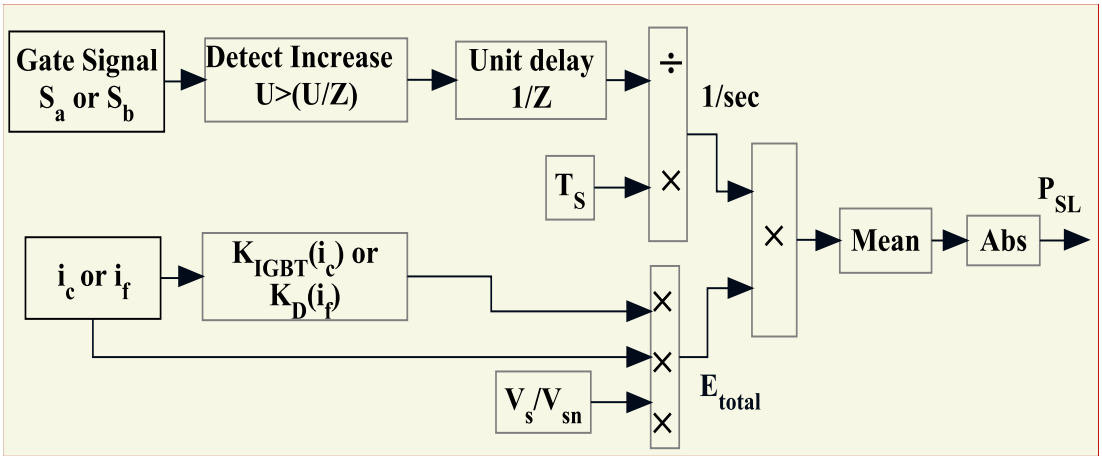


Figure 2.6: Schematic diagram of switching loss P_{SL} calculations

$$P_D(i_f, T) = 0.0153 i_f^2 + (1.2913 - 0.0019 \times T) i_f - (0.0789 + 0.0061 \times T) \quad (2.11)$$

2.4.2 Switching losses of the semiconductor devices

As per the switching loss concern, the current flowing through the switch and its pulse train are the primary inputs to calculate switching losses of the device. The switching loss factor of the IGBT ($K_{IGBT}(i_c)$) or diode ($K_D(i_f)$) is equal to the ratio of the total energy loss (E_{total}) and the current flowing through the device (either i_c or i_f) at the maximum temperature (125^0). The factors of the IGBT and anti-parallel diode are presented in equations 2.12 and 2.13 based on the curve fitting approach.

$$K_{IGBT}(i_c) = 0.0001487 \times i_c^3 - 0.03366 \times i_c^2 + 3.224 \times i_c + 170.3 \quad (2.12)$$

$$K_D(i_f) = -0.0007726 \times i_f^2 - 0.436 \times i_f + 65.53 \quad (2.13)$$

The units of the switching loss factor is $\frac{\mu Watt-sec}{Ampere}$ or $\frac{\mu joule}{Ampere}$.

A schematic switching loss diagram is shown in Figure 2.6. Each rising edges of the pulse train (S_a or S_b) are identified by the detect-increase block from the Simulink library. Actually, the rise-detector block shifts the signal with on unit time step; therefore the unit delay block is added to bring it back to its original position otherwise the final result would be zero. The parameter T_s is a width of the each detected pulses, and usually, it is the sampling time of the system. Afterward, the

Table 2.3: Simulation parameters of the proposed setup

Parameter	Ratings
Modulation index (m_a)	1
Delta (δ)	0.45
Carrier frequency (f_c)	1.5KHz
DC source (V_1)	72V
DC source (V_2)	36V
Power factor (pf)	0.9
Load (P_L)	0.5KW
Load voltage ($V_L(rms)$)	230V
Load inductance (L)	163mH
Load resistance (R)	105.8Ω
Transformer-a	380VA,50Hz
Transformer-b	120VA,50Hz

sampling time (T_s) divides the signal and it's units become sec^{-1}. On another side, two current sensors per switch are needed to sense the IGBT collector current (i_c) and antiparallel diode current(i_f). The identified ones have to monitor in order to find the corresponding switching loss factors ($K_{IGBT}(i_c$ or $K_D(i_f)$). Next, the voltage ratio factor (V_s/V_{sn}) is considered to attain a great approximation in loss calculations. Herein, (V_s) and (V_{sn}) are the operating and maximum blocking voltages of the switching devices. Finally, the converter switching loss (P_{SL}) is determined by adding all individual switching losses of the devices.

2.5 Simulation results

A list of the system parameters presented in Table 2.3 is considered to confirm the validity of the proposed topology with an advanced PWM technique. The isolated gate pulses are required only for eight switches because the switches S_{a2},S_{a4},S_{b2} and S_{b4} are complimentary switches of S_{a1}, S_{a3}, S_{b1} and S_{b3} successively. Furthermore, the VA ratings of transformers are 78% and 22% of the full load power for Tr-a and Tr-b sequentially which is leading to construct a cost-effective system. Moreover, a PWM mode of operation is carrying by the low rated bridge (Bridge-B), thereby the voltage stress of the switching components during high switching frequency instants will not deteriorate the overall performance of the configuration for long-run operations.

As per the waveform concern, the Bridge-A produces a three-level waveform (V_a) shown in Figure 2.7 (a), and Bridge-B accomplishes a seven-level uneven waveform

(V_b) which is exposed in Figure 2.7 (b). The peak values of the V_a and V_b are 216 V and 108V continuously. Later, the secondary windings of the two transformers are connected in series through the load, and hence the load waveform upgrades to a 19-level waveform as shown in the Figure 2.7 (c). Further, the load current waveform lags 25.84^0 behind the load voltage as displayed in the Figure 2.7 (d), and it's RMS value is 1.955A. Here the load current attained pure sinusoidal, due to the inbuilt impedances (load and transformer). The analytical calculations gives an active power 450W, and the simulation provides 446.5W for the given system parameters. The difference of the active power is treated as a loss of the converter which is very negligible.

The presented control scheme mainly affects the total harmonic distortion in an output voltage V_L shown in Figure 2.7 (e) where 19 level output waveform attains 5.81% THD and $V_L(peak) = 323V$. The harmonic spectrum of all possible load voltage levels 5, 7, 9, 11, 13, 15, 17 and 19 with respect to m_a are exposed in the Figure 2.8 (a). The conduction and switching losses of each semiconductor device in the circuit are exposed in Figure 2.8 (b). Herein, Bridge-A possesses higher conduction losses because of fundamental switching and Bridge-B has greater switching losses than another one due to it's PWM operation.

2.6 Experimental results

The laboratory prototype of the converter is constructed to verify the proposed topology with an advanced controlling technique. Herein, SKM75GB123D half-bridge IGBT modules, two linear CRNGO core transformers (Tr.1: 200VA, Tr.2: 100VA), and an Aplab dual DC power supply to provide an input DC sources ($V_1 = 30V$ and $V_2 = 15V$) and TLP-250 optocouplers are used to make the proper gate driver circuits. Further, the OP5142-RT simulator merely considered as a controller with a simulation time $50e^{-6}$. The details of the OP5142-RT simulator is presented in the Appendix-2.

Presently, the output waveforms of the proposed circuit are shown in Figure 2.9 for five modulation index (m_a) values. The Figure 2.9(a) carries Bridge-A, Bridge-B and load voltages of the submitted topology for $m_a = 0.085$. It is evident that, if m_a changes, the power-sharing between the bridges will vary accordingly (Kang et al., 2005). Even though the Figure 2.9(b) attains seven level across the load for $m_a = 0.25$, the Bridge-A could not feed the load since it is not generating any voltage waveform.

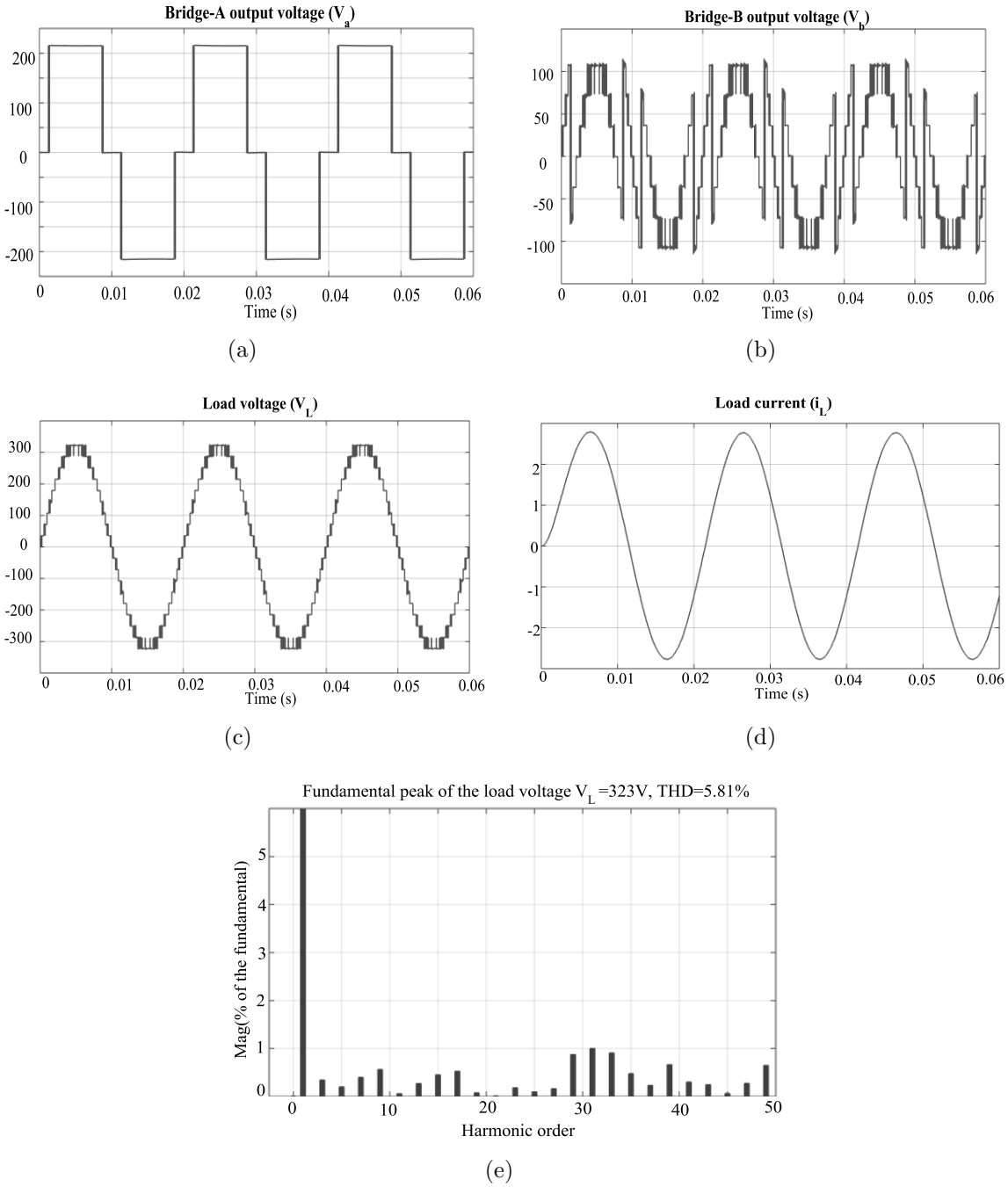
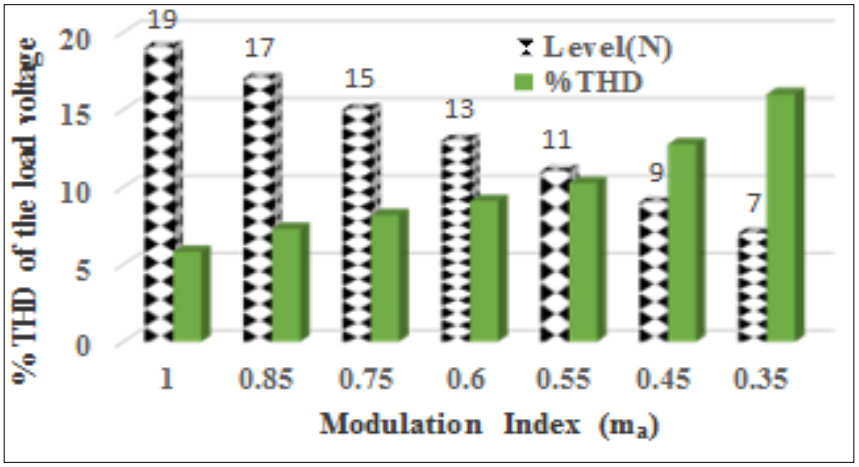
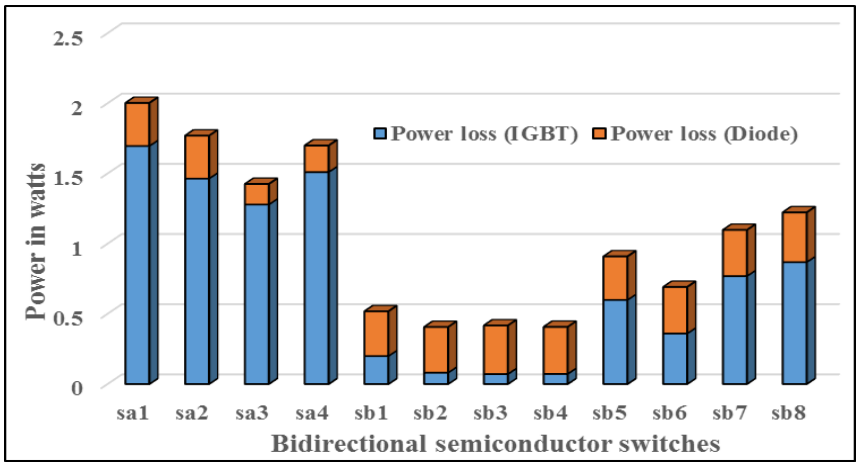


Figure 2.7: Simulation results: (a) Bridge-A output voltage V_a, (b) Bridge-B output voltage V_b, (c) Load voltage V_L, (d) Load current i_L. (e) % THD of the load voltage V_L.



(a)



(b)

Figure 2.8: (a) Effect of the modulation index on %THD and number of levels (b) Power losses of the switches for three delta values

Till $m_a > 0.3$, the transformer-B is the only candidate bearing the total load, and its power handling capability is also less approximately 22% of the rated load. Next, in the Figure 2.9(c), (d) and (e) both the bridges participated in compiling the load waveform.

Further an important practical issues about the transformers when fed with low-frequency waveform creates heating issues. This further effects efficiency of a converter. However, if winding currents are sinusoidal, additional losses can be minimised. On the other side, the presence of the transformer in the proposed design ensures, (i). Less voltage and current rating switches, (ii). Drastically minimises voltage stresses, (iii). Eliminate higher order harmonics, (iv). Provide inbuilt isolation, and (v). Matches the voltages between a source and line (Flores et al., 2009). Afterwards, the proposed MLI holds 19-level load voltage waveform as shown in Figure 2.9 (e) at $m_a = 1$ and 180V, 90V, 270V, 7.3A are the peak-peak magnitudes of V_a, V_b,V_L and i_L sequentially.

The harmonic spectrum of the 19-level load voltage is displayed in Figure 2.10; herein the load voltage has achieved 4.97% THD without any additional filter, and the driving switching frequency is 1.5 kHz. The load parameters of the values $R = 36\Omega$ and $L = 70mH$ are taken to evaluate the presented topology.

2.7 Comparative study

The proposed topology is compared with those presented in the literature regarding switch count, transformers, DC supplies and peak inverse voltage (PIV), etc.

- Switch count: As it can be seen from the Table 2.4 the proposed 19-level inverter requires the least number of the switches. Though the topologies Kang et al. (2005), Gupta and Jain (2012a) needs the same number of switches, the number of levels are lesser than the proposed one.

- Transformer and DC source count: It is inferred from the Table 2.4 that both transformers and DC supplies need only two numbers for generating 19-level output voltage waveform.

- PIV and ratings of the switches: The peak inverse voltage of the proposed converter has the least magnitude followed by the Kang et al. (2005), Behara

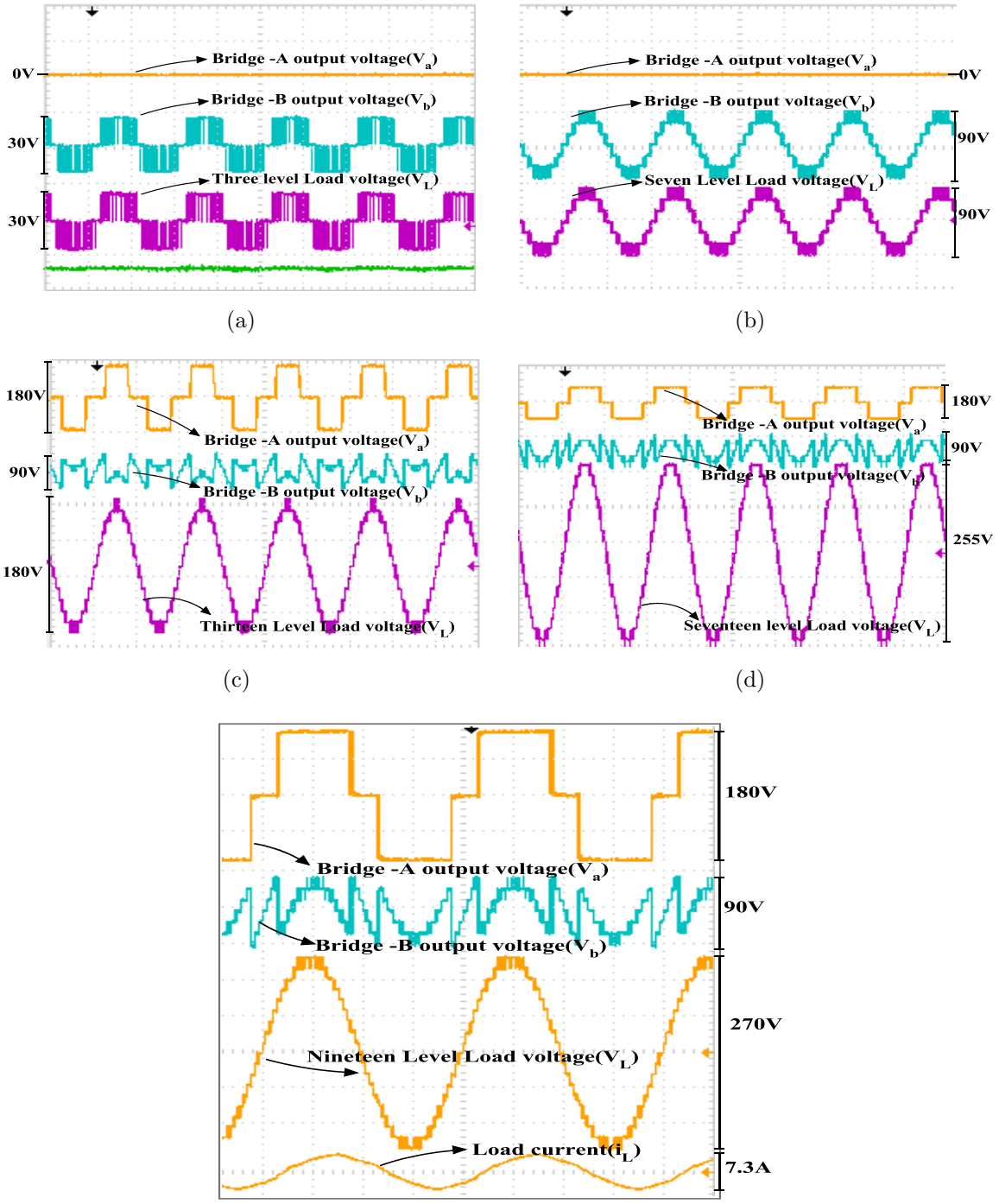


Figure 2.9: (a) Bridge-A output voltage (V_a), Bridge-B output voltage (V_b) and Load voltage (V_L) at $m_a = 0.085$; (b) Bridge-A, Bridge-B and Load voltages at $m_a = 0.25$;(c) Bridge-A, Bridge-B and Load voltages at $m_a = 0.52$; (d) Bridge-A, Bridge-B and Load voltages at $m_a = 0.81$; (e) Bridge-A, Bridge-B and Load across voltages, Load current (i_L) waveforms at $m_a = 1$.

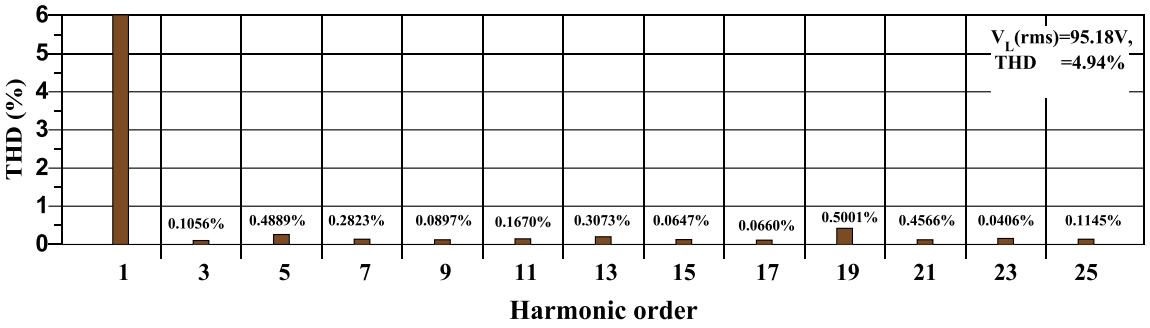


Figure 2.10: FFT spectrum for load voltage (V_L) at $m_a = 1$

Table 2.4: Device count of the proposed topology with other structures

	Recent MLI configurations					
	1	2	3	4	5	**Proposed**
Number of levels	11	19	19	19	15	**19**
Number of DC-sources	1	1	1	5	3	**2**
Number of IGBT-switches	12	20	20	14	12	**12**
Gate drivers	12	20	20	14	12	**12**
PIV	$1V_{dc}$	$9V_{dc}$	$1V_{dc}$	$9V_{dc}$	$7V_{dc}$	$3V_{dc}$
Number of transformers	3	9	9	0	0	**2**

1. Kang et al. (2005)
2. Banaei et al. (2012b)
3. Behara et al. (2016)
4. Babaei and Hosseini (2007)
5. Gupta and Jain (2012a)

et al. (2016). Even though the topologies Kang et al. (2005) and Behara et al. (2016) have the least PIV switches, the number of required transformers are more than the proposed topology. Furthermore, the proposed MLI can be extended to three-phase system where the number of transformers further reduced to 2-three phase transformers instead of six single-phase transformers.

2.8 Summary

This chapter presented a novel single-phase HMLI which employed low-frequency transformers for boosting output voltage levels and provides isolation between the

load and supply. The performance of the proposed MLI is investigated with a new carrier-based LS-SPWM technique. The proposed topology is achieved 19-level PWM output waveform with only two simple bridges. Moreover, the offered switching technique plays a significant role to improve the FFT spectra of the output waveform with the minimum switching frequency. All these features recommend the proposed configuration towards active filters, var compensators, and grid-connected applications.

It is noted that the fundamental switching approaches are also having equal importance along with PWM strategies. Therefore, we have introduced an easiest and novel fundamental switching method along with a new topology in the next chapter in detailed.

Chapter 3

AN NOVEL FUNDAMENTAL SWITCHING STRATEGY FOR A 19-LEVEL INVERTER

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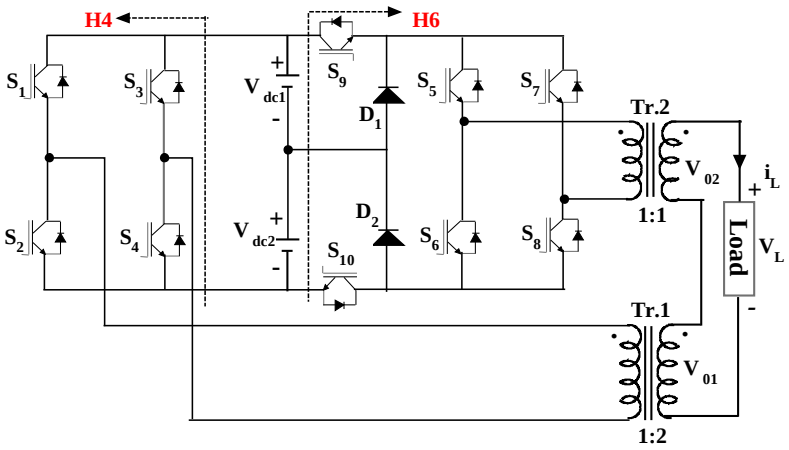
3.1 Introduction

In the earlier chapter, a single-phase 19-level inverter with a new PWM scheme is developed in the view of medium power applications. In this chapter, the same circuit is modified for low voltage applications. Unlike PWM control, a new fundamental switching is developed to control the proposed configuration.

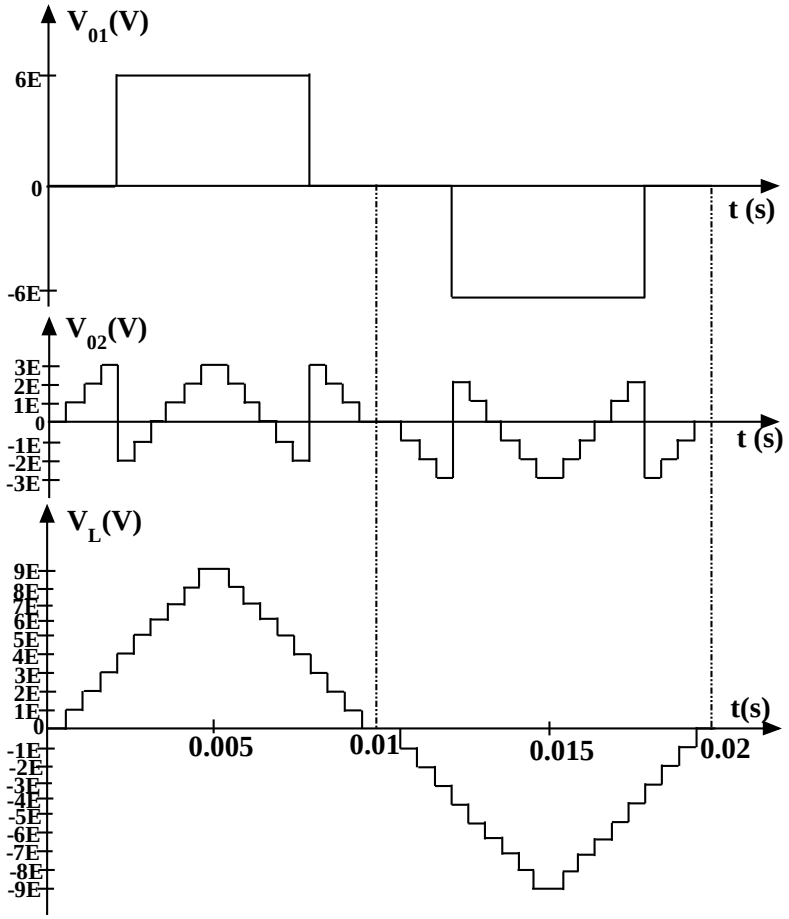
This chapter is organized as follows: Firstly, the topological synthesis of the proposed circuit is done on the basis of previously presented configuration followed by detailed investigation of a new switching approach so-called a fundamental sine quantiser switching technique (FSQST). Secondly, the adequate simulation results are provided using MATLAB/SIMULINK software. Lastly, the experimental results are exposed to verify both proposed technique and the improvised circuit with a detailed comparative results.

3.2 Proposed MLI configuration synthesis

The process of designing 19-level (19L) configuration is initiated by inducing the two diodes in place of switches from the circuit which has demonstrated in the second chapter as shown in the Figure 3.1(a). Thereby control complexity and number of gate drive and switch protection setups are alleviated in the proposed circuit. Later on, an appropriate bridge voltage waveforms are described in Figure 3.1(b). Here, top waveform (V_{01}) is collected across the secondary terminals of transformer-1 and middle waveform (V_{02}) is taken from an output side of the transformer- 2. Regarding the shape of above-mentioned two voltage waveforms, the top one is a quasi-square waveform, and the middle one is a zigzag waveform. However, both waveforms possess quarter wave symmetry as well as odd symmetry, thereby computing the signal become easy and also waveforms are free from an even harmonics. In the proposed configuration, the load is connected between a dotted terminal of transformer-2 and a non-dotted terminal of transformer-1 and remaining secondary terminals of both transformers are shorted. Thus, load current flows from the dotted terminal of transformer-2 to a non-dotted terminal of transformer-1, and corresponding load voltage waveform is showed at the bottom of the Figure 3.1(b). The Figure 3.1(b) is evident that the transformers can boost the magnitude of the individual operating voltages of two bridges (H4 and H6). Thereby the peak inverse voltage (PIV)



(a)



(b)

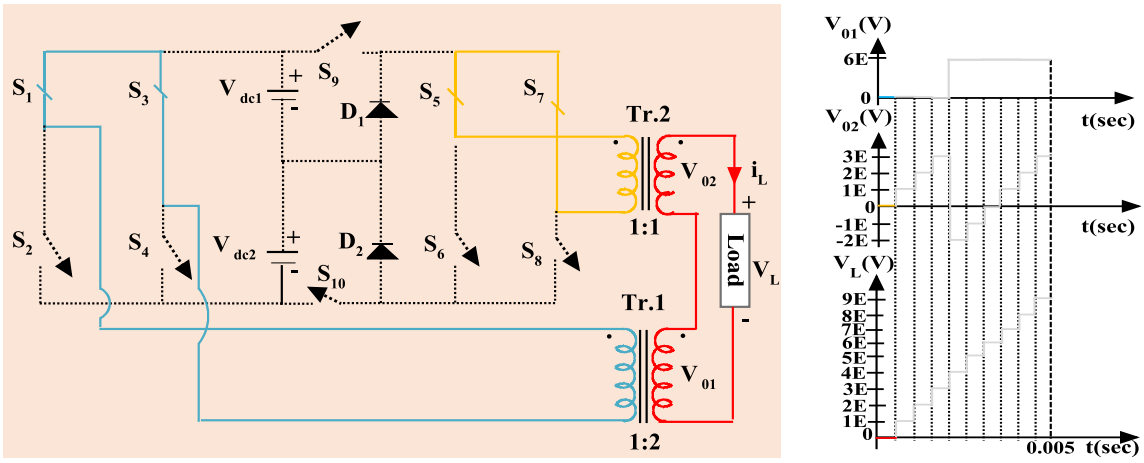
Figure 3.1: (a) Proposed 19-level inverter configuration, (b) Key waveforms of transformer-1 output voltage V_{01}, transformer-2 output voltage V_{02} and load voltage V_L of the proposed topology.

of the semiconductor switches used in H4 and H6 topologies is reduced to one-third of the load voltage.

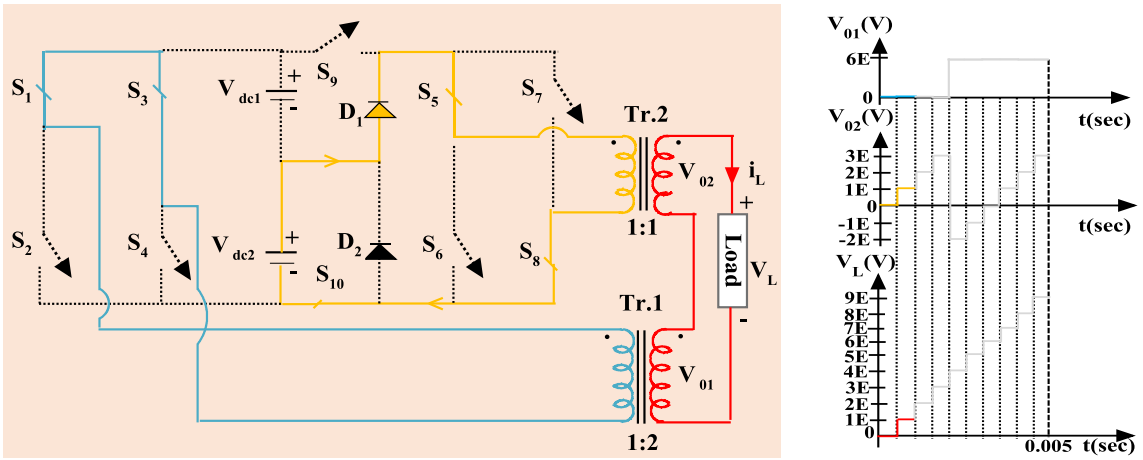
Table3.1 summarizes all the possible output voltage levels and the switching combinations (0 for OFF and 1 for ON state of a switch) that can be generated with the topology. Further, to have a comprehensive understanding of these switching states, a path for the load current, active switches and the effect of each state on bridge voltages, Figure 3.2, 3.3, 3.4 and 3.5 are included (only for a positive quarter cycle of the output voltage). For apprehending the 0^{th} level (0L), the switches S_1, S_3 of H4 and S_5, S_7 of H6 bridges are activated as shown in Figure 3.2(a). Later, the following components, diode D_1 and S_1, S_3, S_5, S_8 and S_{10} switches are handled the primary level (1L) by considering the magnitude of V_{dc2} equal to 1E and a pictorial representation is shown in Figure 3.2(b). For realising second level (2L), the DC source V_{dc1} is selected with the magnitude '2E volts'thereafter S_1, S_3, S_5, S_8 and S_9 and diode D_2 are activated as shown in Figure 3.2(c). Up to the third level (3L), H4 bridge settled at a zeroth state, and an entire topology depends on the H6 bridge which contributes frim 0L to 3L levels alone, the 3L generation is displayed in Figure 3.3(a). Similarly, Figure 3.3,3.4 and 3.5 interprets other positive pertinent levels (4L, 5L, 6L, 7L, 8L and 9L). Afterward, the negative states are accomplished by S_2,S_4, S_6 and S_8 switches in place of S_1, S_3, S_5 and S_7 sequentially. However, switches S_9 and S_{10} of H6-bridge are functioned continuously for a whole period. Regarding hardware pulse generation, six isolated controlling signals are enough to drive the presented configuration (ten switches) to attain all output voltage levels.

3.3 Fundamental sine quantised switching technique

As per switching criterion, large numbers of control techniques are presented over the years in the literature (Colak et al., 2011). Specifically, sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), random pulse width modulation (RPWM) (Trzynadlowski et al., 1994), selective harmonic elimination (SHE) (Dahidah and Agelidis, 2008), Round control (or) Nearest level methods (Kouro et al., 2007a) and so on. Admittedly, every control technique possesses benefits and limits, such as executing the SPWM technique are too complicated for high-level voltage applications especially hybrid and single DC converters, at the same time SVPWM cannot be applicable for single-phase networks and also understanding is



(a)



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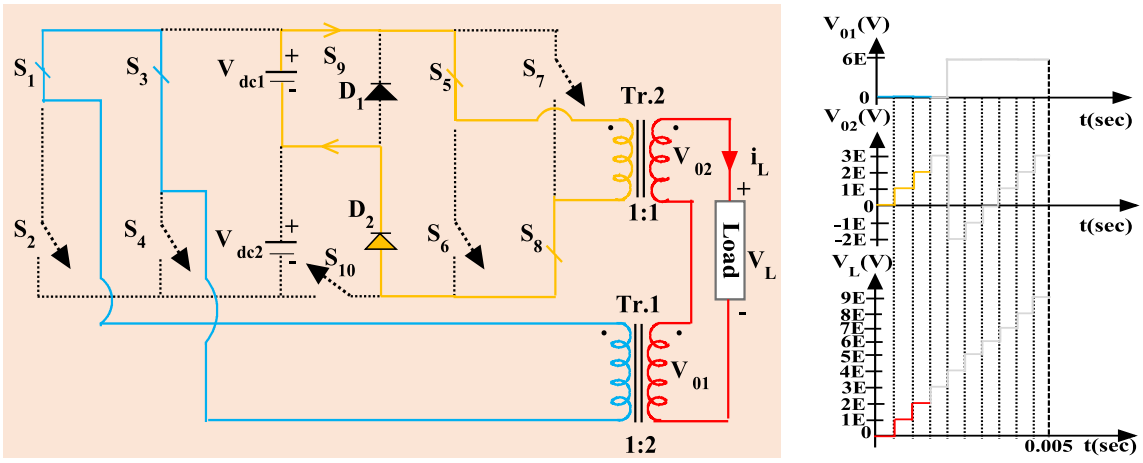
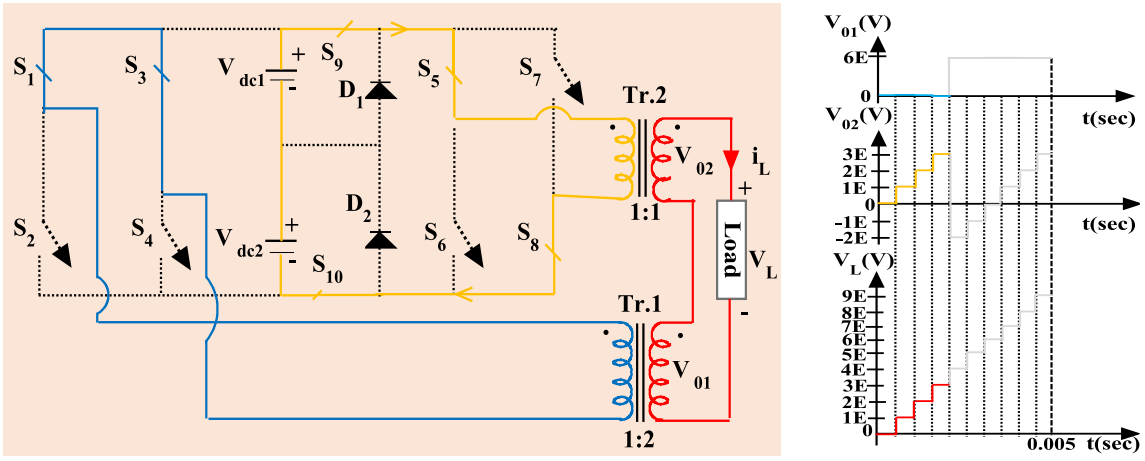
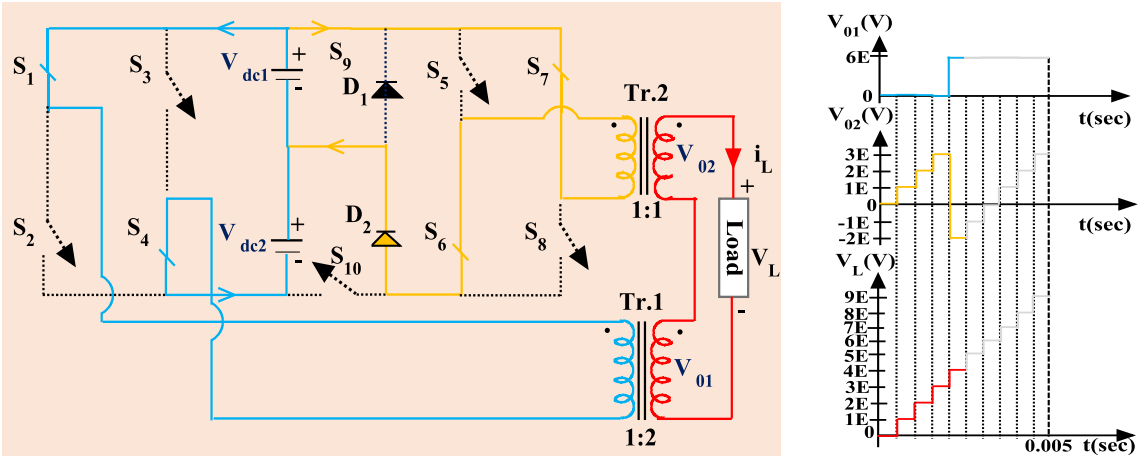


(c)

Figure 3.2: (a) Zero voltage state, (b) First voltage state: E-volts, (c) Second voltage state: 2E-volts



(a)



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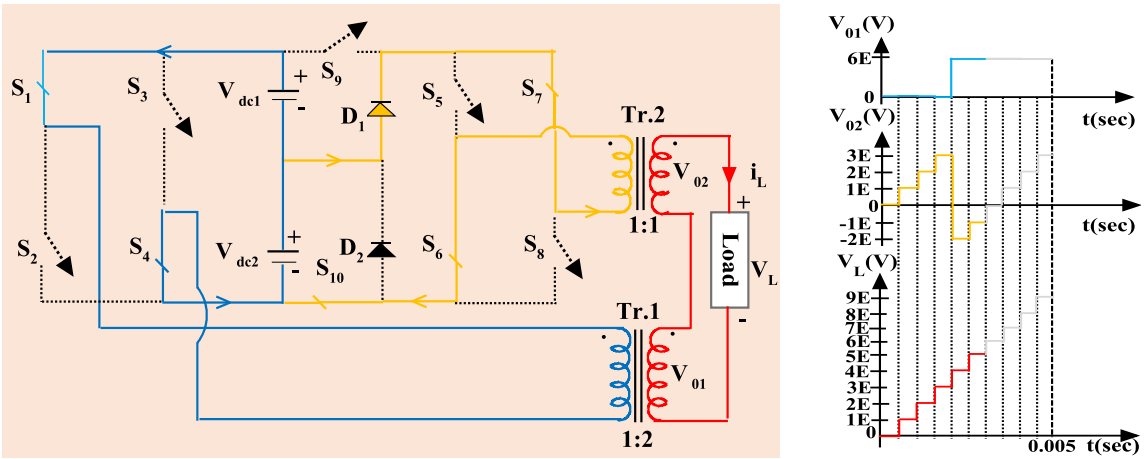
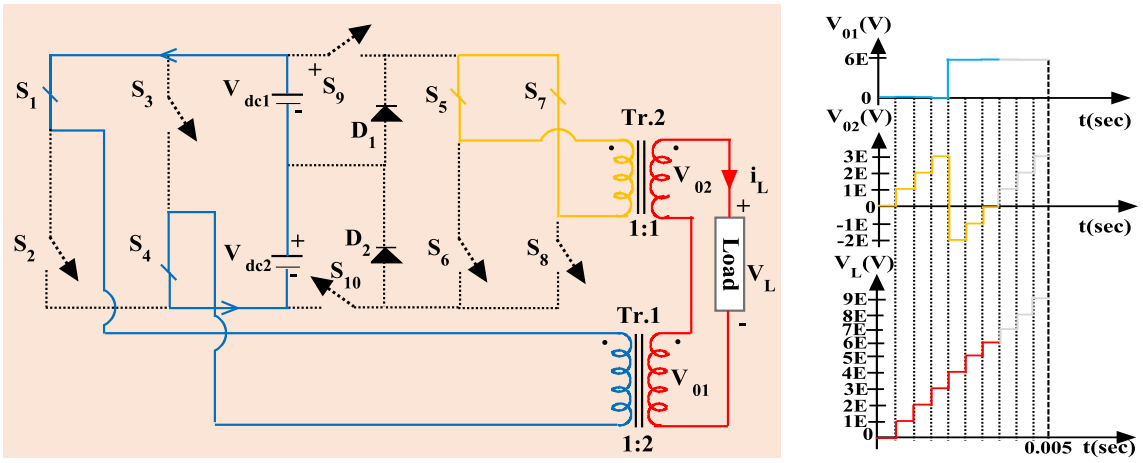
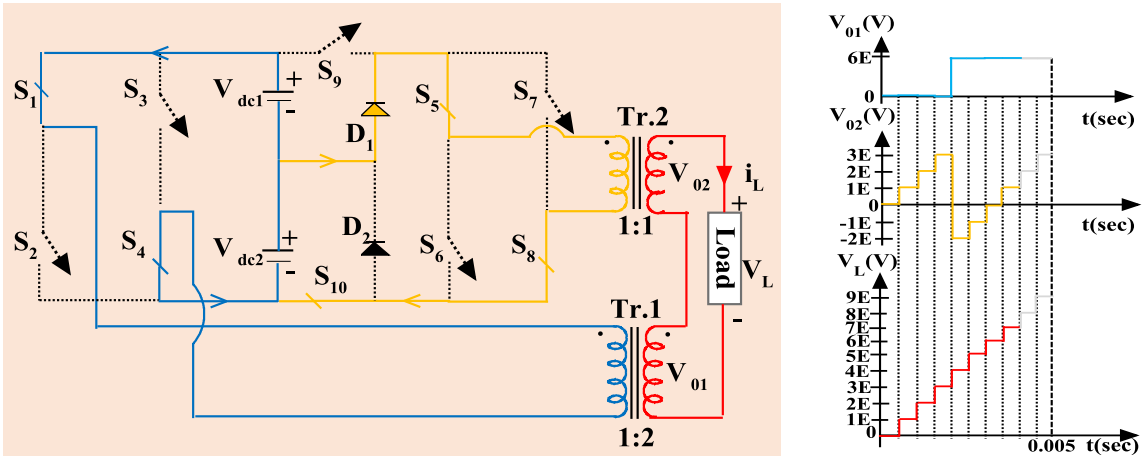


(c)

Figure 3.3: (a) Third voltage state: 3E-volts, (b) Fourth voltage state: 4E-volts, (c) Fifth voltage state: 5E-volts



(a)



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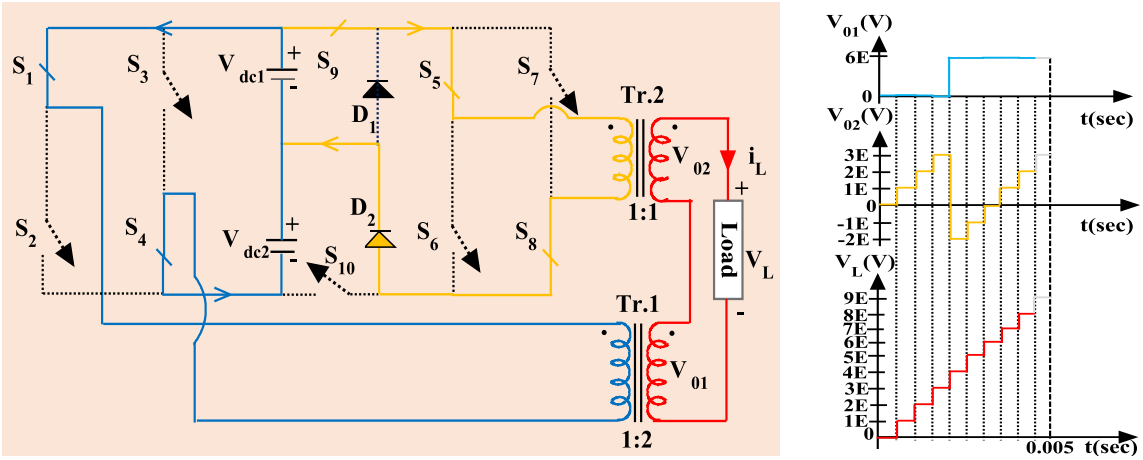


(c)

Figure 3.4: (a) Sixth voltage state: 6E-volts, (b) Seventh voltage state: 7E-volts, (c) Eighth voltage state: 8E-volts

Table 3.1: Triggering states according to load voltage waveform levels

Load voltage	Switching states of H4 -Bridge					Switching states of H6 -Bridge						
V_L	S_1	S_2	S_3	S_4	V_{01}	S_5	S_6	S_7	S_8	S_9	S_{10}	V_{02}
0	1	0	1	0	0	1	0	1	0	0	0	0
1E	1	0	1	0	0	1	0	0	1	0	1	1E
2E	1	0	1	0	0	1	0	0	1	1	0	2E
3E	1	0	1	0	0	1	0	0	1	1	1	3E
4E	1	0	0	1	6E	0	1	1	0	1	0	-2E
5E	1	0	0	1	6E	0	1	1	0	0	1	-1E
6E	1	0	0	1	6E	1	0	1	0	0	0	0
7E	1	0	0	1	6E	1	0	0	1	0	1	1E
8E	1	0	0	1	6E	1	0	0	1	1	0	2E
9E	1	0	0	1	6E	1	0	0	1	1	1	3E

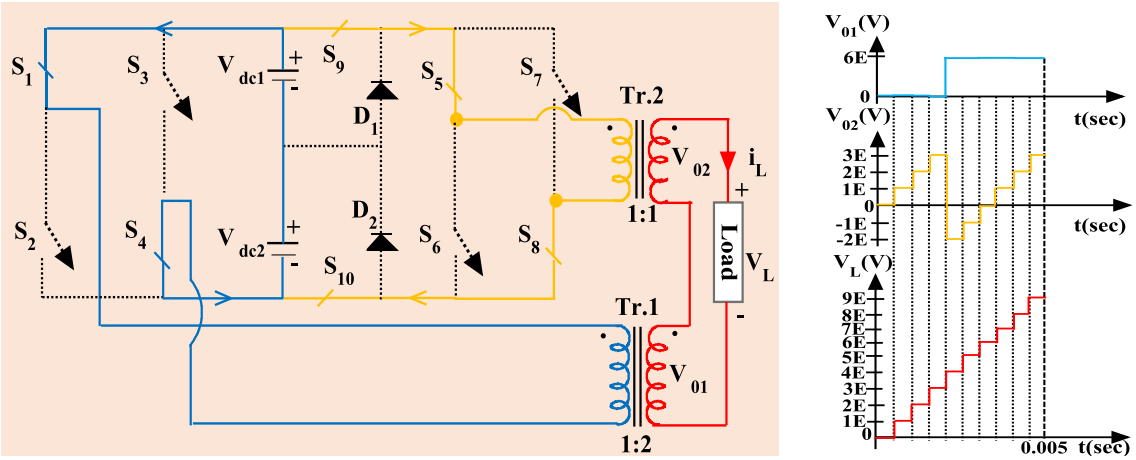
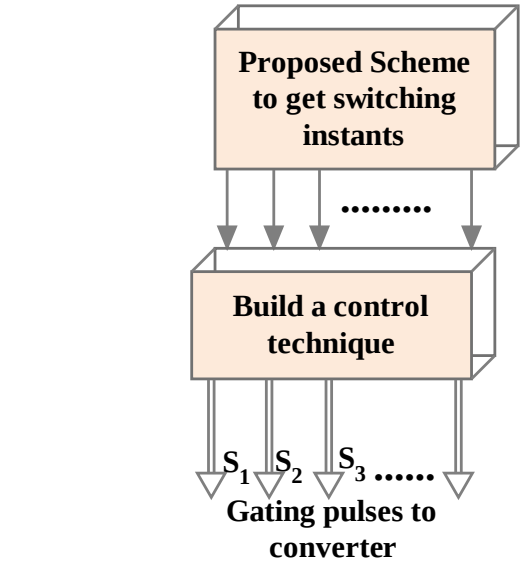


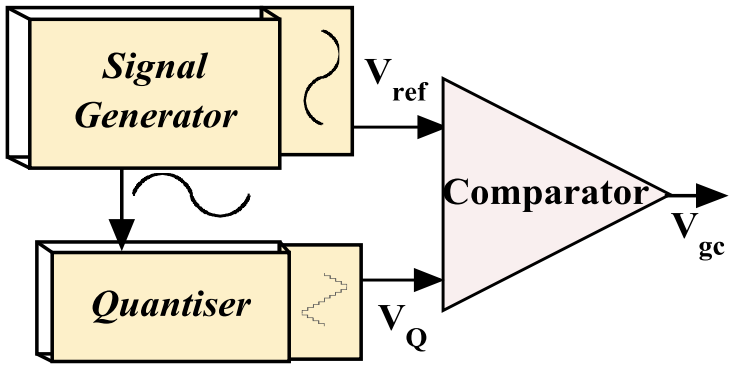
Figure 3.5: Ninth voltage state: 9E-volts

intricate beyond five levels. Thereafter, the formation of an asymmetrical carrier in RPWM is one of the challenging issues. Similarly, Newton Raphson (NR) method is observed to control the quality of the output waveform with appropriate switching angles. An optimised SHE technique with NR method is also presented in the literature (Li et al., 2000a). However, getting firing angles in SHE technique through NR method is a hard task when the output levels are raised up. Moreover, an initial guess plays a key role to solve the mathematical equations in NR method, but guessing the initial values is a pessimistic issue (Suresh et al., 2017). Finally, a Round control method which is quite easier compare to other ones. But, the lack of caring the switching angles severely affects the qualitative waveform. On this line, with a motivation to deprive the colossal harmonic-magnitudes of the load voltage waveform, a Fundamental Sine Quantised Switching Technique (FSQST) is introduced. So far, the hysteresis current control approach and/or DC voltage progression have been adopted the quantisation (Sujanarko et al., 2010, Manjrekar and Venkataramanan, 1996, Rahman et al., 1987, Taghizadeh and Hagh, 2010). But in the proposed scheme, quantiser has elected for creating the pertinent switching angles to control the magnitude and harmonic spectra of the load voltage.

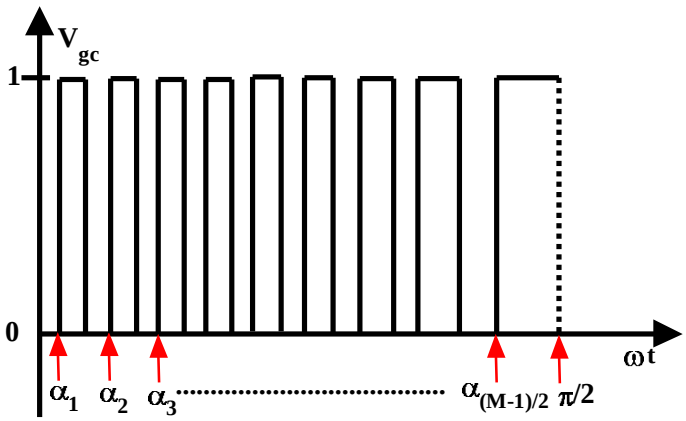
In this concept, designing the quantisation interval (Q) is an imperative step to create the pertaining levels of the output voltage. Herein, the switch controlling is mostly accomplished with the quantiser block and sine reference signal V_{ref} =V_p $\sin(2 \times \pi \times 50 \times t)$, hence it is called 'fundamental sine quantised switching technique (FSQST)'. The sophisticated algorithm of the FSQST is displayed in the Figure 3.6(a). Comprehensively the algorithm is insisting the procedure to find the appropriate switching angles using quantiser, and the suitable control function is built to attain the good harmonic profile in the output voltage waveform. Firstly, two waveforms are considered to get deserved switching instants. One is the sinusoidal waveform (V_{ref}) so-called reference waveform and the second one is a staircase waveform of the reference signal (V_Q). Secondly, by comparing the V_{ref} with V_Q the pulse train (V_{gc}) is created as shown in Figure 3.6 (b). It is evident that the frequency of the comparing signals should not be altered to accomplish the precise switching instants. Henceforth the pulse train also has the same frequency, and the switching instants of the quarter cycle of the V_{gc} are enough to build the whole control schema of the proposed configuration, and it is meticulously demonstrated in Figure 3.6(c). Analytical verification of the FSQS approach is justified in the following subsection.



(a)



(b)



(c)

Figure 3.6: (a) FSQST algorithm, (b) Simulink block representation for V_{gc} generation, (c) V_{gc} signal.

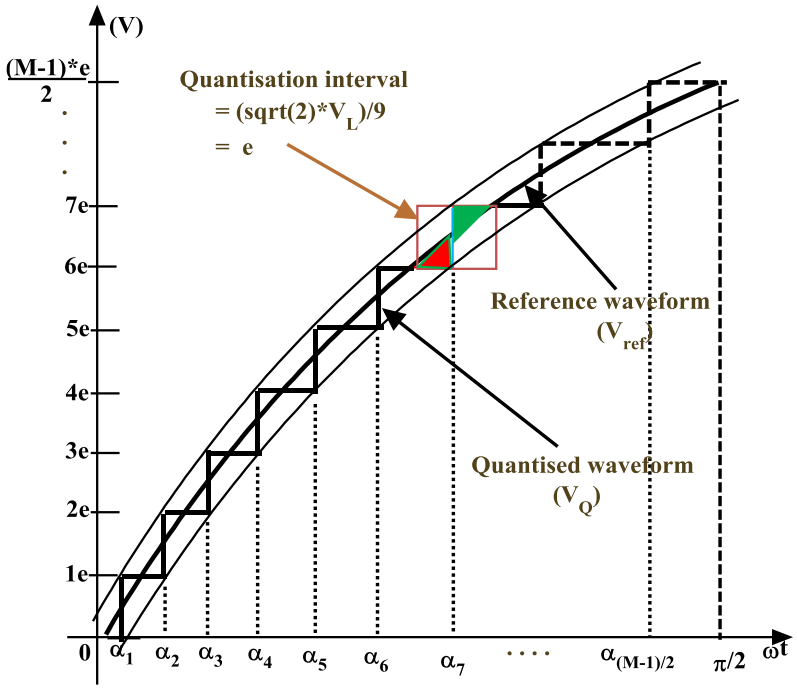


Figure 3.7: Equal area criterion system to evaluate FSQST

3.3.1 Mathematical analysis

The quantiser output waveform V_Q usually a step waveform with an equal magnitude change between two adjacent levels as shown in Figure 3.7. Here 'V_Q'is followed by its quantisation interval (Q) where the Q value depends on the number of output voltage levels and a peak of the reference signal. Moreover, the height of the reference and quantiser waveforms is the same value, if not equal area criterion will be no longer valid which leads to determining the Q magnitude to match with the output voltage levels and fundamental component of the inverter becomes very hard. The functionality of the proposed technique is clearly interpreted through the Figure 3.7. Herein, a reference signal (V_{ref}) passed over the quantiser output signal (V_Q), and the adequate hitting instants are also depicted as α_1, α_2,.....etc., and the 'Q'value is described as follows

$$Q = \frac{V_p}{0.5 \times (M-1)} \tag{3.1}$$

Where M is the number of required output levels. For simplification, let us consider, e equal to the magnitude difference between two consequent levels of quantiser output waveform; α_i is the i^{th} switching angle, where the waveform jumps from $(i-1)^{th}$ level

to i^{th} level; V_{Ln} is an inverter output voltage waveform. The number of coincides occurred between V_{ref} and V_Q signals are "((M-1)/2)+1"times per quarter cycle. Consider the angle $\omega t = \alpha_7$ where the magnitude of the reference and quantiser signals are '$V_p \sin(\alpha_7)$'and '$6.5 \times e'$sequentially. Then,

$$V_p = \frac{6.5 \times e}{\sin(\alpha_7)} \tag{3.2}$$

$$\sin(\alpha_7) = \frac{6.5 \times e}{0.5 \times (M-1) \times Q} \tag{3.3}$$

Due to the equal area distribution, e is equal to Q, therefore

$$\alpha_7 = \sin^{-1}(\frac{13}{(M-1)}) \tag{3.4}$$

Similarly

$$\alpha_8 = \sin^{-1}(\frac{15}{(M-1)}) \tag{3.5}$$

A generalised formula for i^{th} switching angle is

$$\alpha_i = \sin^{-1}(\frac{(2i-1)}{(M-1)}), \quad where \quad i = 1, 2, ...(M-1)/2. \tag{3.6}$$

Then, Load voltage is expressed in Fourier form as follows

$$V_{Ln}(\omega t) = \sum_{n=1,3,5,7,..}^{\infty} \frac{4}{n\pi}(E\cos n\alpha_1 + 2E\cos n\alpha_2 + ...(\frac{M-1}{2}) \times E\cos(n\alpha_{0.5(M-1)}) \tag{3.7}$$

The proposed scheme is also valid for three-phase inverters, in such cases quantiser interval (Q) is depends on the number of line to line voltage levels.

3.3.2 Evaluating the switching instants for the proposed 19L topology by the FSQS approach

Firstly, consider a sine reference waveform (V_{ref}) with unit magnitude and 50 Hz frequency. Secondly, the proposed converter can produce nineteen levels at most, therefore the least Q value has become 1/9 (calculated from an equation 3.1). Due to holding the Q at 1/9, the pulse train V_{gc} has nine switching instants per $(1/4)^{th}$ cycle and these nine instants are sufficient to drive an entire configuration because load voltage is possessing both the quarter wave and odd wave symmetry properties. The switching angles are extracted from the pulse train V_{gc} through the following embedded MATLAB code.

Angle extraction program:

$$
\begin{aligned}
&clc;\\
&clearall;\\
&closeall;\\
&formatshortE;\\
&load(`Vgc.mat');\\
&Vgc = Vgc';\\
&Vgc1 = Vgc(1 : floor(size(Vgc, 1)/4), :);\\
&Vgc2 = Vgc1(find(diff(Vgc1(:, 2)) == 1) + 1, 1);\\
&for \quad ii = 1 : numel(Vgc2)\\
&eval([`alpha' num2str(ii)' = Vgc2(ii). \times (18000)']);\\
&end
\end{aligned}
$$

Structurally, the presented topology requires only six distinct control signals, though the circuit built with ten switches. In another way, the existence of the complementary switches makes a more straightforward controlling embedded program for the proposed structure.

$$
\begin{aligned}
V_{L1}(\omega t) = \frac{4}{\pi}(&E\cos\alpha_1 + 2E\cos\alpha_2 + 3E\cos\alpha_3 + 4E\cos\alpha_4 + 5E\cos\alpha_5\\
&+6E\cos\alpha_6 + 7E\cos\alpha_7 + 8E\cos\alpha_8 + 9E\cos\alpha_9) \qquad (3.8)
\end{aligned}
$$

Fifth and seventh harmonic components,

$$V_{L5}(\omega t) = \frac{4}{5\pi}(E\cos 5\alpha_1 + 2E\cos 5\alpha_2 + 3E\cos 5\alpha_3 + 4E\cos 5\alpha_4 + 5E\cos 5\alpha_5 + 6E\cos 5\alpha_6 + 7E\cos 5\alpha_7 + 8E\cos 5\alpha_8 + 9E\cos 5\alpha_9) \quad (3.9)$$

$$V_{L7}(\omega t) = \frac{4}{7\pi}(E\cos 7\alpha_1 + 2E\cos 7\alpha_2 + 3E\cos 7\alpha_3 + 4E\cos 7\alpha_4 + 5E\cos 7\alpha_5 + 6E\cos 7\alpha_6 + 7E\cos 7\alpha_7 + 8E\cos 7\alpha_8 + 9E\cos 7\alpha_9) \quad (3.10)$$

The switching angles of both theoretical and simulation of the proposed topology are presented in Table 3.2 for different quantisation intervals. The results of both theoretical and simulation are much closer to each other because an error is very minimal (less than one degree). Next, the nineteen level output voltage waveform's fundamental component is derived from the equation 3.8, and the harmonics 5^{th} and 7^{th} are also exhibited in equations 3.9 and 3.10 respectively. However, the overall harmonic spectrum of the output waveform is very appreciable as per the international standards though the lower order harmonics existed with amplitudes less than 1 percent. The error between the simulation and theoretical angles for every 'Q' value is presented in Table 3.2. The difference between the analytical and simulation angles is very negligible, or no variation. Finally, the uniqueness of the FSQS technique with classical fundamental switching techniques is comprehensively presented in Table 3.3.

Table 3.2: Comparative study on simulation and theoretical switching angles

Q	Simulation	Theoretical	Error	Q	Simultaion	Theoretical	Error	Q	Simulation	Theoretical	Error
1	30.6	30	0.6	1/6	5.4	4.8	0.6	1/8	18.9	18.21	0.69
1/2	15.3	14.48	0.82		15.3	14.5	0.8		26.1	25.94	0.16
	48.6	48.6	0		25.2	24.6	0.6		35.1	34.22	0.88
1/3	9.9	9.59	0.31		36	35.7	0.3		44.1	43.43	0.67
	30.6	30	0.6		48.6	48.6	0		54.9	54.34	0.56
	56.7	56.4	0.3		66.6	66.44	0.16		70.2	69.64	0.56
1/4	7.2	7.2	0	1/7	4.5	4.1	0.4	1/9	3.6	3.18	0.42
	22.5	22.02	0.48		12.6	12.4	0.2		9.9	9.59	0.31
	38.7	38.7	0		21.6	20.9	0.7		16.2	16.13	0.07
	61.2	61.04	0.16		30.6	30	0.6		23.4	22.89	0.51
1/5	6.3	5.7	0.6		40.5	40	0.5		30.6	30	0.6
	18	17.46	0.54		52.2	51.79	0.41		37.8	37.67	0.13
	30.6	30	0.6		68.4	68.21	0.19		46.8	46.24	0.56
	45	44.43	0.57		3.6	3.58	0.02		56.7	56.44	0.26
	64.8	64.16	0.64		11.7	10.8	0.9		71.1	70.81	0.29

Table 3.3: Relative study among fundamental switching techniques

Factors	SHE technique [1,2]	Nearest level (or) Round control method [3]	Proposed method
Quality	Nullify,the specified lower order harmonics thereby improve output waveform quality	Improve the quality of output waveform without concern of specific harmonic order	Maximising the quality of output waveform by considering appropriate quantisation value.
Switching losses	Low	Low	Low
As number of levels increase	It becomes complex to implement	It is lightly hard to implement	It is easy to implement
Analytical switching instants produced by	N-R iteration method	Comparison algorithm	Quantised approach
THD profile	Good	Good	Better
limitation	Accurate initial value guessing is difficult	All modulation index values are not possible to implement	Reference waveform is always sinusoidal
Suitable for	Diode clamped MLI, Flying capacitor MLI	Multi cell converters	CHB-MLI, Hybrid MLI, Asymmetrical MLIs

1. Kouro et al. (2010)

2. Dahidah and Agelidis (2008)

3. Trzynadlowski et al. (1994)

3.4 Simulation results

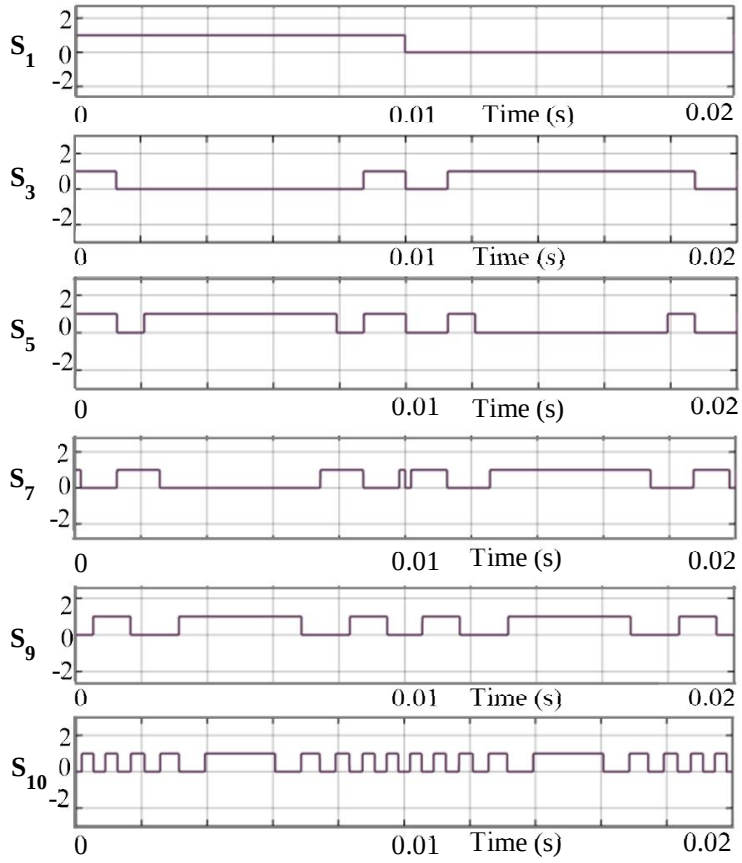


Figure 3.8: Simulation results: Triggering pulses of proposed topology

The present section deals extensively with the simulation verification of the proposed structure. The following device parameters $V_{dc1} = 72.28V$; $V_{dc2} = 36.14V$; $V_L(RMS) = 230V$; $P_{Load} = 200W$ are considered to confirm the simulation validness of the presented configuration. After that, the transformer-1 and transformer-2 power ratings are evaluated mathematically Kang et al. (2005), and the corresponding values are 200VA and 100VA sequentially. As stated in the earlier subsection, the proposed circuit can accomplish 19L output voltage waveform whenever the quantisation ratio of the suggested fundamental switching technique 'Q 'has predefined by 1/9. The simulation gating pulses of corresponding IGBT switches of the proposed topology are presented in Figure 3.8 for the quantisation value $\frac{1}{9}$. Here, gate driving signals for S_2, S_4, S_6 and S_8 IGBT switches are not depicted because, they are complementary switches of S_1, S_3,S_5 and S_7 successively.

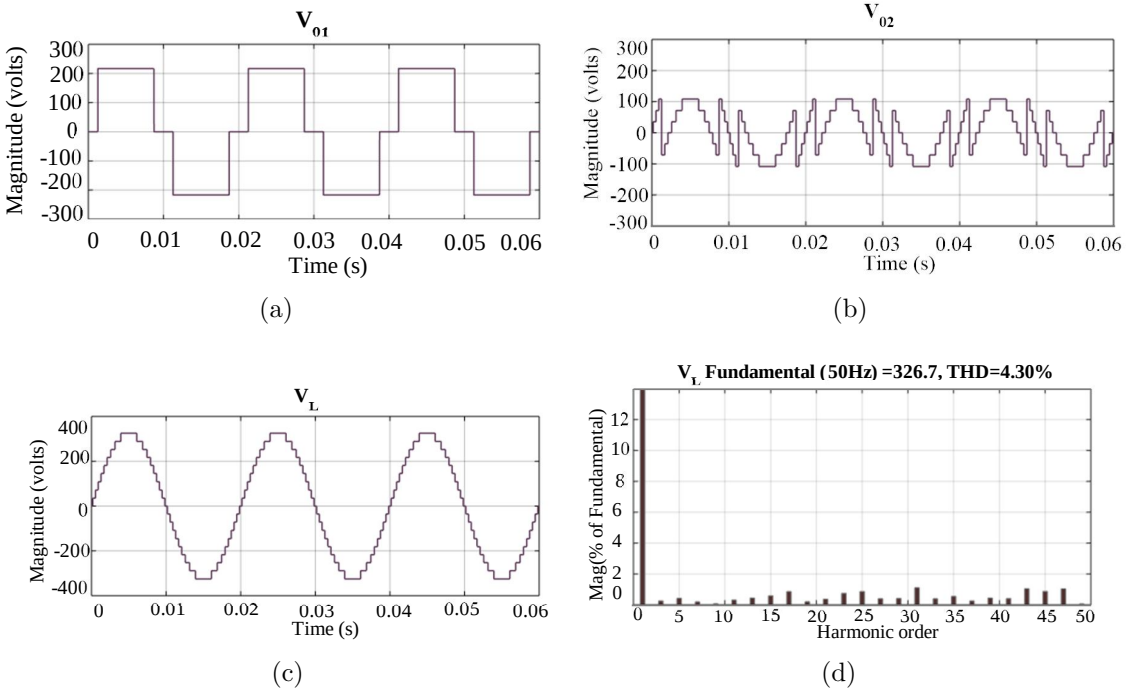


Figure 3.9: Simulation results: (a) Transformer-1 output voltage V_{01} (b) Transformer-2 output voltage V_{02}, (c) Load voltage V_L, (d) % THD of the load voltage V_L

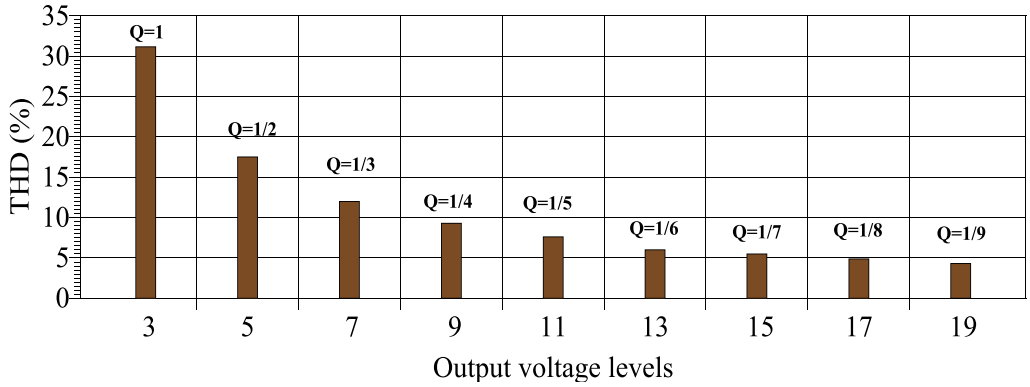


Figure 3.10: Simulation results: %THD variation chart along with quantisation interval (Q)

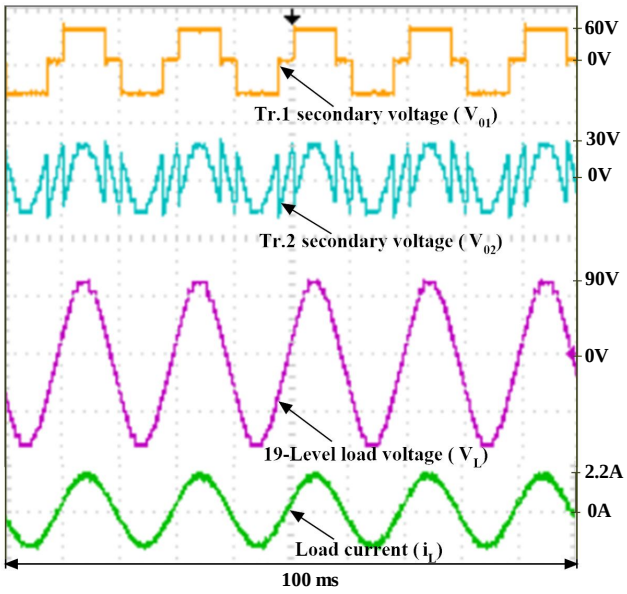
At this instant, the shape of the transformer-1 output voltage (V_{01}) is a quasi-square waveform shown in Figure 3.9 (a). In fact, transformer-1 handles twice the power rating of transformer-2. The peak value of the quasi-square waveform is 216.84 V, and the tip of seven-level uneven waveform V_{02} is 108.42V is shown in Figure 3.9 (b). Though the transformers ratings are different, the maximum blocking voltage

of semiconductor switches used in the proposed inverter is equal. Further, these two voltages V_{01}, V_{02} are connected in series to produce 19-level waveform across load V_L is displayed in Figure 3.9 (c). The new control scheme FSQST mainly effects the total harmonic distortion of the output voltage V_L. The FFT spectrum of load voltage is presented in Figure 3.9 (d) which attains 4.30% THD. Thereafter, the fundamental peak magnitude of load voltage depends on 'Q'as similar to modulation index in selective harmonic elimination technique. These variants will be explained in the further section with hardware figures. The FFT spectrum of all permissible load voltage levels 3, 5, 7, 9, 11, 13, 15, 17 and 19 for the corresponding quantisation interval are exposed in the Figure 3.10. Later, the detailed switch loss calculations are carried in Appendix-A using curve fitting approach. For a given load (200W), the total loss of the proposed MLI is 6.218W for 1 sec and the individual switch losses are shown in Table 3.4 for the same time period (1sec). Therefore the efficiency of the proposed MLI is 96.89%.Furthermore, the proposed MLI can be extended to three phase system where the number of transformers further reduced to two three-phase transformers instead of six single-phase transformers. Thereby, a manufacturing cost of the proposed MLI will be curtailed.

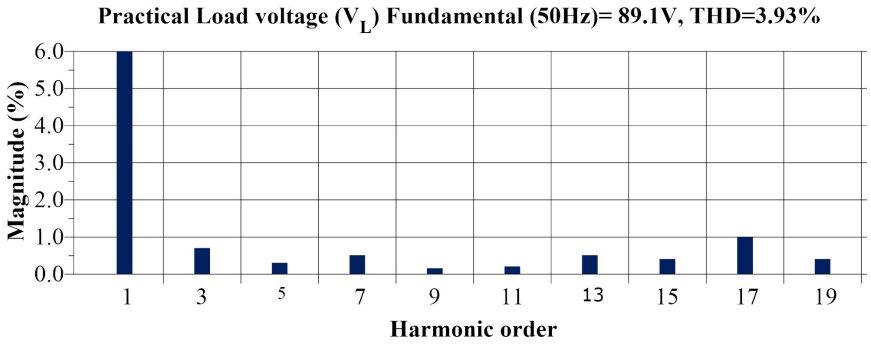
3.5 Experimental results

In hardware verifications, all desired triggering pulses of the proposed topology are accomplished with the help of OP5142 real-time simulator which is one of the fundamental building blocks in the modular OP5600 Input / Output system from Opal-RT Technologies. Appendix 2 comprehensively presented about the OP5142 real-time simulator. Truly an experimental setup is assembled with six SKM75GB123D half-bridge IGBT modules, two linear CRNGO core transformers (Tr.1: 200VA, Tr.2: 100VA), and two-channel Aplab dual DC power supply which provides two input DC sources ($V_{dc1} = 20V$ and $V_{dc2} = 10V$), moreover a suitable gate driver circuits are built by TLP 250 optocouplers. Herein, the OP5142-RT simulator merely considered as a controller running with simulation time $T_s = 50e^{-6}$ seconds, so that there is less possibility to occur dead shot between the complementary switches of proposed topology which leads to curtailing additional dead band circuits. The load parameters $R = 20\Omega$ and $L = 30mH$ are considered to evaluate the presented topology.

The experimental 19-level load voltage, load current and corresponding bridge



(a)



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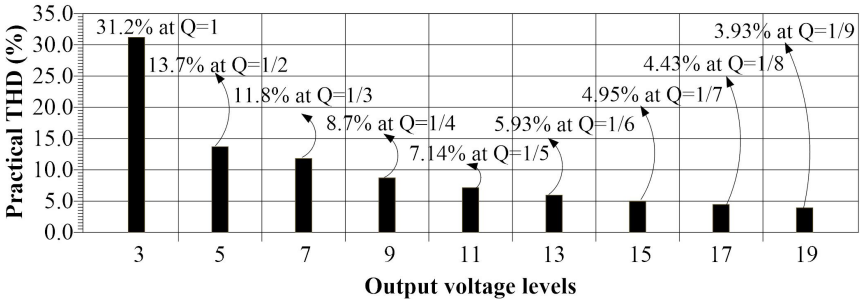

(c)

Figure 3.11: Experimental results for 19-level waveform: (a) H4-bridge corresponding transformer secondary terminal voltage (V_{01}), H6-bridge pertinent transformer secondary terminal voltage (V_{02}), the voltage across the load (V_L), and the current flowing through the load (i_L); (b) THD spectrum of the load voltage; (c) % THD variation chart for other possible load voltage levels.

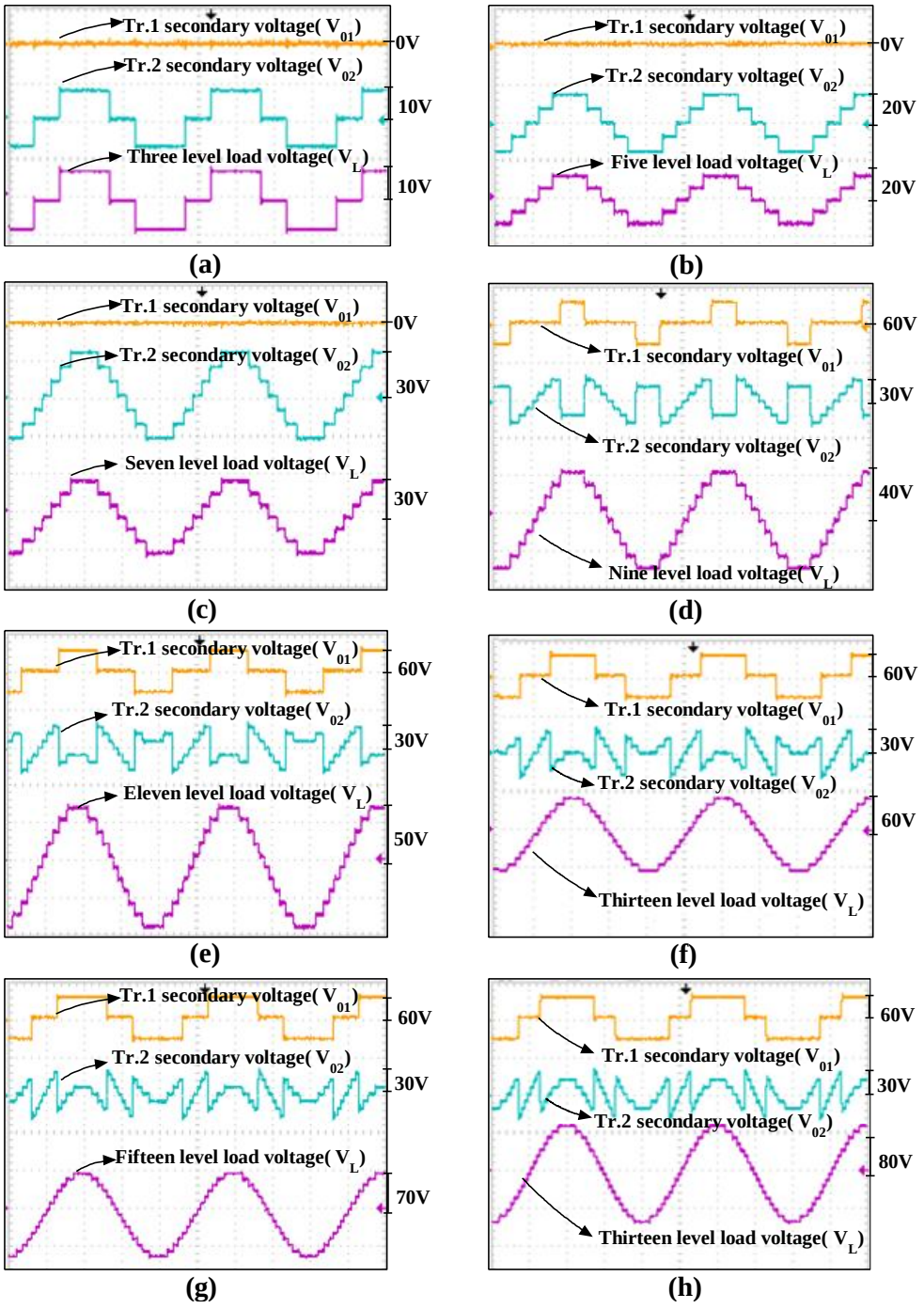

Figure 3.12: Experimental voltage waveforms across the secondary terminals of the Transformer-1 (V_{01}) and Transformer-2 (V_{02}) and the load terminals (V_L) when the quantisation interval 'Q'varies from one to one by eight fraction: (a) V_{01}, V_{02}, and V_L waveforms for $Q = 1$; (b) V_{01}, V_{02}, and V_L waveforms for $Q = 1/2$; (c) V_{01}, V_{02}, and V_L waveforms for $Q = 1/3$; (d) V_{01}, V_{02}, and V_L waveforms for $Q = 1/4$; (e) V_{01}, V_{02}, and V_L waveforms for $Q = 1/5$; (f) V_{01}, V_{02}, and V_L waveforms for $Q = 1/6$; (g) V_{01}, V_{02}, and V_L waveforms for $Q = 1/7$; (h) V_{01}, V_{02}, and V_L waveforms for $Q = 1/8$.

Table 3.4: Detailed loss analysis of the proposed MLI

Device	Insulated Gate Bipolar Transistor		Anti parallel diode		$Device_{loss}(W)$
Switch/Diode	P_{cond}(W)	P_{switch}(W)	P_{cond}(W)	P_{switch}(W)	-
S_1	0.3085	0	0.2619	$1.856e^{-6}$	0.5704
S_2	0.3064	0	0.2619	$4.136e^{-7}$	0.5684
S_3	0.2239	0.00185	0.3189	0.0005387	0.5452
S_4	0.2255	0.001852	0.3186	0.0005375	0.5465
S_5	0.3542	0.00185	0.2644	0.0002644	0.6207
S_6	0.3551	0.001839	0.2645	0.0002693	0.6217
S_7	0.4137	0.002855	0.3013	0.0006974	0.7186
S_8	0.4129	0.002873	0.3012	0	0.7170
S_9	0.03652	0.004095	0.2649	0	0.3056
S_{10}	0.207	0.006222	0.2664	0.0003849	0.4800
D_1	-	-	0.2619	0	0.2619
D_2	-	-	0.2619	0	0.2619

*Total loss = 6.218W

voltages are shown in the Figure 3.11 (a), where 60V, 30V, 90V, 2.2A are the peak magnitudes of V_{01}, V_{02}, V_L and i_L. The resistive-inductive load causes the minimum phase difference between the load voltage and current waveforms. The harmonic spectrum of the load voltage is presented in Figure 3.11 (b), wherein the load voltage has achieved 3.93% THD without any additional filter. The practical THD chart by varying number of levels in the load voltage is shown the Figure 3.11 (c). Experimentally, when the load voltage maintains minimum 15 levels, then the proposed topology can be obtained the below five percent of THD of the load voltage by adopting the FSQS technique.

Figure 3.12 describes practical results of transformer-1 and transformer-2 secondary terminal voltages and load voltage when quantisation interval (Q) changes from 1 to 1/8. Though the V_{02} waveform looks symmetric fashion, the odd and quarter wave symmetry won't loose it's shape. The transformer-1 output voltage will be the zero magnitudes till Q value cross beyond 1/3. At that time, the load should be entirely driven by the transformer-2. Afterward, the Q reaches the value 1/4 then two transformers (1&2) start to feed the load together. As Q changes, accordingly, the

power-sharing between the transformers varied. In fact, a peak value of the fundamental load component always equal to an amplitude of the highest level of the load voltage waveform. For example, in Figure 3.12(h), positive top of the load voltage is 80V, thereby, the peak of the fundamental voltage waveform also be 80V. When the switching technique applies to three-phase delta network, the harmonic profile of the load voltage improves magnificently because of inherently accumulating the two-phase voltage waveforms for giving the line to line voltage waveform. The main limitation of the FSQST is all switching angles are calculated in off-line to execute the proposed topology by the FSQS control schema.

3.5.1 Structural comparative study

Table 3.5: Structural uniqueness of the proposed configurations

	Existed MLI topologies						
	1	2	3	4	5	Chapter 2	**Proposed**
Number of levels	11	19	19	19	15	19	**19**
Number of DC-sources	1	1	1	5	3	2	**2**
Number of IGBT-switches	12	20	20	14	12	12	**10**
Gate drivers	12	20	20	14	12	12	**10**
Diodes	0	0	0	0	0	0	**2**
PIV	$1V_{dc}$	$9V_{dc}$	$1V_{dc}$	$9V_{dc}$	$7V_{dc}$	$3V_{dc}$	$3V_{dc}$
Number of transformers	3	9	9	0	0	2	**2**

1. Kang et al. (2005)
2. Banaei et al. (2012b)
3. Behara et al. (2016)
4. Babaei and Hosseini (2007)
5. Gupta and Jain (2012a)

As per the device count concern, the proposed converter has reduced two self-controlled switches than the circuit reported in chapter2. For higher levels, the device count will be further reduced. Moreover, the presented topology has a compact structure compared to conventional cascaded MLI (Hammond, 1995) where 36 individual semiconductor switches and 9 DC links need to attain the same nineteen levels. Similarly, the transformer-based configuration presented in (Banaei et al.,

2012a) which demands 20 IGBT switches and nine low-frequency transformers for achieving nineteen levels. Herein, the number of devices like transformers and IGBTs are higher than the proposed configuration and thereby, the proposed topology become an economically better circuit than the topology presented by the authors (Banaei et al., 2012a). Moreover, the topology developed in chapter 2 needs twelve controlled switches, but here, the proposed topology has implemented nineteen levels with only ten IGBT switches. The component comparison analysis with existed and popular MLI circuits is described comprehensively in Table 3.5.

3.6 Summary

In the current chapter, a 19L single phase transformer based MLI proposed with only ten semiconductor switches. Moreover, a simple fundamental switching strategy 'FSQS technique'has comprehensively conferred. After that, an experimental and simulation results have been provided to verify the performance of the FSQST for the suggested MLI. In fact, the proposed technique can be adopted in place of any fundamental switching technique (nearest level control, SHE technique, etc.) for improving the harmonic profile of the output waveform and carefully mitigating the switching loss.

Up to now, the transformer based archetypes are investigated for satisfying the specific applications (grid-connected, FACTS, etc.) where the transformers have the more vital importance. However, some of the applications should not accept the existence of the transformer in their configurations for having a variable control and compact size constraints. In this perspective, the next chapter is entirely devoted to propose a novel transformer-less MLI with the least part count.

Chapter 4

A NOVEL MULTI-CELL CMLI

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4.1 Introduction

In the last two chapters, transformer based multilevel inverters with reduced device count are discussed, and such inverters are mainly applicable for grid-connected systems and FACTs devices. The transformer in the inverter design limits the penetration into the drives applications. For addressing this issue, the current chapter proposed an architecture without any inductive elements named as a Multi-cell cascaded multilevel inverter. The chapter is systematised as follows. Section 4.1 gives the details of modes of operation and possible converter extensions. Section 4.2 briefly presents the standard control techniques (SHE and Nearest level control method), and Section 4.3 provides the simulation and power loss calculations of the proposed MLI. Finally, the Real-Time verifications are given in the Sections 4.4, and summary of the chapter is presented at the end.

4.2 Multi-cell MLI topology synthesis

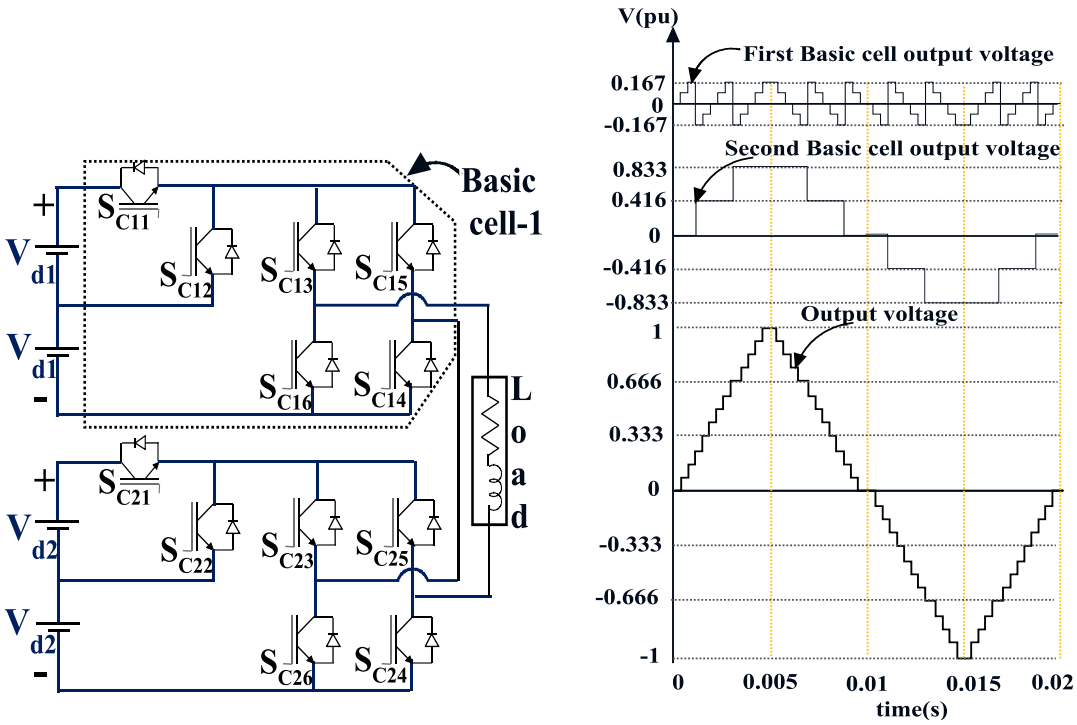
The proposed multi-cell CMLI consists of 'N_{DC}'number of equal DC voltage sources which are handled to synthesize a multilevel output voltage employing power electronic switches. The value of the DC sources used in the different cells is supposed to be different so that more output voltage levels can be generated using fewer devices. Moreover, the number of DC supplies in every sub-cell can be altered according to the requirement of the structure. However, the present configuration shown in Figure 4.1 considered a uniform number of DC supplies in every sub-cell, i.e., n=2, and each sub-cell can generate '2n+1'levels. The Figure 4.1 shows the multi-cell configuration along with key voltage waveforms of each primary cell. Structurally, a basic cell having uniformly two DC sources and four polarity reversing switches and two level creating switches. Though the switches S_{C13} to S_{C16} are withstanding a voltage equal to the total DC voltage of the cell, the entire input supply of the configuration is shared between the cells for promoting to higher voltage applications.

Let us consider, the i^{th} cell has K_i equal input sources and the value of the first-cell source to be followed as

$$V_{d,1} = V_{dc} \tag{4.1}$$

Then the value of the DC voltage source of the i^{th} cell can be determined as follows

$$V_{d,i} = (2k_1 + 1).(2k_2 + 1)...(2k_{i-1} + 1).V_{dc} = V_{dc} \prod_{m=1}^{i-1} (2k_m + 1) \tag{4.2}$$



(a) (b)

Figure 4.1: (a) The proposed 25-level multi-cell CMLI, (b) Key voltage waveforms in per units.

By considering the equation4.2 for the input DC supplies of every sub-cell, the total output levels of the MLI are determined as follows:

$$N_L = (2k_1 + 1).(2k_2 + 1)...(2k_q + 1) = \prod_{m=1}^{q} (2k_m + 1) \tag{4.3}$$

The positive peak magnitude of the load voltage can be written as

$$V_{L,max} = \frac{[(2k_1 + 1).(2k_2 + 1)...(2k_q + 1)] - 1}{2}.V_{dc} = \frac{[\prod_{m=1}^{q}(2k_m + 1)] - 1}{2}.V_{dc} \tag{4.4}$$

The required switches of the each sub-cell is calculated by the following equation.

$$N_{IGBT,i} = 2(k_i + 1) \tag{4.5}$$

Therefore the total switch count of the proposed MLI is function of the DC supplies as follows

$$N_{IGBT} = \sum_{n=1}^{q} 2(k_m + 1) \tag{4.6}$$

Key voltage waveforms of the sub-cells and load voltage waveform are presented in Figure 4.1(b). The proposed MLI has accomplished twenty-five levels for considering the DC magnitude ratio 1:5. The waveform of the first sub-cell seems to be a zigzag fashion so that it is treated as an asymmetrical bridge, and the second sub-cell waveform describes the symmetry (quarter wave and odd wave symmetry), thereby it is named as a symmetrical bridge. The triggering states of both bridges are displayed for half of fundamental cycle in Table 4.1.

4.2.1 Modes of operation of the proposed MLI

The individual switching states of the proposed multilevel inverter are exposed in Figure 4.2.

- 1E Level: The Asymmetrical bridge alone provides the 1E level across the load by conducting its single DC supply through the switches S_{C12}, S_{T11}, and S_{T12}. Herein the DC source of an Symmetrical bridge is bypassed form the load by activating the switches S_{T24} and S_{T22}.

- 2E Level: This level is accomplished when the Asymmetrical bridge switches S_{C11}, S_{T11}, and S_{T12} are turn ON. At the same time, the Symmetrical bridge should be continuing the bypassed state.

- 3E Level: Two outputs of the individual bridges are cascaded to attain the 3E level, where the Symmetrical bridge generates +5E and an Asymmetrical bridge functioned to produce -2E magnitude.

- 4E Level: Similar to 3E level, 4E level also accomplished by cascading two individual bridge outputs, where the Symmetrical bridge generates +5E and an

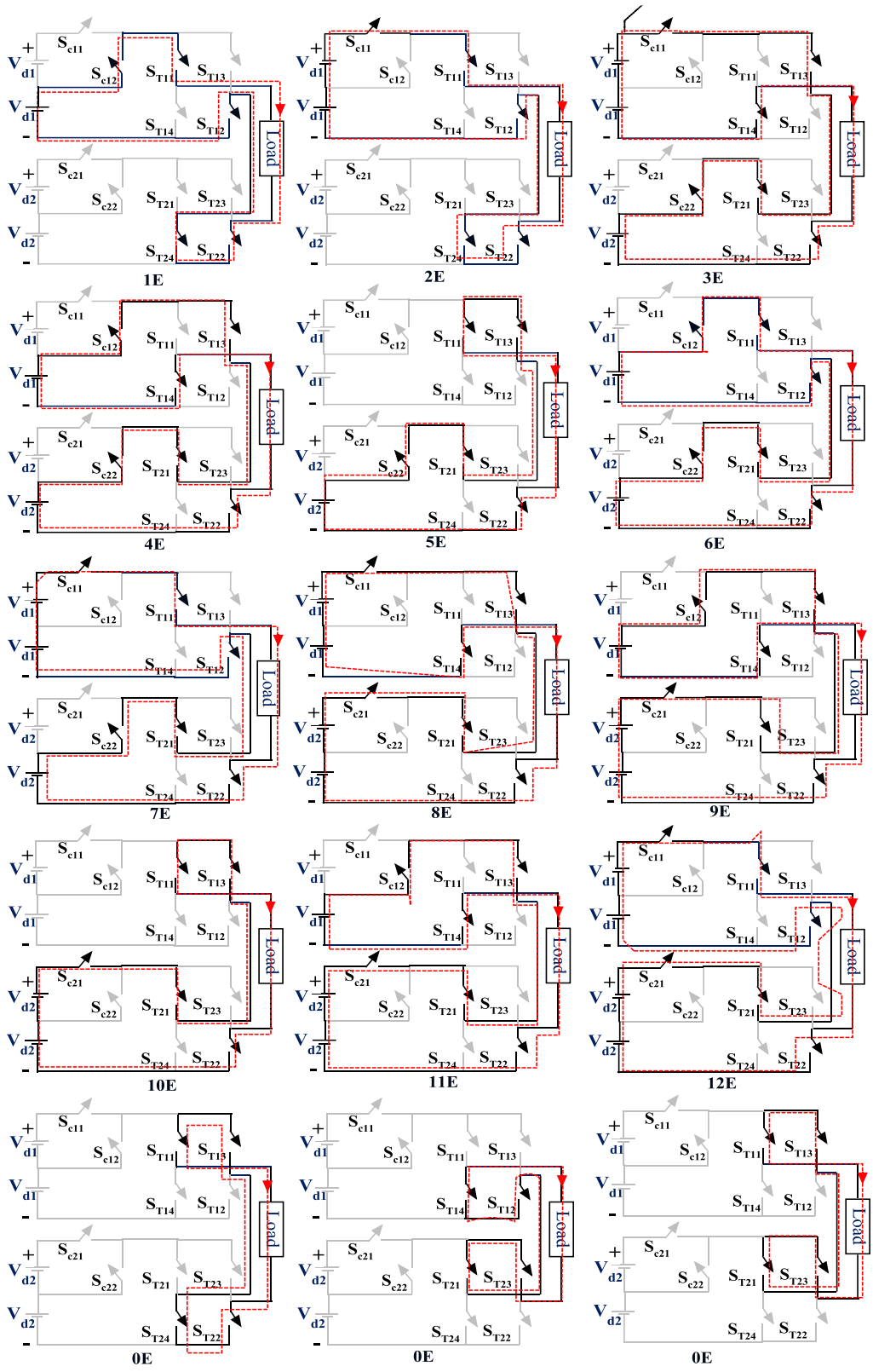


Figure 4.2: Operating modes of the proposed configuration per half cycle

Asymmetrical bridge functioned to produce -1E magnitude.

- 5E Level: The Symmetrical bridge alone provides the 5E level across the load by conducting its single DC supply through the switches S_{C22}, S_{T21}, and S_{T22}. Herein the DC source of an Asymmetrical bridge is bypassed form the load by connecting the switches S_{T11} and S_{T13}.
- 6E Level: The switches S_{C12}, S_{T11}, and S_{T12} of Asymmetrical bridge and the switches S_{C22}, S_{T21}, and S_{T22} of Symmetrical bridge are conducted to attain the 6E level.
- 7E Level: In place of S_{C12}, the switch S_{C11} will conduct to achieve this level from the prior state 6E.
- 8E Level: The 8E level is functioned across the load when the Symmetrical bridge jumps from 5E to 10E and Asymmetrical bridge reverse the +2E polarity to -2E.
- 9E Level: In place of S_{C11}, the switch S_{C12} will conduct to achieve this level from the prior state 8E.
- 10E Level: The Symmetrical bridge alone provides the 10E level across the load through the switches S_{C21}, S_{T21}, and S_{T22}. Herein the DC source of an Asymmetrical bridge is bypassed form the load.
- 11E Level: The switches S_{C12}, S_{T11}, and S_{T12} of Asymmetrical bridge and the switches S_{C11}, S_{T21}, and S_{T22} of Symmetrical bridge are conducted to attain the 11E level.
- 12E Level: In place of S_{C12}, the switch S_{C11} will conduct to achieve this level from the prior state 11E.
- 0E Level: The zeroth level can achieved in multiple ways, in Figure 4.2 three ways are shown, in fact in four ways it can be accomplished. The ultimate goal of the zeroth state is nothing but bypassing the input supplies of the bridges from the load.

The switching table and individual states are representing only about the positive states of the proposed multi-cell MLI. To attain the negative states merely energize the complementary switches of all polarity generators of the sub-cells.

Table 4.1: Triggering states of the semiconductor switches of the proposed MLI

Output Voltage	Asymmetric Bridge							Symmetric Bridge						
V_{out}	S_{C11}	S_{C12}	S_{C13}	S_{C14}	S_{C15}	S_{C16}	V_{C1}	S_{C21}	S_{C22}	S_{C23}	S_{C24}	S_{C25}	S_{C26}	V_{C2}
0	0	0	1	0	1	0	**0**	0	0	1	0	1	0	**0**
E	0	0	1	1	0	0	**E**	0	0	1	0	1	0	**0**
2E	1	0	1	1	0	0	**2E**	0	0	1	0	1	0	**0**
3E	1	0	0	0	1	1	**-2E**	0	0	1	1	0	0	**5E**
4E	0	1	0	0	1	1	**-1E**	0	0	1	1	0	0	**5E**
5E	0	0	1	0	1	0	**0**	0	0	1	1	0	0	**5E**
6E	0	0	1	1	0	0	**1E**	0	0	1	1	0	0	**5E**
7E	1	0	1	1	0	0	**2E**	0	0	1	1	0	0	**5E**
8E	1	0	0	0	1	1	**-2E**	1	0	1	1	0	0	**10E**
9E	1	0	0	0	1	1	**-1E**	1	0	1	1	0	0	**10E**
10E	0	0	1	0	1	0	**0**	1	0	1	1	0	0	**10E**
11E	0	0	1	1	0	0	**1E**	1	0	1	1	0	0	**10E**
12E	1	0	1	1	0	0	**2E**	1	0	1	1	0	0	**10E**

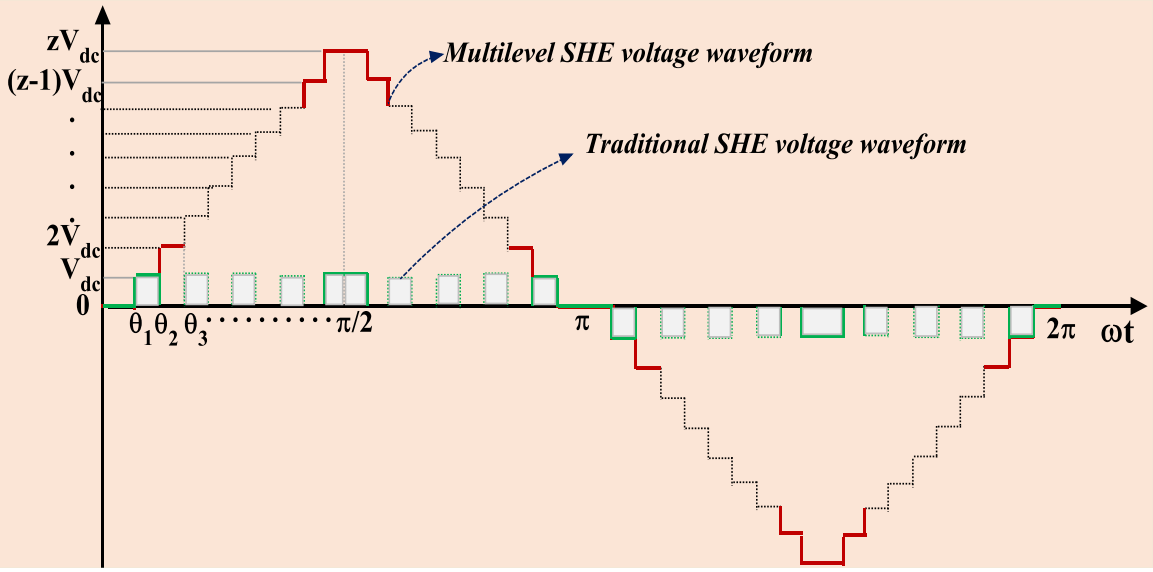


Figure 4.3: SHE voltage waveform for multilevel and traditional inverters

4.3 Standard fundamental modulation techniques

Chapter 3 partially describes the standard low-frequency control algorithms such as selective harmonic elimination (SHE) and nearest level control algorithms. Therefore in the present chapter, the detailed functioning of the general control algorithms are comprehensively provided. In fact, very high-power converters are typically switched with fundamental switching frequency algorithms, below 1 kHz. If the carrier-based pulse width modulation schemes want to implement, then the switching frequency should be very low which causes the existence of the low-order harmonics in the load voltage which creates performance issues. To address this aspect, the SHE is developed where the switching angles are predefined. Furthermore, the angles are precalculated via Fourier system of equations to confirm the elimination of the unwanted lower order harmonics(Holtz, 1994).

4.3.1 SHE control scheme

The magnitude of all unwanted harmonic components of the predefined switched waveform is made equal to the zero while the fundamental component is kept equal to the desired reference amplitude. After that, the set of equations is determined off-line using numerical methods like NewtonRaphson method to get a solution for

the desired switching angles. The concept was extensively accepted for the three-level inverter, and later, it is extended for multilevel configurations (Li et al., 2000b). The SHE switching schema for MLI circuits generates 'z'number of controlling angles per quarter cycle to eliminate the 'z-1'unwanted harmonics. The remaining switching angles control the first harmonic component magnitude for reference tracking. The Figure4.3 reveals prior defined voltage waveform with a set of switching angles. The multilevel staircase waveform satisfies the odd wave symmetry, thereby only odd harmonics are observed in the output waveform. The derivation of the Fourier coefficients are presented as follows:

The Fourier coefficients, average value of waveform a_0 and even harmonic contents a_n are become zero and the odd order harmonic pertinent coefficient b_n only existed in multilevel output waveform shown in Figure4.3. The generalised formula of the coefficient b_n is given below.

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} V(\omega t)sin(n\omega t)d(\omega t) \tag{4.7}$$

Now the equation 4.7 is computed for the multilevel waveform as follows,

$$\begin{aligned}
b_n &= \frac{4}{\pi}[\int_{\theta_1}^{\theta_2} V_{dc}sin(n\theta)d\theta + \int_{\theta_2}^{\theta_3} 2V_{dc}sin(n\theta)d\theta + ... + \int_{\theta_z}^{\frac{\pi}{2}} zV_{dc}sin(n\theta)d\theta] \\
&= \frac{4}{n\pi}[-V_{dc}cos(n\theta)|_{\theta_1}^{\theta_2} - 2V_{dc}cos(n\theta)|_{\theta_2}^{\theta_3} - .... - V_{dc}cos(n\theta)|_{\theta_z}^{\frac{\pi}{2}}] \\
&= \frac{4}{n\pi}[-V_{dc}cos(n\theta_2) + V_{dc}cos(n\theta_1) - 2V_{dc}cos(n\theta_3) + 2V_{dc}cos(n\theta_2) - ... \\
&\quad + zV_{dc}cos(n\theta_z)] \\
&= \frac{4}{n\pi}[V_{dc}cos(n\theta_1) + V_{dc}cos(n\theta_2) + ... + V_{dc}cos(n\theta_z)] \\
&= \frac{4V_{dc}}{n\pi}[cos(n\theta_1) + cos(n\theta_2) + ... + cos(n\theta_z)]
\end{aligned}$$

$Therefore$

$$b_n = \frac{4V_{dc}}{n\pi}\sum_{j=1}^{z} cos(n\theta_j) \tag{4.8}$$

where b_n is the amplitude of n^{th} harmonic, it is worth noting that $\alpha_1 < \alpha_2 < \alpha_3$

$< ....\alpha_z < \frac{\pi}{2}$. Finally the Fourier series form of staircase waveform is expressed as follows

$$V(\omega t) = \sum_{n=1}^{\infty}[b_n]sin(n\omega t) = \sum_{n=1}^{\infty}[\frac{4V_{dc}}{n\pi}\sum_{j=1}^{z}cos(n\theta_j)]sin(n\omega t) \tag{4.9}$$

4.3.1.1 Newton Raphson (NR) approach to determine switching angles

The NR method is adopted for identifying the 'z'switching angles of $2z+1$ level output waveform from the equation4.8, The fundamental amplitude of the voltage waveform is given below

$$b_1 = \frac{4V_{dc}}{\pi}[cos(\theta_1) + cos(\theta_2 + cos(\theta_3)) + ..cos(\theta_z)] \tag{4.10}$$

similarly, odd order harmonic amplitudes are assumed to be zero and presented as follows

$$0 = \frac{4V_{dc}}{3\pi}[cos(3\theta_1) + cos(3\theta_2) + cos(3\theta_3) + ..cos(3\theta_z)] \tag{4.11}$$

$$0 = \frac{4V_{dc}}{5\pi}[cos(5\theta_1) + cos(5\theta_2) + cos(5\theta_3) + ..cos(5\theta_z)] \tag{4.12}$$

$$0 = \frac{4V_{dc}}{7\pi}[cos(7\theta_1) + cos(7\theta_2) + cos(7\theta_3) + ..cos(7\theta_z)] \tag{4.13}$$

$$\vdots$$

$$\vdots$$

$$0 = \frac{4V_{dc}}{n\pi}[cos(n\theta_1) + cos(n\theta_2) + cos(n\theta_3) + ..cos(n\theta_z)] \tag{4.14}$$

Note that, SHE technique does not have any control over the not eliminated harmonic contents, it can only control the amplitudes of fundamental and eliminated harmonic components. The term modulation index (m) is considered to control the amplitude of the fundamental components and is given as

$$m = \frac{b_1}{zV_{dc}} \tag{4.15}$$

Substitute above equation4.15 in the equation4.10, and then rewrite the equations from 4.10 to 4.14 as follows,

$$cos(\theta_1) + cos(\theta_2) + cos(\theta_3) + ..cos(\theta_z) = \frac{zm\pi}{4} \tag{4.16}$$

$$cos(3\theta_1) + cos(3\theta_2) + cos(3\theta_3) + ..cos(3\theta_z) = 0 \tag{4.17}$$

$$cos(5\theta_1) + cos(5\theta_2) + cos(5\theta_3) + ..cos(5\theta_z) = 0 \tag{4.18}$$

$$cos(7\theta_1) + cos(7\theta_2) + cos(7\theta_3) + ..cos(7\theta_z) = 0 \tag{4.19}$$

$$\vdots$$

$$\vdots$$

$$cos(n\theta_1) + cos(n\theta_2) + cos(n\theta_3) + ..cos(n\theta_z) = 0 \tag{4.20}$$

The aforementioned non-linear equations are to be solved to find the appropriate switching angles of the multilevel waveform by the following steps.

Consider the switching angles in matrix form,

$$\theta^j = [\theta_1^j, \theta_2^j, \theta_3^j, ...\theta_z^j]^T \tag{4.21}$$

Similarly the non-linear system matrix (F) is derived

$$F^j = \begin{bmatrix} cos(\theta_1^j) + cos(\theta_2^j) + ... + cos(\theta_z^j) \\ cos(3\theta_1^j) + cos(3\theta_2^j) + ... + cos(3\theta_z^j) \\ cos(5\theta_1^j) + cos(5\theta_2^j) + ... + cos(5\theta_z^j) \\ cos(7\theta_1^j) + cos(7\theta_2^j) + ... + cos(7\theta_z^j) \\ . \\ . \\ . \\ cos(n\theta_1^j) + cos(n\theta_2^j) + ... + cos(n\theta_z^j) \end{bmatrix} \tag{4.22}$$

and

$$\left[\frac{\partial F}{\partial \theta}\right]^j = \begin{bmatrix} -sin(\theta_1^j) - sin(\theta_2^j) - ..... - sin(\theta_z^j) \\ -3sin(3\theta_1^j) - 3sin(3\theta_2^j) - ..... - 3sin(3\theta_z^j) \\ -5sin(5\theta_1^j) - 5sin(5\theta_2^j) - ..... - 5sin(5\theta_z^j) \\ -7sin(7\theta_1^j) - 7sin(7\theta_2^j) - ..... - 7sin(7\theta_z^j) \\ . \\ . \\ . \\ -nsin(n\theta_1^j) - nsin(n\theta_2^j) - ..... - nsin(n\theta_z^j) \end{bmatrix} \tag{4.23}$$

Thereafter harmonic amplitude matrix (A) is

$$A = \begin{bmatrix} \frac{zm\pi}{4} & 0 & 0 & . & . & . & 0 \end{bmatrix}^T \tag{4.24}$$

Then, equations 4.16 to 4.20 can be rewritten in the given matrix format:

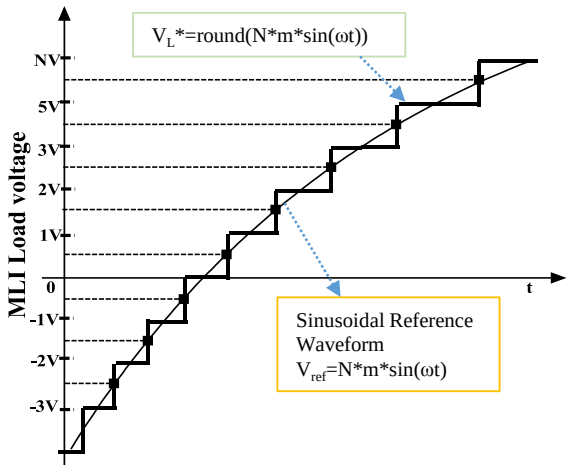
$$F(\theta) = A \tag{4.25}$$

The matrices 4.21 to 4.25 are implemented in the computer program to get the suitable switching angles for corresponding modulation indexes. It is noted that the numerical methods like NR method are performed for various modulation indexes, leading to necessary calculations that are impracticable to work in real time with contemporary microprocessors and thus are executed off-line. Though the solutions are saved in lookup tables, interpolation is used for those unsolved modulation indexes. This makes SHE-based switching algorithms not appropriate for applications requiring high dynamic performance.

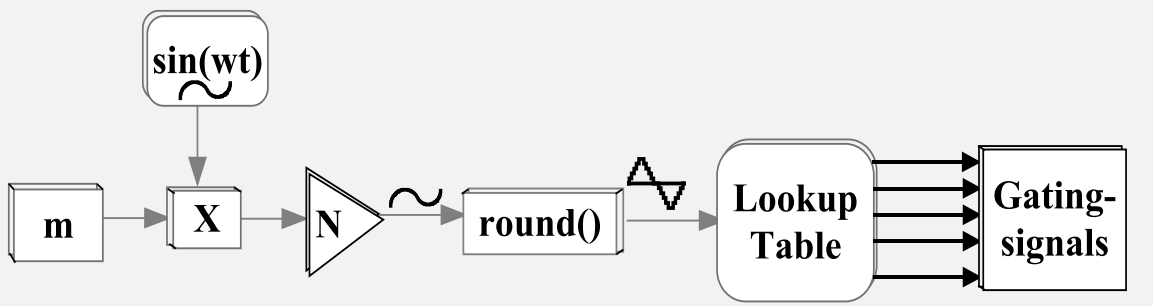
4.3.2 Round control (or) Nearest level control method

It is the most straightforward control approach introduced to reduce the practical difficulties of the asymmetrical CHB converter where the low power rating cells or bridges operate in regenerative mode though the load is not active (Pérez et al., 2007). Moreover, all three phases are controlled individually with appropriate 120^0 phase shifted reference signals to perform switching operation in the three-phase systems. This method mostly employed for high voltage applications where the number of lev-

els is large enough to improve the output voltage. Now, the semiconductor switches



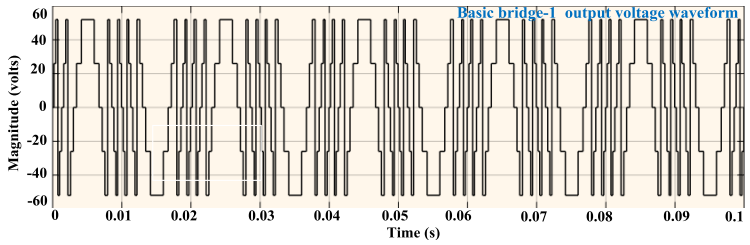
(a)



(b)

Figure 4.4: (a) Nearest voltage level selection, (b) Nearest level control algorithm.

of the converter are triggered with the suitable gating-signals which are created by the Nearest level control (NLC) method. The Figure 4.4 describes the selection of the closest voltage level and an operating principle of the NLC technique pictorially. Firstly, consider the fundamental sinusoidal function with unit magnitude and multiplied with modulation index (m_a). Afterward, allows the resultant signal through the total number of positive levels of the inverter (N). Then apply the round function to get the required levels. The purpose of the round function is that produces only one commutation between two voltage steps which leads the system to reduce the switching losses effectively. Though the technique is easy to implement, still lower order harmonics are presented. Because, it is not an actual modulation technique to eliminate the specific harmonics like SHE approach. Therefore the NLC is not suited for less than 15-levels attaining high-voltage converters.



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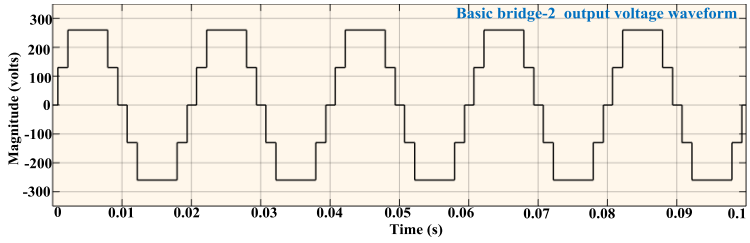

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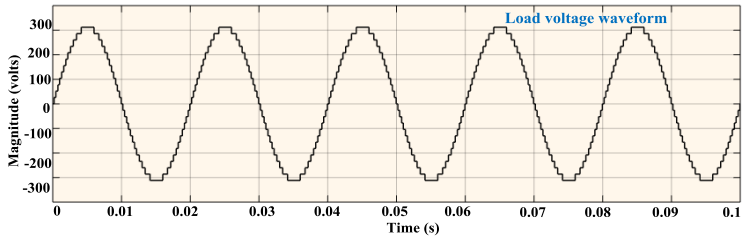

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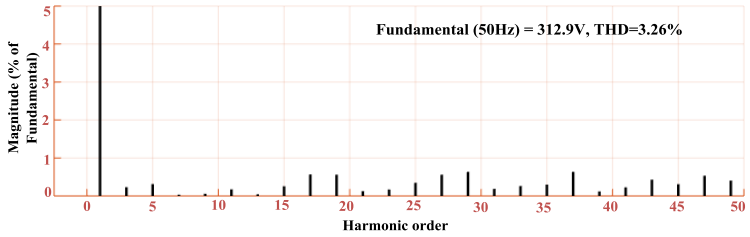
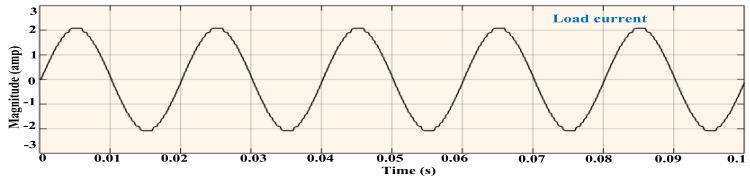


(d)



(e)

Figure 4.5: Simulation results: (a) Output voltage of asymmetric bridge, (b) Symmetric bridge voltage waveform, (c) Load voltage waveform, (d) FFT spectrum of the load voltage, and (e) Load current.

Table 4.2: System attributes considered for simulation and experiments

Parameter	Specifications
Switching devices	IGBTCM100DU12H,600V,100A, MITSUBISH IGBT MODULES
DC source (V_{d1})	26V
DC source (V_{d2})	130V
Load voltage ($V_L(rms)$)	25Level, 220V
Load frequency	50Hz
Load inductance (L)	20mH
Load resistance (R)	150Ω
DSP	eZdspTMF28335

4.4 Results and Discussion

4.4.1 Simulation results

The system parameters considered for the simulation and experimental studies are tabulated in Table4.2. The required simulation load voltage waveform is originated with the aid of MATLAB/Simulink software. Herein the staircase switching strategy is adapted to control the 25-level proposed MLI. This approach is well described in previous subsection so-called nearest level or round control technique. This adopting method has a key feature which attains the minimum error concerning the reference voltage. The operating load is taken a series R-L with magnitudes 150Ω and 20mH. The simulation results are exposed in Figure 4.5. Therein the output voltage waveforms of the asymmetrical and symmetrical bridges are presented in Figure4.5(a) and (b). By adding two bridge output waveforms across the load, the 25-level output waveform is accomplished across the load as shown in Figure4.5(c). Finally, the FFT spectrum of the load voltage and load current waveform are presented in Figure4.5(d) and (e). Though the lower order harmonics have existed in the harmonic profile of the load voltage waveform, the overall %THD is considerably very low, i.e., 3.26%. Moreover, the load inductance inherently smoothens the current waveform. For a given R-L load, the load consumes 325.16W, and an individual switch losses (conduction and switch losses) are calculated using curve fitting approach and described in Table 4.3. Therefore the efficiency of the proposed topology is 97.4% which is due to low switching frequency for each switch.

Table 4.3: Detailed loss analysis of the proposed MLI

Device	Insulated Gate Bipolar Transistor(IGBT)		Anti parallel diode		$Device_{total-loss}(W)$
Switch	P_{cond}(W)	P_{switch}(W)	P_{cond}(W)	P_{switch}(W)	-
S_{C11}	0.3097	0.009973	0.3536	0.002641	0.676
S_{C12}	0.7460	0.01412	0.4143	0	1.1740
S_{C13}	0.2613	0.006535	0.4160	0.002772	0.6867
S_{C14}	0.4075	0.007099	0.3589	0.002466	0.7760
S_{C15}	0.2613	0.006535	0.4160	0.002561	0.6865
S_{C16}	0.4075	0.007099	0.3589	0.002255	0.7757
S_{C21}	0.4851	0.003859	0.2619	0	0.7509
S_{C22}	0.9764	0	0.4651	0.00184	1.443
S_{C23}	0.05019	0	0.2790	0.0003052	0.3295
S_{C24}	0.07183	0	0.2619	0	0.3337
S_{C25}	0.05019	0	0.2790	0.0003052	0.3295
S_{C26}	0.07183	0.000552	0.2619	0	0.3343

*Total loss = 8.296W

4.4.2 Experimental results

To validate the simulation results, the hardware setup is built with the components described in the Table4.2. Further, the gating pulses are generated by the DSP based module programming. In fact, the Code composer studio is used to program the DSP in MATLAB and Simulink software. To extract the experimental switching signals from the PC, Firstly, confirm the MATLAB program for creating the pertinent triggering pulses and then directly dumped the program into the DSP platform through the USB JTAG controller. For hardware verification, the same R-L load is considered to get rid of the bewilderment between simulation and experimental results. An output waveforms are shown in Figure4.6. Herein, Figure4.6 (a) is the asymmetrical bridge output voltage waveform which has slight notches. Similarly Figure4.6 (b) describes the second basic cell output voltage waveform with five-levels. After that, the load voltage waveform has accomplished 25-levels by cascading the prior two bridge outputs as shown in Figure4.6 (c), and finally, the load current waveform is depicted in Figure4.6 (d) which is smoother than load voltage waveform because of the inductive property of the load. Furthermore, the % THD chart of the load volt-

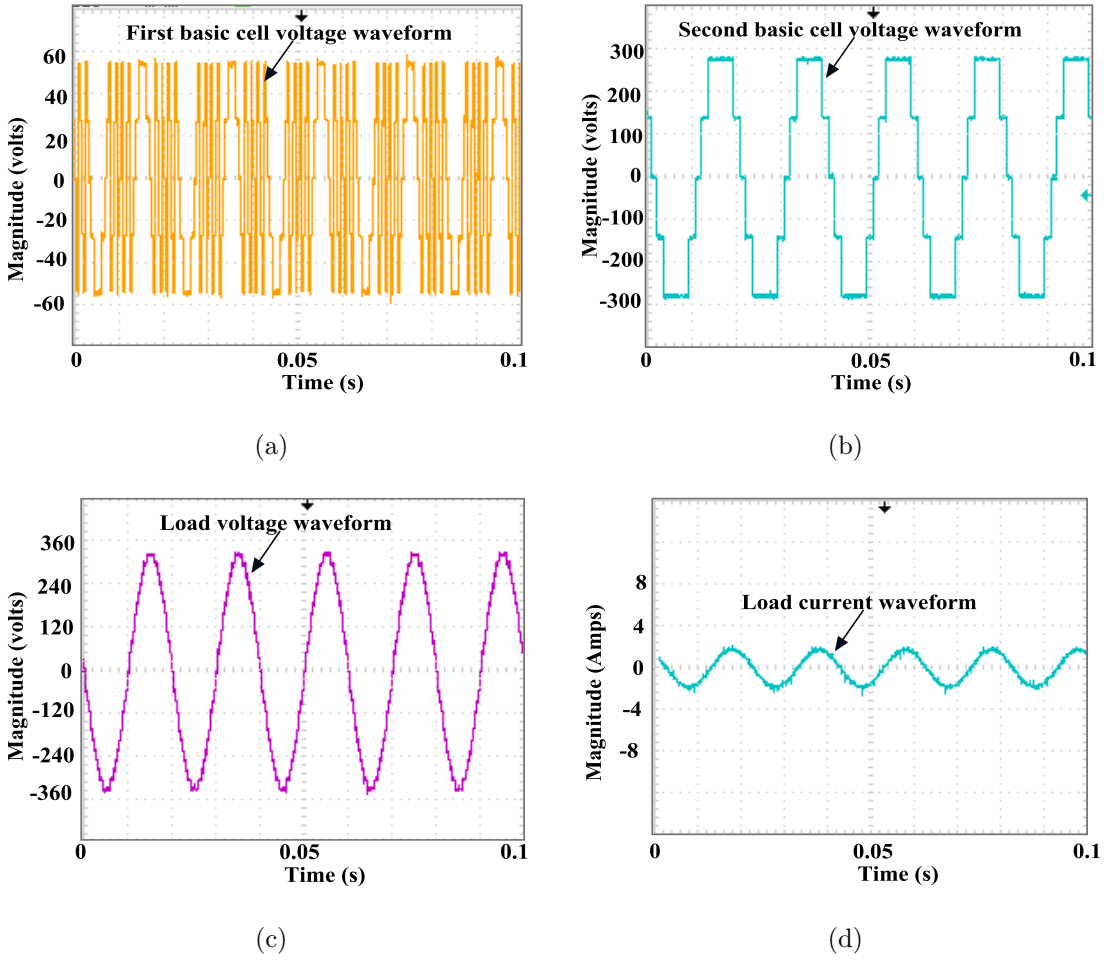


Figure 4.6: Experimental results: (a) Asymmetrical bridge output voltage waveform V_{C1}, (b) Symmetrical bridge output voltage waveform V_{C2}, (c) Load voltage waveform V_L, (d) load current waveform i_L.

age waveform is shown in Figure4.7. Though all odd order harmonics have existed at very low magnitudes (less than one percent), the overall THD is attained 3.00% which is very appreciable magnitude. If the SHE technique is implemented instead of the nearest level control technique, then the specific lower order harmonics become nullified. However, it is tough to adopt the SHE for higher levels.

4.4.3 Comparative study

To confirm the advantages and limitations of the proposed archetype, the standard and recent popular configurations are compared with proposed topology. The Table

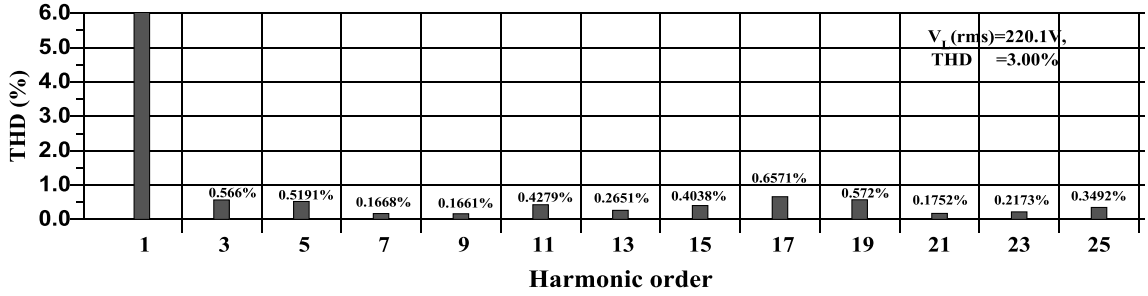


Figure 4.7: %THD variation chart of the proposed 25-level output voltage waveform

Table 4.4: Component comparison of the proposed topology with former configurations

	Devices			
Former configurations	Switch	Clamping diode	balancing capacitors	DC-bus
[1]	48	870	NA	24
[2]	48	NA	435	24
[3]	48	NA	NA	12
[4]	26	NA	NA	08
[5]	14	NA	NA	04
[6]	36	NA	NA	16
[7]	16	NA	NA	04
[Proposed]	12	NA	NA	04

1. Nabae et al. (1981)
2. Meynard and Foch (1992)
3. Hammond (1995)
4. Babaei (2011)
5. Lai and Shyu (2002)
6. Babaei and Hosseini (2009)
7. Dixon et al. (2007)

4.4 contributes in detailed component comparison of the proposed topology regarding switches, clamping diodes, balancing capacitors and DC buses. Usually, to accomplish the 25-level phase voltage waveform from CHB-MLI, DC-MLI and FC-MLI need at least 48-IGBT switches. Besides, hybrid and asymmetric CC-MLIs for both symmetric and asymmetric output voltages demands 26 and 14 switches sequentially. Furthermore, additional diodes and capacitors are not required like DC and FC-MLIs. Another vital issue is input DC-supplies count; the proposed converter runs with only 4-DC supplies whereas standard versions FC, NPC, and CHB-MLIs work with 24, 24, and 12 isolated DC-sources respectively. A part from this, a high number of DC-supplies are needed for asymmetrical and hybrid topologies. Thereby, it can be concluded that the presented configuration uses the least device count for the same levels of the load voltage waveform.

4.5 Summary

This chapter contributed a CMLI with sub-cells with a reduced number of switches. An in-depth investigation is carried out on traditional and recent hybrid and symmetric topologies from current literature to emphasise the merits of the presented configuration. Symmetric topologies can only generate the limited number of levels in the output voltage. On the counter side, these symmetrical versions can operate asymmetrically with different DC supplies. Nevertheless, these can provide a qualitative waveforms (voltage and current). Later on, single DC source based structures are also described, but the capacitor balancing is a highly complicated issue. Thereby, the novel topology is proposed with lesser device count and capable to produce a qualitative waveform. Additionally, the configuration is used the nearest level control approach to trigger the semiconductor switching devices. The experimental results are quite impressive regarding harmonic content in FFT spectrum. Thus, the proposed MLI shows promising attributes than traditional configurations.

Chapter 5

CONCLUSION AND FUTURE SCOPE

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5.1 Conclusion

In the present thesis Three Unique Hybrid MLI topologies and Two New Control techniques are proposed. In this regard with and without transformer based hybrid MLIs are designed. In transformer based architectures two simple bridges are utilised. Further this design is optimised with only 10 switches. To control proposed MLIs two new switching schemes are introduced. However the detail conclusions are drawn in chapter wise as follows:

In Chapter 1, a review of MLIs including the classic, symmetric, asymmetric, single DC, emerging and hybrid topologies has been verified. As an outcome, it was learned that despite many solutions capable of generating more number of voltage levels, an opportunity for developing an alternative way of achieving the same endures are observed. Thus, apart from the existed MLIs, two configurations are gained significant popularity. Firstly, the transformer based MLIs for constant frequency applications such as grid connected, stand alone, and FACTs devices. Secondly, transformerless MLIs for variable frequnecy applications like motor drives, cranes, tranction, and etc.

In Chapter 2, a novel hybrid multilevel inverter which employed low-frequency transformers for boosting output voltage levels and provides isolation between the load and supply are presented for high power applications. The performance of the proposed MLI is investigated with a new carrier-based LS-SPWM technique. The proposed topology is designed and verified for 19-level PWM output waveform with only two bridges. Moreover, the proposed switching technique plays a significant role to improve the FFT spectrum of the output waveform with a low switching frequency. All these features recommends the proposed configuration towards active filters, var compensators, and grid-connected applications.

In Chapter 3, a 19level single phase MLI is proposed with only ten semiconductor switches. Further, a novel fundamental switching strategy 'FSQS technique'has been introduced for the proposed topology. . After that, an experimental and simulation results have been provided to verify the performance of the FSQST for the proposed MLI. In fact, the proposed technique can be adopted in place of any fundamental switching technique (nearest level control, SHE technique, etc.) for improving the harmonic profile of the output waveform and for mitigating the switching loss.

Chapter 4 proposed a multicell MLI without transformers. An in-depth investigation is carried out on recent hybrid and symmetric topologies from current literature to

emphasise the merits of the proposed configuration. Symmetric topologies can only generate the limited number of levels in the output voltage. On the counter side, these symmetrical versions could operate asymmetrically with different DC supplies in-order to enhance the quality of output voltage. Additionally, the configuration is realised with the nearest level control approach to trigger the semiconductor switching devices. The experimental results are quite impressive concerning THD of the resultant voltage waveform. Thus, the proposed MLI would be suitable to variable frequency applications.

5.2 Future scope

Based on the research carried out in this thesis, the recommendations for future research are as follows:

- To integrate the proposed LS-SPWM method for additional improvement in output voltage quality.
- To investigate the application of the presented FSQS technique to other MLIs thereby, resulting in many other interesting topologies.
- To investigate and employ a single DC supply for both cascaded transformer MLIs leading to a reduced cost.
- To further investigate and develop the proposed configurations by substituting a multi winding and high frequency link transformers to make compact structure and a reduced cost.
- Performance and cost comparison of the developed topologies by considering for the suitable applications.

Appendix A

GENERALISED CURVE FITTING ANALYSIS OF THE POWER IGBT

As mentioned in chapter 2, the conduction loss equations from 2.6 to 2.9, and switching loss factors $K_{IGBT}(i_c)$ and $K_D(i_f)$ are derived from the curve fitting approach which calculates total losses of the semiconductor switch with slight effort. Moreover, it has high accuracy and can be planted directly in any circuit simulator. This loss calculations are based on switch data-sheet values and/or experimental measurements, the MLIs delivered in chapter 2 and 3 are built with the SKM75GB123D-IGBT as shown in FigureA.1. Therefore the SKM75GB123D data-sheet information is considered for further explanations.

A.0.1 Conduction losses

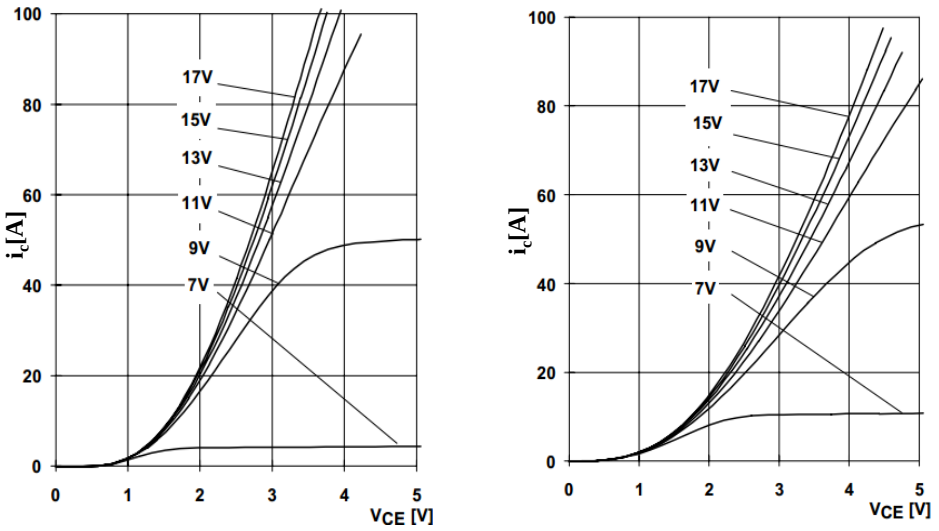
Conventionally, the conduction losses are calculated by placing the V_{dr} representing forward voltage drop and a resistor R_S representing leakage current dependency in series with an ideal switch. Though this approach can be modeled merely in the simulator, the diodes and ideal switches are overloaded with additional parameters. Moreover, the circuit simulator should accommodate controllable resistors to build the temperature dependent characteristics into this model. Thus, we followed an actual procedure presented in (Drofenik and Kolar, 2005).

(a) (b)

Figure A.1: SKM75GB123D IGBT power module under investigation

A.0.1.1 Calculation of the power IGBT-conduction loss (P_{igbt})

The considered IGBT data-sheet (SKM75GB123D) provides characteristic curves between the collector-emitter voltage (V_{CE}) and collector-current (i_C) of the IGBT at different gate-emitter V_{GE} values. Moreover, the datasheet provided V_{CE}- i_C curves for minimum and maximum temperatures [$T_{min} = 25^0$ and $T_{max} = 125^0$] as shown in FigureA.2 individually to describe the temperature dependency.



(a) (b)

Figure A.2: V_{CE} verses i_C characteristic curves of the SKM75GB123D-IGBT switch: (a) At the minimum temperature 25^0, (b) At max temperature 125^0.

Table A.1: V_{CE}- i_C curve data points for $V_{GE} = 15V$ at $T_{min} = 25^0$

V_{CE}(V)	i_C(A)	$P_{igbt,25^0} = (V_{CE} \times i_C)$
0	0	0
1	1.4286	1.4286
1.5	8.5714	12.8571
2	21.4286	42.8572
2.5	40	100
3	62.1429	186.4287
3.5	82.8571	289.999

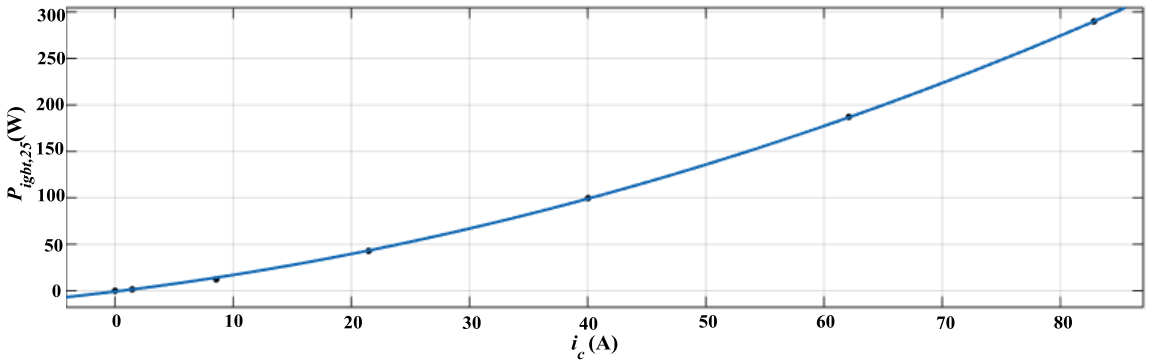


Figure A.3: Curve fitting waveform for IGBT conduction loss at 25^0 with respect to the collector current i_C.

In fact, the experimental working gate-emitter potential voltage V_{GE} is equal to the 15V. Thus, only one V_{CE}- i_C curve data is extracted from FigureA.2(a) and is mentioned in TableA.1. After that, multiply the V_{CE} with i_C to attain the power at each extracted points. The key motivation behind this process is to calculate the power loss in terms of the collector current i_C. To accomplish this approach, i_C versus $P_{igbt,25^0}$ waveform is constructed by using MATLAB curve fitting application. Herein, first, we should provide X and Y-axises data (X-data representing i_C and Y-data representing $P_{igbt,25^0}$) and then the adjust the polynomial order till the error comes minimum value. The presented data has arrived a minimum error at second order polynomial equation. Thereby the waveform shown in FigureA.3 is finalized, and it has possessed the power loss equation A.1.

$$P_{igbt,25^0} = 0.02365 i_C^2 + 1.551 i_C - 0.8995 \tag{A.1}$$

Table A.2: V_{CE}- i_C curve data points for $V_{GE} = 15V$ at $T_{max} = 125^0$

V_{CE}(V)	i_C(A)	$P_{igbt,125^0} = (V_{CE} \times i_C)$
0	0	0
1	2.1429	2.1429
1.5	5.7143	8.5714
2	14.2857	28.5714
2.5	25.7149	64.2873
3	40	120
3.5	55.7143	195.0001
4	72.8571	291.4284
4.5	91.4286	411.4287

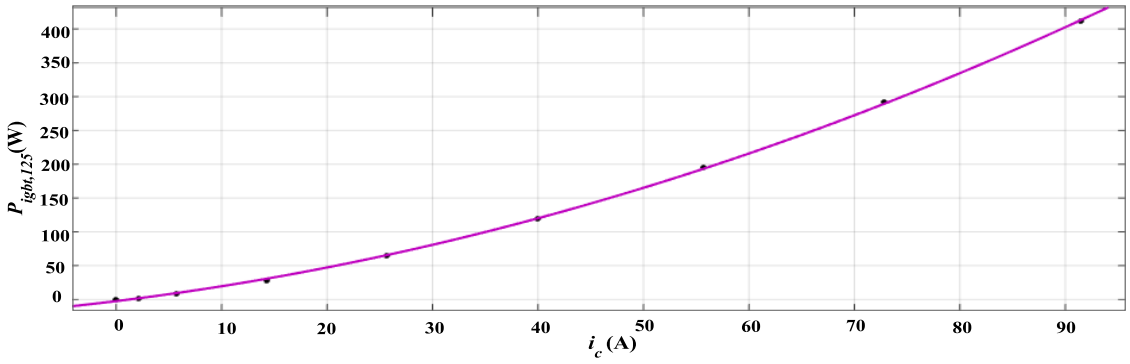


Figure A.4: Curve fitting waveform for IGBT conduction loss at 125^0 with respect to the collector current i_C.

In the similar way, the corresponding waveform of the power loss equation A.2 at 125^0C temperature is drawn as per the TableA.2 and it has shown in FigureA.4.

$$P_{igbt,125^0} = 0.02876i_C^2 + 1.914i_C - 2.452 \tag{A.2}$$

To specify the temperature dependency in the conduction loss equation, the coefficients should represent the running temperature (T). The generalised temperature dependent- second order conduction loss equation has arrived at equationA.3.

$$P_{igbt}(i_C, T) = (a_0 + a_1T)i_C^2 + (b_0 + b_1T)i_C + (c_0 + c_1T) \tag{A.3}$$

These loss pertinent coefficients are derived from the coefficients of the equations A.1

and A.2. The coefficient matrix is

$$\begin{bmatrix} P_{igbt,25^0,a} & P_{igbt,25^0,b} & P_{igbt,25^0,c} \\ P_{igbt,125^0,a} & P_{igbt,125^0,b} & P_{igbt,125^0,c} \end{bmatrix} = \begin{bmatrix} 0.02365 & 1.551 & -0.8995 \\ 0.02876 & 1.914 & -2.452 \end{bmatrix}$$

The power loss equation is in second order, but the first order approximation calculates the coefficients. In other words, when the loss equation is n^{th} order then the related coefficient approximation should the $(n-1)^{th}$ order.

$$\begin{aligned} a_0 &= \frac{P_{igbt,25^0,a} \times T_{max} - P_{igbt,125^0,a} \times T_{min}}{T_{max} - T_{min}} \\ &= \frac{(0.02365 \times 125) - (0.02876 \times 25)}{125 - 25} \\ &= 0.0224 \end{aligned}$$

$$a_1 = \frac{P_{igbt,125^0,a} - P_{igbt,25^0,a}}{T_{max} - T_{min}} = 0.00005$$

$$b_0 = \frac{P_{igbt,25^0,b} \times T_{max} - P_{igbt,125^0,b} \times T_{min}}{T_{max} - T_{min}} = 1.46025$$

$$b_1 = \frac{P_{igbt,125^0,b} - P_{igbt,25^0,b}}{T_{max} - T_{min}} = 0.00363$$

$$c_0 = \frac{P_{igbt,25^0,c} \times T_{max} - P_{igbt,125^0,c} \times T_{min}}{T_{max} - T_{min}} = -0.511375$$

$$c_1 = \frac{P_{igbt,125^0,c} - P_{igbt,25^0,c}}{T_{max} - T_{min}} = -0.015525$$

An equationA.3 will be modified as follows by substituting all the above constants,

$$\begin{aligned} P_{igbt}(i_c, T) = &(0.0224 + 0.000058 \times T)i_c^2 + (1.46025 + 0.00363 \times T)i_c \\ &- (0.511375 + 0.015525 \times T) \end{aligned} \tag{A.4}$$

A.0.1.2 Anti-parallel diode-conduction loss (P_D) calculation

The anti parallel diode follows the same steps what the IGBT has done for calculating it's conduction losses.

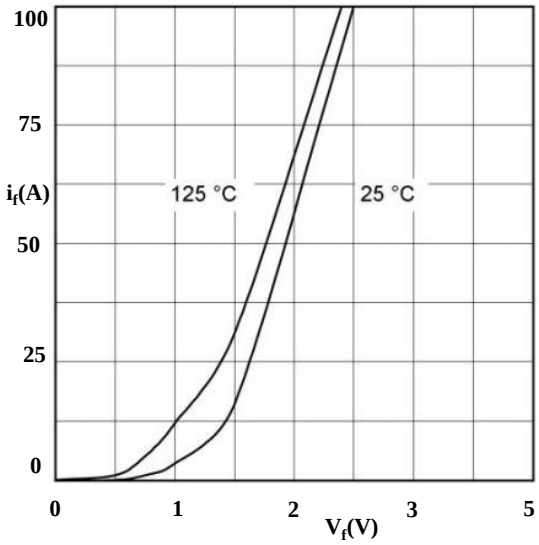


Figure A.5: Anti-parallel diode under investigation

- First, trace the corresponding diode characteristic curve V_f(Forward voltage drop of the diode) versus i_f (Forward leakage current of the diode) from the data-sheet which is depicted in the FigureA.5.

- Second, trace the samples from the diode characteristic curves for minimum and maximum temperatures, it is described in TableA.3.

- Third, consider the X-axis data as $i_{f,25^0}$ ans Y-axis data as $P_{D,25^0}$ for $T_{min} = 25^0$ and fit the data into the MATLAB curve fitting application to get suitable loss equation in terms of i_f. In the same fashion, we can get the another loss equation for $T_{max} = 125^0$. The optimised diode conduction loss equations (A.5 & A.6) and curve fitting graphs(A.6) are given below.

- Fourth, Incorporate the temperature dependency in the conduction loss equation as similar to the equation A.3 for this anti-parallel diode. Finally, the temperature dependent loss expression arrives at equation A.7.

$$P_{D,25^0} = 0.01521 i_f^2 + 1.245 i_f - 0.2321 \tag{A.5}$$

$$P_{D,125^0} = 0.01485 i_f^2 + 1.06 i_f - 0.8451 \tag{A.6}$$

Table A.3: V_f- i_f curve data points for $T_{min} = 25^0$ and $T_{max} = 125^0$

$V_{f,25^0}$(V)	$i_{f,25^0}$(A)	$P_{D,25^0} = (V_{f,25^0} \times i_{f,25^0})$	$V_{f,125^0}$(V)	$i_{f,125^0}$(A)	$P_{D,125^0} = (V_{f,125^0} \times i_{f,125^0})$
0	0	0	0	0	0
0.5	0	0	0.5	1.7143	0.8571
1	2.8571	2.8571	1	10	10
1.5	17.1429	25.714	1.5	30	45
2	50	100	2	64.2857	128.5714

Thereby, the coefficient matrix of the diode conduction loss parameter is deduced as follows.

$$\begin{bmatrix} P_{D,25^0,a} & P_{D,25^0,b} & P_{D,25^0,c} \\ P_{D,125^0,a} & P_{D,125^0,b} & P_{D,125^0,c} \end{bmatrix} = \begin{bmatrix} 0.01521 & 1.245 & -0.2321 \\ 0.01485 & 1.06 & -0.8451 \end{bmatrix}$$

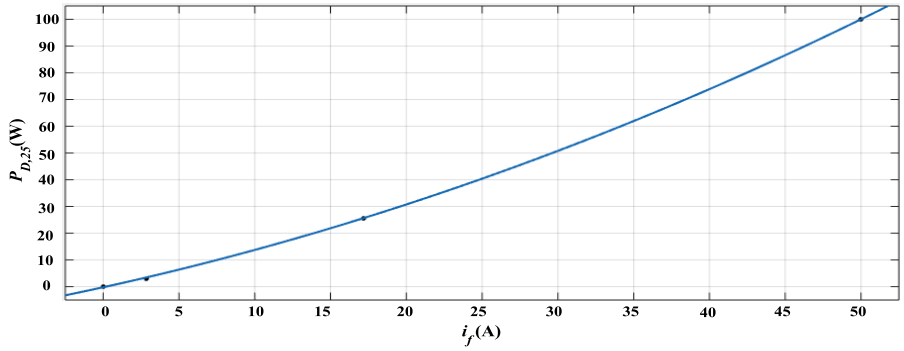
$$P_D(i_f, T) = (0.0153 \times T)i_f^2 + (1.2913 - 0.0019 \times T)i_f - (0.0789 + 0.0061 \times T) \tag{A.7}$$

A.0.2 Switching losses

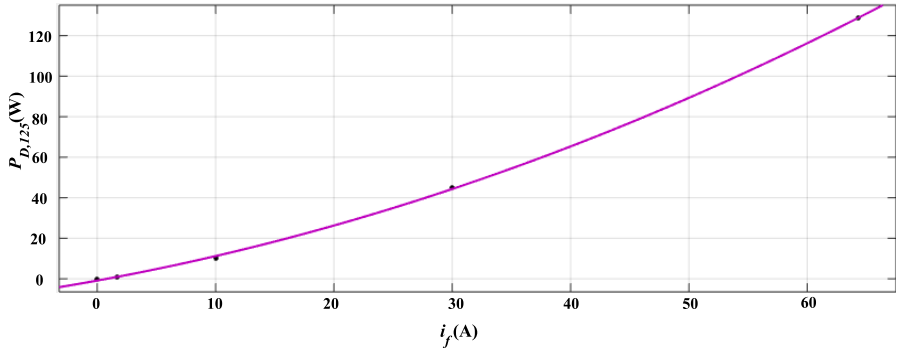
The switching losses usually contribute a notable weight in the total power electronic device losses. Switching loss analysis is significant to estimate the junction temperature for improving the system reliability. [Chen and Downer (2004), Drofenik and Kolar (2005)] calculated switching losses by using a very simple calculations in MATLAB.

A.0.2.1 Switching loss factor calculation for the IGBT switch

The semiconductor device data-sheets are often provided the current dependency of the energy loss graphs as shown in the FigureA.7. Now we have to trace and tabulate the total energy loss (E_{total}) samples from the Figure A.7 concerning the current waveform samples and is described in Table A.4. Herein, the ratio of the total switching energy loss ($E_{ON} + E_{OFF}$) to the current has defined as a switching loss factor ($K_{IGBT}(i_C)$) which can be approximated by a third-order polynomial curve fitting graph as also presented in FigureA.8.



(a)



(b)

Figure A.6: Diode curve fitting graphs for calculating conduction loss (P_D) : (a) At the minimum temperature 25^0C (b) At max temperature 125^0C

$$K_{IGBT}(i_C) = \frac{E_{total}}{i_C}[\frac{\mu Ws}{A}]$$
$$= 0.0001487 \times i_c^3 - 0.03366 \times i_c^2 + 3.224 \times i_c + 170.3 \quad \text{(A.8)}$$

A.0.2.2 Switching loss factor calculation for the anti-parallel diode

The diode turn-on energy losses are negligible so that only turn-off energy losses are considered. The diode turn-off energy loss concerning the forward current i_f is shown in FigureA.9. Herein, considered $R_G = 24\Omega$ from the data-sheet and proceeded the above-defined steps to find the switching factor K_D. Now, the final expression is derived and described in equation A.9.

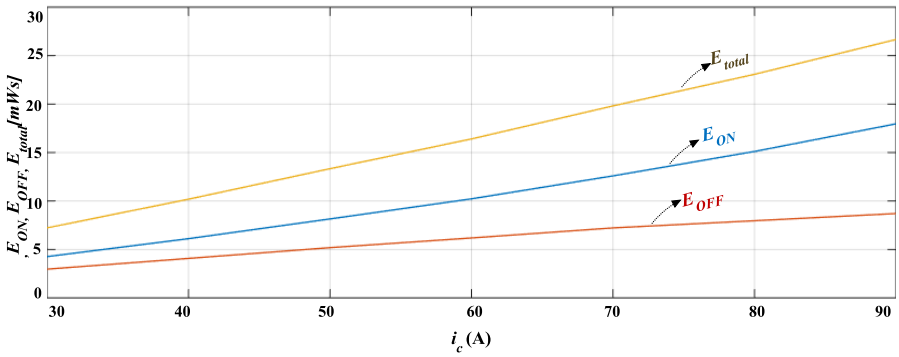


Figure A.7: Device-switching energy loss characteristic graphs of the SKM75GB123D-IGBT switch depend on collector current i_c

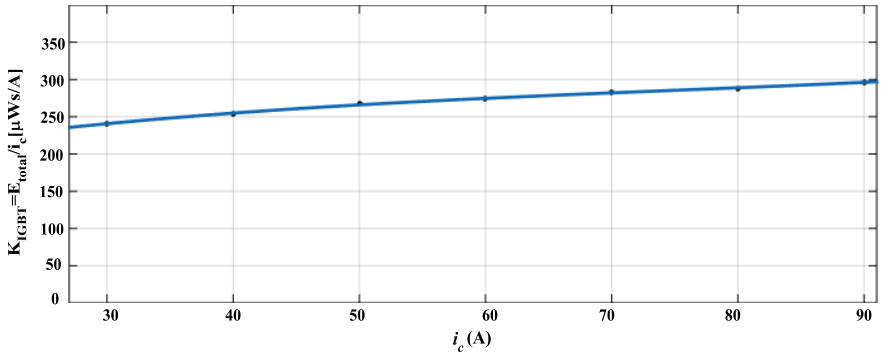


Figure A.8: The parameter $K_{IGBT}(i_C)$ for a given maximum junction temperature ($T_{max} = 125^0$)

Table A.4: Extraction of the samples for deducing the switching factor at $T_{max} = 125^0$

i_C(A)	E_{ON}(mWs)	E_{OFF}(mWs)	E_{total}(mWs)	$K_{IGBT}(i_C)[\frac{\mu Ws}{A}]$
30	4.2593	2.9630	7.2223	240.7
40	6.1111	4.0741	10.1852	254.6
50	8.1481	5.1852	13.3333	266.7
60	10.2222	6.1852	16.4074	273.5
70	12.5926	7.2222	19.8148	283.1
80	15.1111	7.9630	23.0741	288.4
90	17.9630	8.7037	26.6667	296.3

$$K_D(i_f) = \frac{E_{OFF}}{i_f}[\frac{\mu Ws}{A}] = -0.00077266 \times i_f^2 - 0.0436 \times i_f + 65.53 \tag{A.9}$$

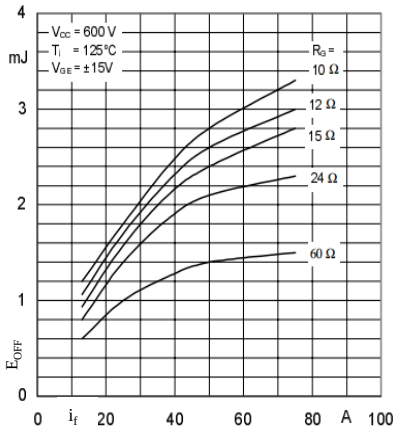


Figure A.9: Diode turn-off energy dissipation per one switching

Appendix B

DESCRIPTION OF EXPERIMENTAL PLATFORM

This chapter describes the experimental setup and software used to implement the developed control strategies and a detailed description of the laboratory prototype.

B.1 Overview of the experimental platform

The generalised block diagram representation of the developed prototype is shown in Figure B.1. The setup comprises of the following units:

- A computer for rapid-prototyping and real-time control
- An OP5142-Real Time(RT) Simulator with an inbuilt compiler to run the program developed, signal feedback, control signal generation and communicating with the computer
- Interface cards (Isolations, dead band circuit, etc.)
- Power circuit board (IGBTs and gate drivers)
- The current sensors and voltage sensors
- DC supplies
- The load box

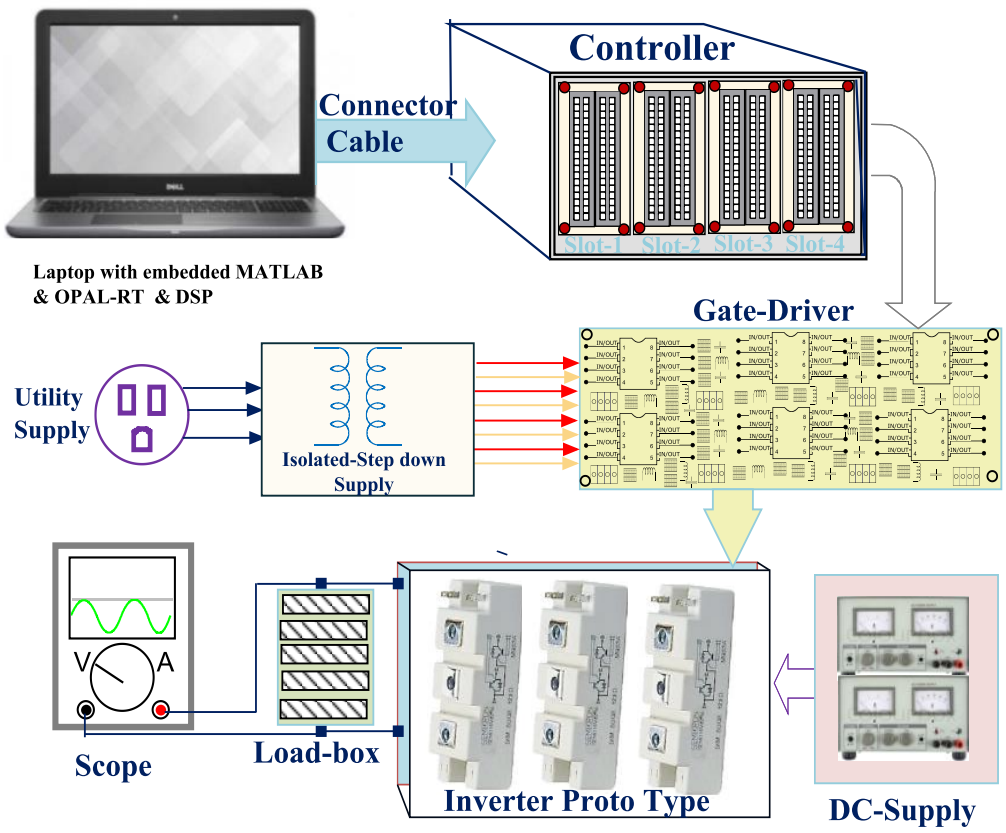


Figure B.1: Platform of the experimental setup

B.2 OP5142-RT Simulator

OP5142-RT Simulator is designed to enable rapid prototyping and real-time simulation (Hardware-In-the-Loop) of various engineering applications like complex power grids, wind farms, micro-grids and hybrid vehicle with step time as low as 10microseconds to attain the excellent simulation accuracy. The picture of the OP5600 simulator and its back and front views along with inside FPGA layout is shown in Figure B.2. The user has the flexibility to develop the desired model using Simulink which is further compiled for generating the appropriate C-code. The generated C-code is dumped into the FPGA platform. In the present work, the simulator has been used as the controller to provide the experimental switching signals. The following are the essential specifications of the OP5600 simulator:

Compatible Simulation Systems and Software

- RT-LAB

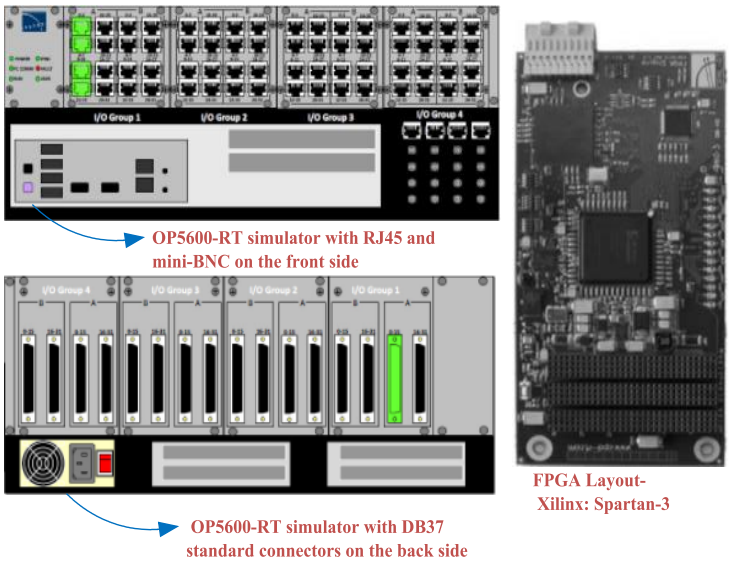


Figure B.2: The OP5600 Simulator layout

- HYPERSIM
- eMEGASIM
- ePHASORSIM
- eFPGASIM

CPU

- INTEL XEON E5
- XILINX FPGA (standard confguration): Spartan 3 (3.3 GHz) processor with Red Hat Linux
- Hard (disc 250 Gb, 7200 rpm, SATA)

Number of cores

- 4 for general purpose
- 8, 16, or 32 for complex networks

I/O and connectors

- I/O modules with 16 analog or 32 digital signals: 8
- Maximum number of I/O channels : 256
- Connectors: 4 panels of 4 DB37F

B.2.1 Steps to dump the .mdl file in OP5600-RT Simulator through MATLAB/Simulink

The user has to follow the standard steps to run the active Simulink model in RT-platform.

1. Prior mandatory changes in the .mdl file:

    - First, chose the fixed step solver (Step size:50e-6sec in the present case), and single-tasking for periodic sample times.
    - Second, uncheck the "block reduction" in "Optimisation" parameters
    - Third, Expand the "Optimisation" and select the "Signals and Parameters." Herein, unchecks the "Signal storage reuse."
    - Fourth, save the model and verify the working status of the model.
    - Fifth, Once the model is running in the Simulink, then split the model into two subsystems.
    - In one subsystem contains only the constant blocks and scopes (This subsystem is named as SC_any name), and other subsystem consists of the plant (This subsystem is named as SM_any name)
    - Place the adequate RT-lab blocks in two subsystems and save the model. Then after closing the MATLAB.

2. Procedure to dump the model into OP5600 simulator

    - Initially keep the OP5600 pertinent bitstream file and .mdl file in the same folder. Moreover, the computer should be pinging with Simulator.
    - Give the right click on the "RT-LABv11.08.13" application and select the "Run as administrator" option. Then RT-LABv11.08.13 application window will open.
    - Create the New Target by giving the right click on "Target" of the Project Explorer and set as a Development node.
    - Now double-click on "create new project" option and give the project name.
    - Add the .mdl file to this project by choosing the "import" option once the new project is created.

- Then automatically the new window will open with the name of .mdl file beside the Target file.
- Four main steps are presented in the side window of "Preparing and Compiling." Follow these steps one by one. First, select the "Edit" to make any modifications in the model. Second, select the "set" to fix the Target platform as a "Redhat." Third, click on "Build" option to build the model in FPGA platform. Fourth, select the "Assign" to fix the targets to the subsystems.
- Later on, Five executing steps are there.

  Step-1: click on "set the executing properties" and choose the Real-time simulation mode as a "Hardware synchronized."

  Step-2: Load the model

  Step-3: Execute the model

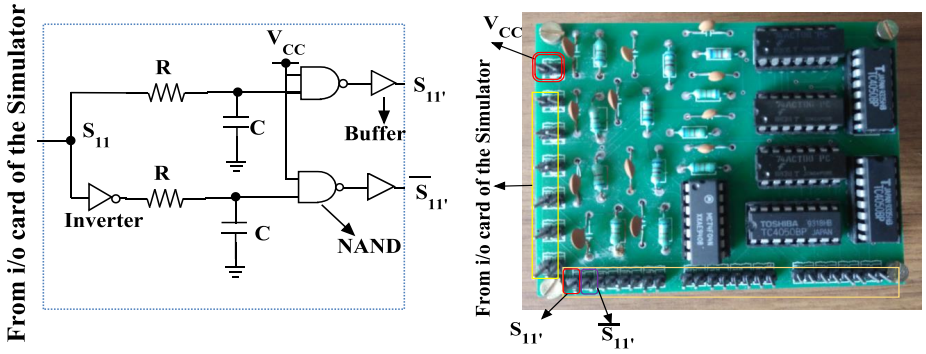
  Step-4: Pass the model to make the hardware connections like collecting the pulses through the i/o card from the Digital output of the OPAL-RT.

  Step-5: Reset the model when the experiment is finished.
- Close the project and RT-LAB application.

B.3 The peripheral interface circuit board

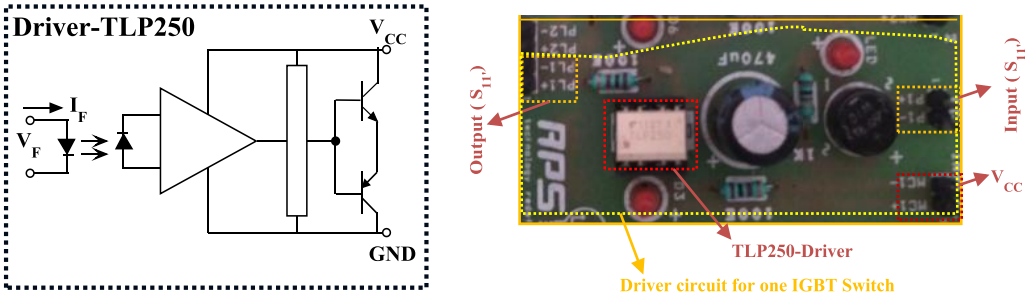
Practically, the power switch exhibits a finite delay time during switching ON and OFF. Thus, it is essential to introduce a small dead time termed as dead band among the switching of power switches constituting a leg or the switches whose simultaneous switching ON leads to the shoot-through condition. The required dead band can be generated in many ways like an analog-based circuit, dedicated digital circuits or using the internal dead band modules of DSPs. In this work, a digital circuit with passive components based dead band generator is developed. The schematic and the printed circuit board (PCB) of the designed dead band circuitry is shown in Figure B.3(a) and Figure B.3(b) respectively. The minimum dead band required for the selected IGBT (SKM75123D) with a rating of 1200 V and 75 A is given as (Xi, 2007).

$$t_{\mathrm{db,min}} = [(t_{\mathrm{d,off}} - t_{\mathrm{d,on}}) + (t_{\mathrm{pd,max}} - t_{\mathrm{pd,min}})] \times 1.2 \tag{B.1}$$



(a) (b)

Figure B.3: (a) Schematic, (b) PCB of the developed dead band circuit.



(a) (b)

Figure B.4: (a) Schematic, (b) PCB of the developed driver circuit and inverter power board.

where, $t_{\mathrm{d,off}}$ and $t_{\mathrm{d,on}}$ respectively are the turn-off and turn-on delay time of the switch, $t_{\mathrm{pd,max}}$ and $t_{\mathrm{pd,min}}$ respectively are the maximum and minimum driver propagation delay. Referring to (Toshiba, 2002) and (SEMITRANS, 2) the value of $t_{\mathrm{db,min}}$ is computed to be

$$t_{\mathrm{db,min}} = [(380 - 44) + (500 - 150)] \times 1.2 = 823.2\,\mathrm{ns} \tag{B.2}$$

Further, the value of R and C is computed using (B.2) as $t_{\mathrm{db,min}} = R \times C$. Taking the nearest values as 100 Ω and 10nF results in a dead band of 1 μs. The schematic and the printed circuit board (PCB) of the developed gate drive is shown in Figure B.4(a) and Figure B.4(b) respectively. Gate driver is an essential part of the power circuit that is responsible for providing the required source and sinking current of the gate to source capacitance of the power switch. The CC-65 AC/ DC current clamp meter

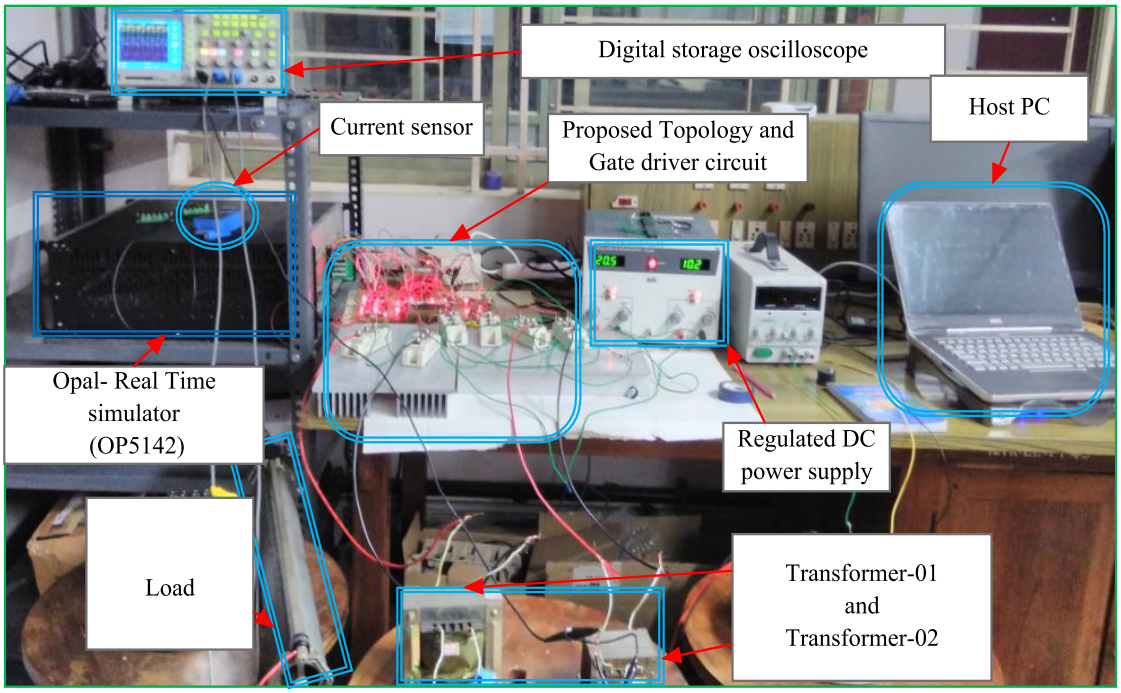


Figure B.5: Experimental setup built with OPAL-RT simulator

is employed for sensing the load current. However, the procedure for the design of the sensors is considered from (Mishra and Sasitharan, 2010). The overall hardware setup with other associated units is shown in Figure B.5.

Bibliography

Abu-Rub, H., Holtz, J., Rodriguez, J., and Baoming, G. (2010). Medium-voltage multilevel convertersstate of the art, challenges, and requirements in industrial applications. *Industrial Electronics, IEEE Transactions on*, 57(8):2581–2596.

Alilu, S., Babaei, E., and Mozafari, S. (2013). A new general topology for multilevel inverters based on developed h-bridge. *Proc. PEDSTC*, pages IR–113.

Alishah, R. S., Nazarpour, D., Hosseini, S. H., and Sabahi, M. (2014). New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels. *IET Power Electronics*, 7(1):96–104.

Apsley, J. M., Gonzalez-Villasenor, A., Barnes, M., Smith, A. C., Williamson, S., Schuddebeurs, J. D., Norman, P. J., Booth, C. D., Burt, G. M., and McDonald, J. (2009). Propulsion drive models for full electric marine propulsion systems. *IEEE Transactions on Industry Applications*, 45(2):676–684.

Araujo-Vargas, I., Cano-Pulido, K., Ramirez-Hernandez, J., Mondragon-Escamilla, N., Nicolas-Villalva, C.-I., Villarruel-Parra, A., Cortes-Rodriguez, D.-d.-J., and Perez-Pinal, F.-J. (2014). A single dc-source seven-level inverter for utility equipment of metro railway, power-land substations. *Industry Applications, IEEE Transactions on*, 50(6):3876–3892.

Babaei, E. (2008). A cascade multilevel converter topology with reduced number of switches. *Power Electronics, IEEE Transactions on*, 23(6):2657–2664.

Babaei, E. (2011). Charge balance control methods for a class of fundamental frequency modulated asymmetric cascaded multilevel inverters. *Journal of Power Electronics*, 11(6):811–818.

Babaei, E., Alilu, S., and Laali, S. (2014a). A new general topology for cascaded multilevel inverters with reduced number of components based on developed h-bridge. *Industrial Electronics, IEEE Transactions on*, 61(8):3932–3939.

Babaei, E. and Farhadi Kangarlu, M. (2011). Multilevel inverter with cross-connected structure. *Iran Patents, Registered under*, (72371).

Babaei, E., Hosseini, S., Gharehpetian, G., Haque, M. T., and Sabahi, M. (2007). Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology. *Electric Power Systems Research*, 77(8):1073–1085.

Babaei, E. and Hosseini, S. H. (2007). Charge balance control methods for asymmetrical cascade multilevel converters. In *Electrical Machines and Systems, 2007. ICEMS. International Conference on*, pages 74–79. IEEE.

Babaei, E. and Hosseini, S. H. (2009). New cascaded multilevel inverter topology with minimum number of switches. *Energy Conversion and Management*, 50(11):2761–2767.

Babaei, E., Kangarlu, M. F., and Mazgar, F. N. (2012). Symmetric and asymmetric multilevel inverter topologies with reduced switching devices. *Electric Power Systems Research*, 86:122–130.

Babaei, E., Kangarlu, M. F., and Sabahi, M. (2014b). Extended multilevel converters: an attempt to reduce the number of independent dc voltage sources in cascaded multilevel converters. *Power Electronics, IET*, 7(1):157–166.

Babaei, E., Laali, S., and Bayat, Z. (2015). A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. *Industrial Electronics, IEEE Transactions on*, 62(2):922–929.

Banaei, M. R., Khounjahan, H., and Salary, E. (2012a). Single-source cascaded transformers multilevel inverter with reduced number of switches. *Power Electronics, IET*, 5(9):1748–1753.

Banaei, M. R., Salary, E., et al. (2012b). Single-source cascaded transformers multilevel inverter with reduced number of switches. *IET Power Electronics*, 5(9):1748–1753.

Behara, S., Sandeep, N., and Udaykumar, R. (2016). Transformer-based seven-level inverter with single-dc supply for renewable energy applications. In *Power Electronics (IICPE), 2016 7th India International Conference on*, pages 1–6. IEEE.

BinWu (2006). *High-power converters and AC drives*. John Wiley & Sons.

Chen, J. and Downer, S. (2004). Mosfet loss and junction temperature calculation model in matlab. In *Proc. PCIM*, volume 4, pages 23–27.

Cheng, Y., Qian, C., Crow, M. L., Pekarek, S., and Atcitty, S. (2006). A comparison of diode-clamped and cascaded multilevel converters for a statcom with energy storage. *IEEE Transactions on Industrial Electronics*, 53(5):1512–1521.

Choi, J.-S. and Kang, F.-s. (2015). Seven-level pwm inverter employing series-connected capacitors paralleled to a single dc voltage source. *Industrial Electronics, IEEE Transactions on*, 62(6):3448–3459.

Choi, W.-k. and Kang, F.-s. (2009). H-bridge based multilevel inverter using pwm switching function. In *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*, pages 1–5. IEEE.

Colak, I., Kabalci, E., and Bayindir, R. (2011). Review of multilevel voltage source inverter topologies and control schemes. *Energy Conversion and Management*, 52(2):1114–1128.

Cortés, P., Ortiz, G., Yuz, J. I., Rodríguez, J., Vazquez, S., and Franquelo, L. G. (2009). Model predictive control of an inverter with output *lc* filter for ups applications. *IEEE Transactions on Industrial Electronics*, 56(6):1875–1883.

Dahidah, M. S. and Agelidis, V. G. (2008). Selective harmonic elimination pwm control for cascaded multilevel voltage source converters: A generalized formula. *IEEE Transactions on power electronics*, 23(4):1620–1630.

Dixon, J., Bretón, A., Ríos, F. E., Rodríguez, J., Pontt, J., Pérez, M., et al. (2007). High-power machine drive, using nonredundant 27-level inverters and active front end rectifiers. *Power Electronics, IEEE Transactions on*, 22(6):2527–2533.

Drofenik, U. and Kolar, J. W. (2005). A general scheme for calculating switching- and conduction-losses of power semiconductors in numerical circuit simulations

of power electronic systems. In *Proceedings of the 2005 International Power Electronics Conference (IPEC05), Niigata, Japan, April*, pages 4–8. Citeseer.

Du, Z., Tolbert, L. M., and Chiasson, J. N. (2006). Active harmonic elimination for multilevel converters. *Power Electronics, IEEE Transactions on*, 21(2):459–469.

Ebrahimi, J., Babaei, E., and Gharehpetian, G. B. (2012). A new multilevel converter topology with reduced number of power electronic components. *Industrial Electronics, IEEE Transactions on*, 59(2):655–667.

Flores, P., Dixon, J., Ortúzar, M., Carmi, R., Barriuso, P., and Morán, L. (2009). Static var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells. *IEEE Transactions on Industrial Electronics*, 56(1):130–138.

Franquelo, L. G., Rodriguez, J., Leon, J., Kouro, S., Portillo, R., et al. (2008). The age of multilevel converters arrives. *Industrial Electronics Magazine, IEEE*, 2(2):28–39.

Gupta, K. and Jain, S. (2012a). Topology for multilevel inverters to attain maximum number of levels from given dc sources. *Power Electronics, IET*, 5(4):435–446.

Gupta, K. K. and Jain, S. (2012b). Theoretical analysis and experimental validation of a novel multilevel inverter topology for renewable energy interfacing applications. *Journal of Renewable and Sustainable Energy*, 4(1):013113.

Gupta, K. K. and Jain, S. (2014). Comprehensive review of a recently proposed multilevel inverter. *IET Power Electronics*, 7(3):467–479.

Hammond, P. W. (1995). A new approach to enhance power quality for medium voltage drives. In *Petroleum and Chemical Industry Conference, 1995. Record of Conference Papers., Industry Applications Society 42nd Annual*, pages 231–235. IEEE.

Hinago, Y. and Koizumi, H. (2010). A single-phase multilevel inverter using switched series/parallel dc voltage sources. *Industrial Electronics, IEEE Transactions on*, 57(8):2643–2650.

Holtz, J. (1994). Pulsewidth modulation for electronic power conversion. *Proceedings of the IEEE*, 82(8):1194–1214.

Islam, M. R., Guo, Y., and Zhu, J. (2014). A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems. *IEEE Transactions on Power Electronics*, 29(8):4167–4182.

Jinghua, Z. and Zhengxi, L. (2008). Research on hybrid modulation strategies based on general hybrid topology of multilevel inverter. In *Power Electronics, Electrical Drives, Automation and Motion, 2008. SPEEDAM 2008. International Symposium on*, pages 784–788. IEEE.

Kang, F.-S., Park, S.-J., Cho, S. E., Kim, C.-U., and Ise, T. (2005). Multilevel pwm inverters suitable for the use of stand-alone photovoltaic power systems. *Energy Conversion, IEEE Transactions on*, 20(4):906–915.

Kangarlu, M. F. and Babaei, E. (2013). Cross-switched multilevel inverter: an innovative topology. *IET Power Electronics*, 6(4):642–651.

Kangarlu, M. F., Babaei, E., and Laali, S. (2012). Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources. *IET Power Electronics*, 5(5):571–581.

Khomfoi, S. and Aimsaard, C. (2009). A 5-level cascaded hybrid multilevel inverter for interfacing with renewable energy resources. In *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, 2009. ECTI-CON 2009. 6th International Conference on*, volume 1, pages 284–287. IEEE.

Kouro, S., Bernal, R., Miranda, H., Silva, C. A., and Rodríguez, J. (2007a). High-performance torque and flux control for multilevel inverter fed induction motors. *IEEE Transactions on Power Electronics*, 22(6):2116–2123.

Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L. G., Wu, B., Rodriguez, J., Pérez, M. A., and Leon, J. I. (2010). Recent advances and industrial applications of multilevel converters. *IEEE Trans. Ind. Electron.*, 57(8):2553–2580.

Kouro, S., Rebolledo, J., and Rodríguez, J. (2007b). Reduced switching-frequency-modulation algorithm for high-power multilevel inverters. *Industrial Electronics, IEEE Transactions on*, 54(5):2894–2901.

Kumar, N. K. and Sivakumar, K. (2015). A quad two-level inverter configuration for four-pole induction-motor drive with single dc link. *Industrial Electronics, IEEE Transactions on*, 62(1):105–112.

Laali, S., Abbaszadeh, K., and Lesani, H. (2010). A new algorithm to determine the magnitudes of dc voltage sources in asymmetric cascaded multilevel converters capable of using charge balance control methods. In *Electrical Machines and Systems (ICEMS), 2010 International Conference on*, pages 56–61. IEEE.

Lai, J.-S. and Peng, F. Z. (1996). Multilevel converters-a new breed of power converters. *Industry Applications, IEEE Transactions on*, 32(3):509–517.

Lai, Y.-S. and Shyu, F.-S. (2002). Topology for hybrid multilevel inverter. *IEE Proceedings-Electric Power Applications*, 149(6):449–458.

Lee, S. and Kang, F. (2008). A new structure of h-bridge multilevel inverter. In *Proc. KIPE Conf.*, pages 388–390.

Leon, J. I., Kouro, S., Vazquez, S., Portillo, R., Franquelo, L. G., Carrasco, J. M., and Rodriguez, J. (2011). Multidimensional modulation technique for cascaded multilevel converters. *Industrial Electronics, IEEE Transactions on*, 58(2):412–420.

Li, L., Czarkowski, D., Liu, Y., and Pillay, P. (2000a). Multilevel selective harmonic elimination pwm technique in series-connected voltage inverters. *IEEE Transactions on Industry Applications*, 36(1):160–170.

Li, L., Czarkowski, D., Liu, Y., and Pillay, P. (2000b). Multilevel selective harmonic elimination pwm technique in series-connected voltage inverters. *IEEE Transactions on Industry Applications*, 36(1):160–170.

Liao, Y.-H. and Lai, C.-M. (2011). Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources. *IEEE Transactions on Power Electronics*, 26(9):2386–2392.

Lipo, T. A. and Manjrekar, M. D. (1999). Hybrid topology for multilevel power conversion. US Patent 6,005,788.

Liu, H., Tolbert, L. M., Khomfoi, S., Ozpineci, B., and Du, Z. (2008). Hybrid cascaded multilevel inverter with pwm control method. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pages 162–166. IEEE.

Liu, Y. and Luo, F. (2005). Trinary hybrid multilevel inverter used in statcom with unbalanced voltages. *IEE Proceedings-Electric Power Applications*, 152(5):1203–1222.

Lund, R., Manjrekar, M. D., Steimer, P., and Lipo, T. A. (1999). Control strategies for a hybrid seven-level inverter. In *Proceedings of the European Power Electronic Conference*.

Malinowsk-Gopakumar, K., Rodriguez, J., and Perez, M. A. (2010). A survey on cascaded multilevel inverters. *Industrial Electronics, IEEE Transactions on*, 57(7):2197–2206. cited by 785.

Manjrekar, M. and Venkataramanan, G. (1996). Advanced topologies and modulation strategies for multilevel inverters. In *Power Electronics Specialists Conference, 1996. PESC'96 Record., 27th Annual IEEE*, volume 2, pages 1013–1018. IEEE.

Manjrekar, M. D., Lip, T., et al. (1998). A hybrid multilevel inverter topology for drive applications. In *Applied Power Electronics Conference and Exposition, 1998. APEC'98. Conference Proceedings 1998., Thirteenth Annual*, volume 2, pages 523–529. IEEE.

Manjrekar, M. D., Steimer, P. K., and Lipo, T. A. (2000). Hybrid multilevel power conversion system: a competitive solution for high-power applications. *IEEE Trans. Ind. Appl.*, 36(3):834–841.

Marchesoni, M., Mazzucchelli, M., and Tenconi, S. (1990). A nonconventional power converter for plasma stabilization. *IEEE Trans. Power Electron.*, 5(2):212–219.

McGrath, B. P. and Holmes, D. G. (2002). Multicarrier pwm strategies for multilevel inverters. *IEEE Transactions on industrial electronics*, 49(4):858–867.

Mcmurray, W. (1971). Fast response stepped-wave switching power converter circuit. US Patent 3,581,212.

Meynard, T. and Foch, H. (1992). Multi-level conversion: high voltage choppers and voltage-source inverters. In *Power Electronics Specialists Conference, 1992. PESC'92 Record., 23rd Annual IEEE*, pages 397–403. IEEE.

Mishra, M. K., K.-K. V. G. and Sasitharan, S. (2010). A dsp-based integrated hardware set-up for a dstatcom: design, development, and implementation issues. *IETE Journal of Research*, 56(1):11–21.

Mokhberdoran, A. and Ajami, A. (2014a). Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology. *Power Electronics, IEEE Transactions on*, 29(12):6712–6724.

Mokhberdoran, A. and Ajami, A. (2014b). Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology. *Power Electronics, IEEE Transactions on*, 29(12):6712–6724.

Mueller, O. M. and Gran, R. J. (1998). Reducing switching losses in series connected bridge inverters and amplifiers. US Patent 5,734,565.

Nabae, A., Takahashi, I., and Akagi, H. (1981). A new neutral-point-clamped pwm inverter. *IEEE Transactions on industry applications*, (5):518–523.

Nami, A., Liang, J., Dijkhuizen, F., and Demetriades, G. D. (2015). Modular multilevel converters for hvdc applications: Review on converter cells and functionalities. *Power Electronics, IEEE Transactions on*, 30(1):18–36.

Nami, A., Wang, L., Dijkhuizen, F., and Shukla, A. (2013). Five level cross connected cell for cascaded converters. *European Power Electronics (EPE2013), Lille, France*.

Nami, A., Zare, F., Ghosh, A., and Blaabjerg, F. (2011). A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped h-bridge cells. *Power Electronics, IEEE Transactions on*, 26(1):51–65.

Ounejjar, Y., Al-Haddad, K., and Gregoire, L.-A. (2011). Packed u cells multilevel converter topology: theoretical study and experimental validation. *Industrial Electronics, IEEE Transactions on*, 58(4):1294–1306.

Peng, F. Z. (2000). A generalized multilevel inverter topology with self voltage balancing. In *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE*, volume 3, pages 2024–2031. IEEE.

Peng, F. Z., Lai, J.-S., McKeever, J. W., and VanCoevering, J. (1996). A multilevel voltage-source inverter with separate dc sources for static var generation. *IEEE Transactions on Industry Applications*, 32(5):1130–1138.

Pereda, J. and Dixon, J. (2011). High-frequency link: a solution for using only one dc source in asymmetric cascaded multilevel inverters. *Industrial Electronics, IEEE Transactions on*, 58(9):3884–3892.

Pereda, J. and Dixon, J. (2012). 23-level inverter for electric vehicles using a single battery pack and series active filters. *IEEE Transactions on vehicular technology*, 61(3):1043–1051.

Pérez, M., Rodriguez, J., Pontt, J., and Kouro, S. (2007). Power distribution in hybrid multi-cell converter with nearest level modulation. In *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, pages 736–741. IEEE.

Rahman, M. A., Quaicoe, J. E., and Choudhury, M. (1987). Performance analysis of delta modulated pwm inverters. *IEEE Transactions on power electronics*, (3):227–233.

Rajeevan, P., Sivakumar, K., Patel, C., Gopakumar, K., and Haitham, A.-R. (2011). A hybrid nine-level inverter for im drive. In *Industrial Electronics (ISIE), 2011 IEEE International Symposium on*, pages 65–70. IEEE.

Rech, C. and Pinheiro, J. R. (2007). Hybrid multilevel converters: Unified analysis and design considerations. *Industrial Electronics, IEEE Transactions on*, 54(2):1092–1104.

Rodriguez, J., Franquelo, L. G., Kouro, S., Leon, J. I., Portillo, R. C., Prats, M. A. M., and Perez, M. A. (2009). Multilevel converters: An enabling technology for high-power applications. *Proceedings of the IEEE*, 97(11):1786–1817.

Rodriguez, J., Lai, J.-S., and Peng, F. Z. (2002). Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.*, 49(4):724–738.

Rodriguez-Bernet (2007). Multilevel voltage-source-converter topologies for industrial medium-voltage drives. *Industrial Electronics, IEEE Transactions on*, 54(6):2930–2945.

Ruiz-Caballero, D., Ramos-Astudillo, R. M., Mussa, S. A., Heldwein, M. L., et al. (2010). Symmetrical hybrid multilevel dc–ac converters with reduced number of insulated dc supplies. *Industrial Electronics, IEEE Transactions on*, 57(7):2307–2314.

Sabate, J., Garces, L. J., Szczesny, P. M., Li, Q., and Wirth, W. F. (2004). High-power high-fidelity switching amplifier driving gradient coils for mri systems. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 1, pages 261–266. IEEE.

Saeedifard, M., Barbosa, P. M., and Steimer, P. K. (2012). Operation and control of a hybrid seven-level converter. *IEEE Transactions on Power Electronics*, 27(2):652–660.

Samadaei, E., Gholamian, S., Sheikholeslami, A., and Adabi, J. (2016). An envelope type (e-type) module: Asymmetric multilevel inverters with reduced components.

Sanjeevan, A. R., Kaarthik, R. S., Gopakumar, K., Rajeevan, P., Leon, J. I., and Franquelo, L. G. (2015). Reduced common-mode voltage operation of a new seven-level hybrid multilevel inverter topology with a single dc voltage source. *IET Power Electronics*.

SEMITRANS, S. (2). Igbt modules.

Sepahvand, H., Liao, J., Ferdowsi, M., and Corzine, K. A. (2013). Capacitor voltage regulation in single-dc-source cascaded h-bridge multilevel converters using phase-shift modulation. *Industrial Electronics, IEEE Transactions on*, 60(9):3619–3626.

Sirisukprasert, S., Huang, A. Q., and Lai, J.-S. (2003). Modeling, analysis and control of cascaded-multilevel converter-based statcom. In *Power Engineering Society General Meeting, 2003, IEEE*, volume 4, pages 2561–2568. IEEE.

Soto, D., Pena, R., Reyes, L., and Vasquez, M. (2003). A novel cascaded multilevel converter with a single nonisolated dc link. In *Power Electronics Specialist Conference, 2003. PESC'03. 2003 IEEE 34th Annual*, volume 4, pages 1627–1632. IEEE.

Stynski, S., San-Sebastian, J., Malinowski, M., and Etxeberria-Otadui, I. (2009). Analysis of multilevel pwm converter based on flc modules for an ac traction application. In *Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*, pages 1–6. IEEE.

Sujanarko, B., Ashari, M., and Purnomo, M. H. (2010). Improved voltage of cascaded inverters using sine quantization progression. *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, 8(2):123–130.

Suresh, Y. and Panda, A. K. (2010). Performance of cascade multilevel h-bridge inverter with single dc source by employing low frequency three-phase transformers. In *IECON 2010-36th Annual Conference on IEEE Industrial Electronics Society*, pages 1981–1986. IEEE.

Suresh, Y., Venkataramanaiah, J., Panda, A. K., Dhanamjayulu, C., and Venugopal, P. (2017). Investigation on cascade multilevel inverter with symmetric, asymmetric, hybrid and multi-cell configurations. *Ain Shams Engineering Journal*, 8(2):263–276.

Taghizadeh, H. and Hagh, M. T. (2010). Harmonic elimination of cascade multilevel inverters with nonequal dc sources using particle swarm optimization. *IEEE Transactions on Industrial Electronics*, 57(11):3678–3684.

Tolbert, L. M. and Habetler, T. G. (1998). Novel multilevel inverter carrier-based pwm methods. In *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. the 1998 IEEE*, volume 2, pages 1424–1431. IEEE.

Tolbert, L. M. and Peng, F. Z. (2000). Multilevel converters as a utility interface for renewable energy systems. In *Power Engineering Society Summer Meeting, 2000. IEEE*, volume 2, pages 1271–1274. IEEE.

Toshiba, D. (2002). Tlp250 (inv) rev.

Trzynadlowski, A. M., Blaabjerg, F., Pedersen, J. K., Kirlin, R. L., and Legowski, S. (1994). Random pulse width modulation techniques for converter-fed drive systems-a review. *IEEE Transactions on Industry Applications*, 30(5):1166–1175.

Tsang, K.-M. and Chan, W.-L. (2014). Single dc source three-phase multilevel inverter using reduced number of switches. *Power Electronics, IET*, 7(4):775–783.

Varschavsky, A., Dixon, J., Rotella, M., and Morán, L. (2010). Cascaded nine-level inverter for hybrid-series active power filter, using industrial controller. *Industrial Electronics, IEEE Transactions on*, 57(8):2761–2767.

Waltrich, G. and Barbi, I. (2010). Three-phase cascaded multilevel inverter using power cells with two inverter legs in series. *Industrial Electronics, IEEE Transactions on*, 57(8):2605–2612.

Wang, Y., Li, H., Shi, X., and Xu, B. (2004). A novel carrier-based pwm strategy for hybrid multilevel inverters. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 6, pages 4233–4237. IEEE.

Xi, Z. (2007). How to calculate and minimize the dead time requirement for igbts properly. *EUPEC application note AN2007-04. V1. 0*.

Zeng, F.-P., Tan, G.-H., Wang, J.-Z., and Ji, Y.-C. (2010). Novel single-phase five-level voltage-source inverter for the shunt active power filter. *IET Power Electronics*, 3(4):480–489.

Zhang, J., Zou, Y., Zhang, X., and Ding, K. (2001). Study on a modified multilevel cascade inverter with hybrid modulation. In *Power Electronics and Drive Systems, 2001. Proceedings., 2001 4th IEEE International Conference on*, volume 1, pages 379–383. IEEE.

PUBLICATIONS BASED ON THE THESIS

Papers in refereed journals

Papers published

1. J.Venkataramanaiah, Y.Suresh, and A.K.Panda., "Development of a New Hybrid Multilevel Inverter Using Modified Carrier SPWM Switching Strategy.", *IEEE Transactions on Power Electronics* ., Feb. 2018.

2. J.Venkataramanaiah, Y.Suresh, and A.K.Panda., "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies.", *Renewable and Sustainable Energy Reviews, Elsevier.*, vol. 76, pp. 788-812, 2017.

3. J.Venkataramanaiah, Y.Suresh, and A.K.Panda, "Design and Development of a Novel 19-Level Inverter Using an Effective Fundamental Switching Strategy.", *IEEE Journal of Emerging and Selected Topics in Power Electronics.*, 2017 Nov 22.

4. Y.Suresh, J.Venkataramanaiah, A.K.Panda, C.Dhanamjayulu, & P.Venugopal,"Investigation on cascade multilevel inverter with symmetric, asymmetric, hybrid and multi-cell configurations.", *Ain Shams Engineering Journal, Elsevier.*,vol. 8(2), pp. 263-76., 2017 Jun 1.

Papers published in refereed conference proceedings

1. J.Venkataramanaiah, and Y.Suresh., "Performance Verification of a New Cascaded Transformer Based Multilevel Inverter Using Modified Carrier SPWM Strategy" In Proc. *International Conference on Emerging Trends in Engineering, Science and Technology (ICETEST)* , PICC.,DOI. 978-1-5386-2462-3/18/$31.00 2018 IEEE.

2. J.Venkataramanaiah, K.S.Reddy, and Y.Suresh., "Design and Implementation of a Symmetrical Multilevel Inverter Topology" In Proc. *National Conference on Recent Trends in Power Engineering (NCRTPE)* , Dec 2015.

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