DYNAMIC VOLTAGE RESTORER BASED ON HIGH FREQUENCY LINK DIRECT AC-AC CONVERTER

Thesis

Submitted in partial fulfillment of the requirements for the degree of DOCTOR OF PHILOSOPHY

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May 2016

DECLARATION

I hereby *declare* that the Research Thesis entitled **DYNAMIC VOLTAGE RESTORER BASED ON HIGH FREQUENCY LINK DIRECT AC-AC CONVERTER** which is being submitted to the *National Institute of Technology Karnataka, Surathkal* in partial fulfillment of the requirement for the award of the Degree of *Doctor of Philosophy* in the **Department of Electrical and Electronics Engineering** is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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Research Guide

Chairman-DRPC (Signature with Date and Seal)

Acknowledgements

I would like to express my sincere appreciation to my research supervisor Dr. P. Parthiban, Assistant Professor, Department of Electrical and Electronics Engineering for giving me an opportunity to work under his guidance and for his constant encouragement, guidance, supervision as well as for the motivation during the research. His annotations and thought provoking discussions are the key behind the successful completion of this work. I express my heartful thanks to Dr. Vinatha. U, Head of the Department, Electrical and Electronics Engineering for providing the required facilities to complete the project successfully. I take this opportunity to express my thanks to the teaching and non-teaching staff of the department, for their co-operation during my stay here. Specially I am grateful to my parents, my wife, brothers and all my family members for their help and support during the research. Finally, I thank my friends Yassar Hassan, K. Ravikumar, Gautham Sarang, Arun Augustin, and all those who helped during the research work.

Abstract

Power quality has been a concern for last decade with increase in sensitive loads. Power quality issues affect the quality of production, reduce production efficiency and increases the production cost. Dynamic voltage restorer(DVR) is a power quality improving device used for improving voltage quality to a sensitive load. DVR is connected in series with the supply and injects a voltage in series with the supply voltage to correct the voltage quality problems. The major voltage quality problems identified are voltage sag, voltage swell, voltage harmonics, flicker and voltage imbalance.

DVR is identified to be cost effective solution for protecting sensitive loads from voltage related power quality issues. Conventional DVR is using either energy storage based or two stage ac-dc-ac converter based system. These topologies are bulky and costly due to the big line frequency isolation transformer and bulky dc-link capacitor. The extend of cost reduction and efficiency can be improved by eliminating the injection transformer.

A new DVR topology based on high frequency link direct ac-ac converter is proposed in this work. This topology does not require a line frequency transformer. Instead it uses a high frequency link transformer. High frequency transformer is very small compared to a line frequency transformer. The dc-link capacitance is not required for this topology. A fictitious dclink is maintained. Since the DVR does not have an injection transformer, it has lower loss, lower cost and it is less bulky.

Keywords: Dynamic Voltage Restorer(DVR), voltage sag, transformerless DVR, VSI.

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Nomenclature

| SYMBOL | MEANING | SYMBOL | MEANING | |
|----------------------------|-----------------------------------|------------------|---------------------------------------|--|
| Ω Ohms | | f | Frequency | |
| ω Angular frequency | | ω_0 | Angular frequency at resonance | |
| n | Turns ratio of the HF transformer | ω_{in} | Source voltage angular frequency | |
| Z_L | Load impedance | Z_s | Source impedance | |
| R_L | Load resistance | X_L | Inductive load reactance | |
| Z_F | Fault impedance | R_F | Fault resistance | |
| V_{dc} | dc-link voltage | | | |
| V_{sA}, V_{sB}, V_{sC} | RMS source voltages | d_a, d_b, dc_c | Duty ratios of bidirectional switches | |

Abbreviations

| Abbreviation | Expansion | | |
|----------------------|---|--|--|
| DVR | Dynamic Voltage Restorer | | |
| $_{ m HF}$ | High Frequency | | |
| ac | Alternating Current | | |
| dc | Direct Current | | |
| THD | Total Harmonic Distortion | | |
| PQ | Power Quality | | |
| CRT | Cathode Ray Tube | | |
| CBEMA | Computer Business Equipment Manufacturers Association | | |
| ITIC | Information Technology Industry Council | | |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistors | | |
| IGBT | Insulated Gate Bipolar Transistors | | |
| GTO | Gate Turn-Off thyristors | | |
| IGCT | Integrated Gate Commutated Thyristors | | |
| BIL | Basic Insulation Level | | |
| SMES | Superconducting Magnetic Energy Storage | | |
| VSI | Voltage Source Inverter | | |
| CSI | Current source Inverter | | |
| SPWM | Sinusoidal Pulse Width Modulation | | |
| RMS | Root Mean Square | | |
| PWM | Pulse Width Modulation | | |
| PLC | Programmable Logic Controller | | |
| PET | Power Electronic Transformer | | |
| ZCD | Zero Crossing Detector | | |
| LPF | Low Pass Filter | | |

Chapter 1

Introduction

The ultimate goal of modern industries is to maximize their profit by reducing the production cost. This is possible with continuous production. An uninterpretable and stable power supply is required to achieve this objective. There is enormous increase in the number of sensitive equipments during last few decades like automation devices, power electronic converters, adjustable drives etc. The lack of quality power can lead to complete shut of the plant, causing big financial loss to the industry. But most of the power quality issues are happening in the industry itself. Non-linear loads, sudden inclusion and removal of heavy loads etc are some of the example.

The frequent and severe power quality issues are voltage sag, voltage swell, voltage harmonics, flicker, notches and voltage imbalance. Faults and sudden switching of heavy loads are the main causes of voltage sag. Voltage swell happens mainly due to sudden removal of heavy loads or inclusion of large capacitance load.

The quality of power can be maintained using static or dynamic devices. Dynamic compensation devices can generally called as custom power devices. The voltage quality can be improve by custom power devices such as DVR, DSTATCOM and UPQC. DSTATCOM is a shunt connected device and it injects current to maintain the voltage constant. DVR is a series connected device and it inject voltage in series to the source to improve the voltage quality. DVR is identified to be a cost effective solution for voltage quality problems. The first DVR was installed in 1996 by Westinghouse and is discussed in (Klumpner et al 2000)

There have been lots of papers published on DVR circuit topologies, control techniques, PWM techniques and detection techniques. The presented circuit topologies can be broadly categorized into two.

- 1. DVR that uses an energy storage device,
- 2. DVR that uses ac-dc-ac converter.

In the first group the required dc voltage provided through a transformer from the grid (source side or load side). In the second group of presented topologies for DVR, the required energy for compensation is taken from the dc capacitor or another energy storage element such as double-layer capacitor, superconducting magnet or lead acid battery via an inverter (Nielsen et al. 2005).

There has been very less attention to topologies that do not require any storage element. A zero energy sag corrector has been published in (Prasai et al. 2008), which is able to compensate balanced and unbalanced voltage sags without using a capacitor. Voltage swells cannot be compensated with this topology. The ability of harmonics compensation has not been investigated.

A topology for single phase DVR based on direct ac-ac converter has been presented in (Perez et al. 2006). The compensation ranges for voltage sags and swells are restricted to 25% and 50% respectively in the presented topology. A DVR based on indirect matrix converter has been published in (Wang et al. 2009). The DVR presented is able to compensate balanced voltage sags. This topology needs a flywheel energy storage element and the capability of the topology for voltage flicker and harmonics has not been investigated. The compensation duration is also limited. Moreover regulation and control of flywheel speed is complicated. In (Babaei et al. 2009), another matrix converter-based DVR has been presented. Two main problems of this topology are the high number of switches and very limited compensation range.

DVR based on reduced number of switches has been presented in (Babaei et al. 2010). He has proposed two topologies. One with four bidirectional switches perphase and the other with six bidirectional switches per-phase. Both topologies need a bulky line frequency isolation transformer. Three phase cannot be compensated with this topology.

In this research work a new topology for three-phase DVR is proposed. The proposed topology is based on high frequency link direct converter. The bulky isolation transformer can be replaced with a small high frequency transformer. This reduces the size and cost of the DVR as the high frequency transformer size is very small compared to the counterpart line frequency transformer. Also the proposed system does not require a big dc-link capacitance.

1.1 Objectives

The quality of the power can be improved with DVR thereby improving the reliability of the supply. The performance analysis of the existing DVR topologies has to be carried out. The main objective of the work is to develop a new topology to improve the performance and functionalities of the DVR. The major objectives of this research work are summarized below.

- 1. To carry out the extensive literature review to understand the state of the art of the existing DVR topologies.
- 2. To develop new converter topology to improve the performance and reduce the cost of the DVR. DVR topology using dual bridge matrix converter with a high frequency isolation transformer is proposed.
- 3. To suggest a suitable control technique for the proposed topology.
- 4. To do analysis of the DVR for different types of sags .
- 5. To analyze the performance of the proposed DVR topology against different types of loads.

1.2 Organization and Contribution of the Thesis

Chapter 1: General introduction to various power quality issues and its solutions is given in this chapter. Information regarding the background and motivation for the current research on the DVR is provided. Also, the objectives of the thesis is defined including an outline of the thesis. The contribution and organization of the thesis is presented.

Chapter 2: This chapter gives an overview of power quality issues, which are relevant for the design and control of a DVR with focus on voltage dips and interruptions. The power quality standards including IEEE standard is also explained. The components of the DVR and its operating principle and various voltage injection methods are presented. Thereafter, different DVR system topologies are presented with respect to circuit topologies.

Chapter 3: The control strategy of the DVR is discussed in this chapter. The modulation strategy used for the matrix converter is also explained. Automated control technique is used to control the single phase VSI. Voltage sag is produced by a magnitude change with or without a phase shift of the supply voltage. Thus it is necessary to quantify and correct for phase shift (if any) prior to compensate for the voltage sags. To quantify the phase shift a random reference phase angle waveform was generated and by using a feedback control loop the error (between the supply and the reference) phase angle is regulated to zero.

Chapter 4: The simulation results of the DVR against different types of faults and loads are discussed in this chapter. The performance of the same is analyzed with different kinds of loads such as linear and non-linear loads and sag with and without phase shift. The performance of the DVR against different types of sags like single phase sag, three phase symmetric sag and three phase unsymmetrical sag has been discussed. The load is assumed to be fixed in all the cases. The simulation is carried out and the results are analyzed for different voltage sag and load conditions.

Chapter 5: The conclusion and future work are discussed in this chapter.

Chapter 2

Literature Review

2.1 Introduction

Different power quality issues are discussed in this chapter. Since DVR is used to rectify voltage quality problems, more emphasis is given to voltage quality issues. This chapter explains different issues of power quality with emphasis put on voltage quality issues, which are relevant for the DVR. Basic power electronic controllers for voltage dip mitigation are presented giving emphasis on DVR. Basic elements of a conventional DVR is discussed. The different system topologies of the DVR are also discussed. The topologies are classified based on connection to the distribution line.

2.2 Voltage Power Quality Problems

There are so many power quality problems in the power system due to which the power delivered to the end users will be affected (Bollen 2001). Some definitions of general voltage power quality problems are described below.

- 1. Transient
 - (a) Impulsive
 - (b) Oscillatory
- 2. Short duration variations
 - (a) Sag (Dip)

- (b) Swell (Surge)
- 3. Long duration variations
 - (a) Over-voltages
 - (b) Under-voltages
- 4. Interruptions
- 5. Waveform distortion
 - (a) dc offset
 - (b) Harmonics
 - (c) Inter-harmonics
 - (d) Notching
 - (e) Noise
- 6. Voltage flicker
- 7. Voltage unbalance(three phase)
- 8. Frequency variations.

2.2.1 Transient Disturbance

These are sudden change of supply side voltage or the load current. The major causes of transient disturbances are lightning or switching causing injection of energy. Impulsive transients and oscillatory transients are the two classifications. In impulsive transient the distortion is an impulse as shown in Fig. 2.1. Fig. 2.2 shows oscillatory transient waveform in which the distortion is oscillating.

2.2.2 Voltage Sag

Voltage sag is defined as a reduction in RMS value of the voltage from 0.1pu to 0.9pu and last for a duration of 0.5 cycles to one minute. Voltage waveform with a sag is shown in Fig. 2.3. The major causes of voltage sag are faults, sudden change in load such as large motor starting and sudden switching of heavy loads.



Figure 2.1: Impulsive transient waveform



Figure 2.2: Oscillatory transient waveform

2.2.3 Voltage Swell

Voltage swell is defined as an increment in RMS voltage from 1.1pu to 1.8pu and lasts for a duration of 0.5 cycles to one minute as shown in Fig.2.4. The major causes are switching of capacitor, removal of heavy loads and faults.



Figure 2.3: Voltage waveform with a sag



Figure 2.4: Voltage waveform with swell

2.2.4 Over Voltage and Under Voltage

These are long duration voltage variations which lasts more than a minute to less than two days. Under voltages RMS magnitudes varies between from 0.8pu to 1pu. Under voltages are mainly caused by transformers or out of service lines. The magnitude variations in over voltage condition is from 0.1pu to 1.2pu.

2.2.5 Voltage Interruption

The complete loss of electric voltage is called voltage interruption as illustrated in Fig.2.5. Interruptions are mainly caused by circuit breaker re-closures in the case of temporary faults. Interruption causes stopping of sensitive equipments like PLC, ASD and computers, loss of data, unwanted tripping etc.



Figure 2.5: Voltage waveform with interruption

2.2.6 Waveform distortion

2.2.6.1 dc Offset

Inclusion of a dc voltage or current in ac power system causes dc offset. Geometric disturbance due to higher latitude is one of the reasons for dc offset. Half wave rectification also causes dc offset. Half wave rectification also introduces even harmonics in the ac system. Dc offset in ac supply causes transformer saturation in normal operating conditions. Additional heating happens due to this and it reduces the life span of transformer. Electrolytic erosion of connectors and grounding electrodes are another effect of dc offset.

2.2.6.2 Harmonics

Harmonics are distortion caused by integer multiple of the frequency of a base signal, called the fundamental. The harmonics are mainly caused by non-linear loads and devices. Harmonics is analyzed using harmonic spectrum. Harmonic spectrum gives the magnitude of the harmonic contents versus frequency. Total Harmonic Distortion(THD) gives the total harmonic content in a voltage or current waveform.Harmonic distortion are generated by power electronics loads like adjustable speed drives, switched mode power supplies, voltage regulators etc.

2.2.6.3 Inter-harmonics

Inter-harmonics are non-integer frequency components of voltage or current reference frequency. Cycloconverters, arcing devices, induction motors, and static frequency converters are the major sources of inter-harmonics. The visual flicker on CRT is one of the effects of inter-harmonics.

2.2.6.4 Voltage Notching

Notching is a recurring power quality disturbance due to the normal operation of power electronic devices such as rectifiers. Notching occurs when the dc-link current is commutated from one phase to another in a solid state rectifier as illustrated in Fig. 2.6. Subsequently, a momentary short circuit happens between two phases during this period. There will be four notches per cycle in any phase voltage waveform for a six pulse rectifier.



Figure 2.6: Voltage notching waveform

2.2.6.5 Noise

Noise is a random variation in electrical signal with broadband spectral content lower than 200 kHz as illustrated in Fig. 2.7. Noise is superimposed upon the phase current or phase voltage or signal voltage. The major producers of noise are switching power supplies, power electronic devices, arcing devices, control circuits and loads with solid state rectifiers. Noise can be reduced by using filters, line conditioners and isolation transformers.



Figure 2.7: Noise in waveform

2.2.7 Voltage Flicker

The voltage flicker is caused by modulation of the amplitude of the waveform with a frequency less than 25 Hz as illustrated in Fig.2.8. The variation in lamp intensity in normal bulb is a visual indication of flicker, which a human eye can detect. Arcing and frequent starting of an elevator motors are the major causes of flicker. DSTATCOM, filters and static VAR compensator can be used to nullify the flicker problem.



Figure 2.8: Voltage waveforms showing flicker.

2.2.8 Outage

Outage is defined as an interruption that has duration lasting in excess of one minute.

2.2.9 Frequency Deviation

It is a variation in frequency from the nominal supply frequency above/below a predetermined level, normally \pm 0.1%.

The categories of power quality variation is summarized in Table. 2.1.

| Categories | Spectral | Typical | Typical |
|-----------------------------|----------------------|-------------------|---------------|
| | Content | Duration | Magnitudes |
| 1 Transients | | | |
| 1.1. Impulsive | | | |
| 1.1.1. Voltage | > 5 kHz | $< 200 \ \mu s$ | |
| 1.1.2. Current | > 5 kHz | $< 200 \ \mu s$ | |
| 1.2. Oscillatory | | | |
| 1.2.2. Low frequency | < 500 Hz | < 30 cycles | |
| 1.2.2. Medium frequency | 300 - 2 kHz | < 3 cycles | |
| 1.2.2. High frequency | > 2 kHz | < 0.5 cycle | |
| 2 Short-Duration Variations | | | |
| 2.1. Sags | | | |
| 2.1.1. Instantaneous | | 0.5 - 30 cycles | 0.1 - 1.0 pu |
| 2.1.2. Momentary | | 30 - 120 cycles | 0.1 - 1.0 pu |
| 2.1.3. Temporary | | $2 \sec - 2 \min$ | 0.1 - 1.0 pu |
| 2.2. Swells | | | |
| 2.2.1. Instantaneous | | 0.5 - 30 cycles | 0.1 - 1.8 pu |
| 2.2.2. Momentary | | 30 - 120 cycles | 0.1 - 1.8 pu |
| 2.2.3. Temporary | | $2 \sec - 2 \min$ | 0.1 - 1.8 pu |
| 3 Long-Duration Variations | | | |
| 3.1. Over-voltages | | $> 2 \min$ | 0.1 - 1.2 pu |
| 3.2. Under-voltages | | $> 2 \min$ | 0.8 - 1.0 pu |
| 4 Interruptions | | | |
| 4.1. Momentary | | $< 2 \sec$ | 0 |
| 4.2. Temporary | | $2 \sec - 2 \min$ | 0 |
| 4.3. Long-term | | $> 2 \min$ | 0 |
| 5 Waveform Distortion | | | |
| 5.1. Voltage | 0 - 100th harmonic | steady state | 0 - 0.2 pu |
| 5.2. Current | 0 - 100th harmonic | steady state | 0 - 1 pu |
| 6 Waveform Notching | 0 - 200 kHz | steady state | |
| 7 Flicker | $< 30 \mathrm{~kHz}$ | intermittent | 0.1 - 0.07 pu |
| 8 Noise | 0 - 200 kHz | intermittent | |

 Table 2.1: Categories of power quality variation

2.3 Effects of PQ Quantities

2.3.1 Voltage dips

Voltage dips causes machine/process downtime, scrap cost, clean up costs, product quality and repair costs all contribute to make these types of problems costly to the end-user

2.3.2 Transients

Transients leads to tripping, component failure, hardware reboot required, software glitches, poor product quality

2.3.3 Harmonics

Harmonics causes transformer and neutral conductor heating leading to reduced equipment life span, audio hum, video flutter, software glitches, and power supply failure.

2.4 Sources of Power Quality Problems

- Power electronic devices
- IT and office equipments
- Arching devices
- Load switching
- Large motor starting
- Embedded generation
- Sensitive equipment
- Storm and environmental related damage.

2.5 Power Quality Standards

Power quality standards are used to define the margin in which the voltage and frequency allowed to vary. There are some other standards which limits the voltage distortion, current harmonic content, fluctuations in the voltage, and the interruption duration. There are three reasons for developing power quality standards. They are (a)defining the nominal environment, (b)defining the terminology, and (c)limit the number of power quality problems. There are mainly two sources of power quality measurement standards (Bollen 2001): the International Electro-technical Commission (IEC) and the International Electrical and Electronics Engineers (IEEE).

2.5.1 IEC Power Quality Measurement Standards

<u>IEC 61000-4-30</u>, titled - <u>Power Quality Measurement Methods</u> is a proscriptive standard. It sets out Class-A measurement methods with sufficient precision to guarantee that any two compliant instruments, when connected to the same signal, will produce the same results. It also describes Class-B instruments, which are described as producing useful results, without ensuring that their results will match any other instrument. This standards sets out methods for measuring power frequency, steady state voltage, flicker(as a reference to another standard), sags/swells characterized only by depth and duration, interruptions, unbalance, voltage harmonics(again as a reference to another standard), and mains signaling voltages.

2.5.2 IEEE Power Quality Measurement Standards

- 1. <u>IEEE 1159, titled</u> Monitoring Electric Power Quality is the principal power quality measurement standard from the *IEEE*. The latest edition has been divided into three parts: 1159.1, 1159.2, and 1159.3.
- 2. <u>IEEE 1159.1</u>, titled <u>Guide for Recorder and Data Acquisition Requirements for</u> <u>Characterization of Power Quality Events</u>. As the title implies, this standard covers both the instrumentation requirements and the post-processing event characterization requirements. It is closely aligned with *IEC* 61000-4-30, but provides far more tutorial information, and provides useful methods for interpreting power quality recordings. As for early 2005, work continues on this document. There continues to be some confusion about how to align *IEEE* and

IEC standards without infringing on the copyright requirements and standards marketing positions of either organization.

3. <u>IEEE 1159.3</u>, titled - <u>Data File Format for Power Quality Data Interchange</u>. It describes in detail the PQDIF(Power Quality Data Interchange Format) data format, which is becoming the standard file format for interchangeable power quality data.

2.5.3 Other power quality related *IEEE* standards task forces, and projects include

- IEEE Task Force P1564, titled Voltage Sag Indices
- *IEEE* 1346 titled Electric Power System compatibility with Electronic Process Equipment
- *IEEE* P1100, titled Power and Grounding Electronic Equipment, also known as the Emerald Book
- *IEEE* 1433, Power Quality Definitions
- IEEE 519, Harmonic Control in Electric Power Systems
- *IEEE* Task Force P519A, Guide for Applying Harmonic Limits on Power Systems
- *IEEE* P1547, Distributed Resources and Electric Power Systems Interconnection.

IEEE definition of Voltage Sag

A Voltage Sag (as defined by *IEEE* standard 1159 - 1995, *IEEE* recommended practice for monitoring electric power quality) is a decrease in RMS voltage at the power frequency for durations from 0.5 cycles to 1 minute, reported as the remaining voltage.

2.6 Voltage-Tolerance Requirements

The power supply of a computer, and most consumer electronics equipment normally consists of a diode rectifier along with an electronic voltage regulator (dc-dc converter). The power supply of all these low power electronic devices is similar and so is their sensitivity voltage sag. This may leads to sag-induced trip. A television will show black screen for up to few seconds; a compact disk player will reset itself and start from the beginning of the disc, or just wait for the new command.



Figure 2.9: CBEMA Curve

A process-control computer of a chemical plant is rather similar in power supply to any desktop computer. Thus they will both trip on voltage sags and interruptions. But the desktop computer's trip might lead to the loss of one hour of work (typically less), where the process-control computer's trip easily leads to a restarting procedure of 48 hours plus sometimes a very dangerous situation.



Figure 2.10: ITIC Curve

Voltage-tolerance curves have been made for different consumer electronics equipments to see the tolerance to voltage sag for different time durations. The voltagetolerance of personal computers varies over a wide range: 30-170 ms, 50 - 70% being the range containing half of the models. The first modern voltage-tolerance curve was introduced for mainframe computers. This gives voltage-tolerance requirement for a whole range of equipment. The requirement of a voltage-tolerance curves of equipment is that they should all be above the voltage-tolerance requirement in Fig. 2.9. The curve shown in Fig. 2.9 became well known when the Computer Business Equipment Manufacturers Association (CBEMA) started to use the curve as a recommendation for its members. Then it begin to known as *CBEMA Curve*. The curve was subsequently taken up in an IEEE standard and became a kind of reference for voltage tolerance as well as for severity of voltage sags. Recently a "revised CBEMA curve" has been adopted by Information Technology Industry Council(ITIC), which is the successor of CBEMA. The new curve therefore referred to as the *ITIC curve*; it is shown in Fig. 2.10.

The ITIC curve gives somewhat stronger requirements than the CBEMA curve. This is because power quality monitoring has shown that there are an alarming number of sags just below the CBEMA curve.

2.7 Sag Mitigation Techniques

- 1. Tap Changers
- 2. Custom Power Devices
 - (a) Shunt compensation (DSTATCOM)
 - (b) Series compensation (DVR)
 - (c) Combined series and shunt compensation (UPQC)

2.7.1 Custom Power Devices

Custom power devices are power electronic controllers are meant to provide high quality, reliable and uninterruptible power to the customers with sensitive loads.

The classification of compensating type custom power devices is done based on the different topologies used as discussed in Yash et al (2008). For power quality improvement the VSI bridge structure is generally used for the development of compensating type custom power devices, because of self-supporting dc voltage bus with a large dc capacitor, while the use of CSI is less reported. The current source inverter topology finds it application for the development of active filters, DSTATCOM and UPQC. The VSI topology is popular because it can be expandable to multilevel, multi-step and chain converters to enhance the performance with lower switching frequency and increased power handling capacity. In addition to this, this topology can exchange a considerable amount of real power with energy storage devices in place of the dc capacitor.

The topology can be shunt (DSTATCOM), series (SSC commercially known as DVR), or a combination of both (UPQC). The second classification is based on the number of phases, such as two-wire (single phase) and three- or four-wire three-phase systems. Both the SSC and DSTATCOM have been used to mitigate the majority the

power system disturbances such as voltage dips, sags, flicker, unbalance, and harmonics. For lower voltage sags, the load voltage magnitude can be corrected by injecting only reactive power into the system. However, for higher voltage sags, injection of active power, in addition to reactive power, is essential to correct the voltage magnitude. Both DVR and DSTATCOM are capable of generating or absorbing reactive power, but the active power injection of the device must be provided by an external energy source or energy storage system. The response time of both DVR and DSTATCOM is very short and is limited by the power electronics devices. The expected response time is about 25 ms, and which is much less than some of the traditional methods of voltage correction such as tap-changing transformers.

2.7.1.1 Shunt Compensation Method

Distribution Static Synchronous Compensator (D-STATCOM) comes under this category. D-STATCOM regulates the load voltage in shunt configuration, ie; it injects a current to compensate the load voltage variation. D-STATCOM is most widely used for power factor correction, to eliminate current based distortion and load balancing, when connected at the load terminals. It can also perform voltage regulation when connected to a distribution bus.

2.7.1.2 Series Compensation Method

The DVR is a series compensation device. It is connected before the load in series with the mains, using a matching transformer, to eliminate voltage harmonics, and to balance and regulate the terminal voltage of the load or line. The main functions of the DVR are voltage regulation, reactive power compensation, compensation for voltage sag and swell and unbalance voltage compensation (for 3-phase systems).

The shunt connected DVR, elimination of the series transformer, the utilization of rectifiers, inverters with reduced switch-count and absence of energy storage devices are the main ideas behind the different economical topologies of DVR.

2.7.1.3 Combined series and shunt compensation (UPQC)

UPQC is a combination of shunt and series active power filter filters. The dc-link storage element is shared between two VSI bridges operating as active series and active shunt compensator. It is considered as a most versatile device that can inject current in shunt and voltage in series simultaneously in a dual control mode. The functions of UPQC are reactive power compensation, voltage regulation, compensation for voltage sag/swell, unbalance compensation for current and voltage (for 3-phase systems), and neutral current compensation (for 3-phase 4-wire systems). It can eliminate negative-sequence currents. Its main drawbacks are its large cost and control complexity because of the large number of solid-state devices involved.

Two topologies of UPQC (right-shunt and left-shunt) are reported in the literature. The over all characteristics of right-shunt UPQC are superior to those of left-shunt UPQC. In addition to this UPQC connected between two different feeders is called Interline Unified Power Quality Conditioner (IUPQC) and a UPQC, without sharing active power during steady state is called UPQC-Q.

2.8 The basic elements of a DVR

Fig. 2.11 illustrates some of the basic elements of a DVR which consists of:

- 1. Converter
- 2. Filter unit
- 3. Injection transformer
- 4. dc-link and energy storage
- 5. By-pass equipment
- 6. Dis-connection equipment.

2.8.1 Converter

Converter is used to produce required voltage for compensation from fixed voltage. For dc-link energy storage VSI is used. A stiff dc voltage supply of low impedance at the input is used to energize the VSI. The output voltage of the converter is independent of the load current. The capacitor used in the VSI reduces the variations in output voltage. Graetz bridge inverter and Neutral point clamp inverter are two common inverter connections used for three phase DVR. H-bridge inverter is the common method used for single phase DVRs.


Figure 2.11: The basic elements of a DVR in a single-phase representation

Switching Devices : MOSFET and IGBT are the most common switching devices used in practice. MOSFET has got higher switching frequency and high on-resistance. The limitation is its power, voltage and current rating. IGBT is a newer device, which is introduced in early 1980s. IGBT has better power, voltage and current rating compared to MOSFET. IGBTs are used in medium power applications. The frequency of operation is less compared to MOSFET. GTO and IGCT are the other two switching device that can be used for the converter implementation. GTO can be turned off by applying negative current pulse at the gate. The voltage rating of GTO is very high compared to MOSFET and IGBT. The major drawback of GTO is it cannot meet the dynamic requirement of DVR. IGCT is very recent device. It has got better performance. IGCT can be used to make larger power rated converters.

2.8.2 Filter unit

The nonlinear characteristics of the switches makes the inverter output distorted. The inverter output of the DVR is distorted and contains lots of harmonics due to the nonlinear characteristics of the semiconductor switches used. The filter unit is used to filter higher-order switching harmonics generated by the PWM VSI and improve the quality of the energy supply. Inverter side and line side filtering are the basic types of filtering schemes.

The advantage of the inverter side filter are (a)it prevents the higher order harmonic currents(due to VSI) to penetrate into the series injection transformers, since it is closer to the harmonic source and (b)the components are rated at low voltage, since the filter is located at low voltage side. The disadvantages are that the filter inductor causes voltage drop and phase(angle) shift in the (fundamental component of) voltage injected (inverter output). This can affect the control scheme of the DVR.

The location of the filter on the high voltage side(line side filter) overcomes the drawbacks, i.e., the filter voltage drop and phase shift problem don't disturb this system(the leakage reactance of the transformer can be used as the filter inductor). But it results in higher rating of the transformers as high frequency currents can flow through the windings. In both filtering schemes, filter capacitor will cause increased inverter ratings. The increased filter capacitor provides better harmonic attenuation but the rating of the inverter is related with the capacitor value.

2.8.3 Injection transformer

The primary functions of the transformer is to boost the voltage generated by the VSI and to isolate and couple the DVR to the distribution system. The maximum effectiveness and reliability can only be ensured by proper selection of the electrical parameters of the injection transformer. The turns ratio, MVA rating, primary winding voltage and current ratings, and the short-circuit impedance values of transformers are required for proper interconnection of the injection transformer into the DVR.

2.8.4 dc-link and energy storage

The required ac voltage to be injected to the grid is synthesized from a stiff dclink. The energy storage is required to provide active power injection to the load to restore the supply voltages during deep voltage dips. Lead-acid batteries, Super Conducting Magnetic Energy Storage (SMES), flywheel or Super-capacitors can be used for energy storage. The depth and duration of the sag decides the capacity of the energy storage required for the DVR. Batteries of high voltage configuration is a good choice for energy storage. The shortcoming with batteries are its short lifetime and it requirement of a battery management system, which is expensive. Ultra-capacitors are good alternative for lead acid batteries. Voltage range of ultra-capacitors are wider compared to batteries. Specific energy density of ultra-capacitors are lower than batteries, but it has got higher power density compared to batteries. This makes it ideal for short duration pulses of few seconds. Ultra-capacitors got longer life time and short charge time.

2.8.5 By-pass equipment

Since the DVR is a series connected device, any fault current that occurs due to a fault in the downstream will flow through the inverter circuit. The power electronic components in the inverter circuit are normally rated to the load current as they are expensive to be over rated. Therefore to protect the inverter from high currents, a by-pass switch (crowbar circuit) is incorporated to by-pass the the load current during faults, overload and service.

Basically the crowbar circuit senses the current flowing in the distribution circuit and if it is beyond the inverter current rating the circuit bypasses the DVR circuit components (dc Source, inverter and the filter) thus eliminating high currents flowing through the inverter side. When the supply current is in normal condition the crowbar circuit will become inactive and is illustrated in Fig. 2.11 as a mechanical bypass and a thyristor bypass.

2.8.6 Disconnection equipment

Disconnection equipment is used to disconnect the DVR completely for service or repair.

2.9 DVR Types

2.9.1 Based on Location of the DVR

The DVRs intended location is either at the MV distribution level or at the LV-level close to a LV customer. This section discusses the different perspectives with the two alternatives.

A simplified model of the DVR is illustrated in Fig. 2.12 and can help to evaluate the best location of a DVR. The DVR can be represented as an ideal voltage source (V_{conv}) with an inserted reactive element (X_{DVR}) , which mainly represents the reactive elements in the injection transformers and line filters, and an inserted resistive element (R_{DVR}) , which represents the losses in the DVR. The size of the inserted impedance is closely related to the DVR voltage rating (V_{DVR}) and the DVR power rating (S_{DVR}) according to:

$$X_{DVR} = \frac{V_{DVR}^2}{S_{DVR}} v_{DVR,X}$$
(2.1)

$$R_{DVR} = \frac{V_{DVR}^2}{S_{DVR}} v_{DVR,R}$$
(2.2)

$$Z_{DVR} = \frac{V_{DVR}^2}{S_{DVR}} v_{DVR,Z}.$$
(2.3)

(2.4)

 $v_{DVR,Z}$ depends on the type of transformer used, the line-filter, losses in the VSC etc. A DVR with high injection capability (high V_{DVR}) and the ability only to protect

a small load (low S_{DVR}) has a large equivalent DVR impedance (Z_{DVR}).

Going from a LV level DVR to a higher voltage level DVR the pu value of the reactance $(v_{DVR,X})$ tends to increase, and the pu value resistance $(v_{DVR,R})$ tends to decrease.

A high resistive part increases the energy, which should be dissipated from the DVR and the costs associated with the losses. A high total inserted DVR impedance increases the potential load voltage distortion and load voltage fluctuations if the load is non-linear and/or has a fluctuating load behavior.



Figure 2.12: Single-phase simplified model of the DVR

2.9.2 The DVR applied to the MV-level

Connected to the MV-level, the DVR protects a large consumer or a group of consumers. The insertion of a DVR in the medium voltage distribution system is illustrated in Fig. 2.13. The supply impedance for LV load increases slightly by inserting large DVR at the MV-level. Assuming an infinite bus-bar at the 66 kV level, the impedance for a LV load consists of the sum of impedances from the 66/11 kV transformer, cables and overhead lines at the 11 kV level, the 11/0.4 kV distribution transformer and finally LV cables to the LV load. The impedance and the increase in impedance by inserting a DVR can be expressed as:

$$Z_{s,b} = Z_{(11/66)} + Z_{line,11} + Z_{(11/0.4)}$$
(2.5)

$$Z_{s,a} = Z_{DVR} + Z_{s,b} \tag{2.6}$$

$$Z_{i,p} = \frac{Z_{DVR}}{Z_{s,b}} 100\%$$
(2.7)



Figure 2.13: DVR located at the medium voltage distribution system

For a LV load the dominating impedance is most likely the LV line impedance $(Z_{line,0.4})$ and the impedance of the distribution transformer $(Z_{11/0.4})$. Protecting a large MV load close to the DVR, the increase in impedance experienced by the load can be significant. Inserting one high rated DVR at the MV-level has certain advantages:

- The impedance seen by a LV load by inserting a large DVR at the MV level is relatively small.
- The MV distribution systems in Denmark are operated as a three wire system with isolated or inductor grounded system. In such a system injection of positive and negative sequence system is sufficient and a more simple DVR topology and hardware can be used.
- Looking from costs per MVA view point it is recommended to install large central DVR at the medium voltage level instead of decentralized low voltage units.

Some of the disadvantages can be summarized to:

• Protecting a large load may require a medium voltage DVR otherwise the losses in the DVR will be too high.

- During ground faults in the MV system the phase to ground voltages can increase with $\sqrt{3}$, and a higher isolation level of the injection transformers must be ensured.
- A part of the DVR rating may be utilized on loads, which do not require a supreme voltage quality.
- The DVR is connected to a voltage level, which requires a high isolation level and the short circuit level is high.

2.9.3 The DVR applied at the LV-level

The insertion of a DVR at the low voltage four-wire 400 V level is illustrated in Fig.2.14. The increase in impedance by insertion of a small rated DVR can be significant for the load to be protected from voltage dips. Thereby, the percent change in the impedance $(Z_{i,p})$ in (2.7) can be increased by several hundred percent. Inserting a DVR at LV-level has certain advantages:



Figure 2.14: DVR located at the low voltage distribution system

• The DVR can be installed exactly at the location where the voltage sag sensitive load is connected.

- Since most of the customers have access to LV-level, the placing of the LV DVR can be either from customer side or from the utility side.
- Since distribution transformer decreases the short-circuit level, the DVR is easier to protect

The disadvantages with a LV solution are:

- The insertion of the DVR causes significant increase in the impedance. This may affect the site short circuit level and protection. Distortion in the load voltage and variation in the load can be expected as a result of non-linear and time varying load currents.
- Voltage sags containing zero sequence voltage component can be seen. DVR has to generate positive, negative and zero sequence components to compensate the loads connected between neutral and phase.

2.9.4 Based on DVR topologies

In this chapter the main topologies for DVRs are discussed with focus on methods to connect the DVR to the grid, converter topologies suited for DVRs and methods to ensure active power during the voltage dip mitigation. The section includes a survey of the different topologies for DVRs, which also have been discussed by Aschcraft et al (1996) and Nielsen et al (2001).

2.9.5 Converter connection

The DVR is going to inject a voltage in series with the supply, which requires either galvanic isolation to the VSI or letting the VSI float at the potential of the supply voltages. Two different approaches are considered here, referred to as a transformer connected converter or a direct connected converter.

2.9.5.1 Transformer connected converter

Using a low frequency transformer (50/60 Hz) to transfer the VSI voltages to series injected voltages is the most common method, which is illustrated in Fig. 2.15(a). Sree et al (2000) has tried to replace the low frequency transformer with a high frequency

transformer link together with a floating cyclo-converter based DVR. Ensuring the galvanic isolation with a low frequency transformer the following advantages can be obtained:

- The transformer ratio can be chosen rather arbitrarily, thereby the transformer can be scaled to a standard industrial converter voltage. Either up or down in voltage to achieve the best performance.
- The transformer can be used to ensure the DVRs Basic Insulation Level (BIL).
- The transformer can be used as a part of an important line-filter. Either as the first inductance close to the converter or as an inductor close to the load in a LCL-filter configuration.
- A relative simple converter topology with six active switches can be used to inject the voltages into the grid.
- One dc-link is sufficient, which simplify the dc-link, charging circuit and the dc-link voltage control.

Some of the disadvantages, when using injection transformers are:

- The series injection transformers are not of the shell transformers, because the design differs from mass produced shunt transformers and the voltage rating varies with the required injected voltages.
- The transformers increase losses, have a non-linear behavior and can be a limiting factor regarding the bandwidth of the DVR system.
- The low frequency injection transformers are bulky with high cost, weight and volume.

2.9.5.2 Directly connected converter

Series injection with transformer-less converters has been reported for VAr compensator. DVRs using a directly connected converter are stated as an idea and the concept is used by Sree et al (2000). Technically, direct connection is the best suited for series devices, which only exchanges reactive power with the grid, because the transfer of



(a)



(b)

Figure 2.15: Different converter connection methods. a) DVR including an injection transformer to ensure galvanic isolation between the supply and VSI. b) transformer-less DVR, directly connected to the grid and a separate dc capacitor for each phase leg.

power require charging of three separate dc-links. Fig. 2.15(b) shows a directly connected DVR converter and the advantages with a directly connected DVR converter are:

• The performance is expected to be improved, because the bandwidth is not

decreased by the transformer and the non-linear effects and voltage drop caused by the transformers are removed.

• The bulky transformers can be avoided. A compact DVR solution can be developed with low volume, low weight etc.

Some of the disadvantages are:

- Protection of the power electronics is more complicated and BIL must be ensured more actively.
- The converter topology has to be more complex and a high isolation to ground has to be ensured.
- The converter topologies are more complex and a higher number of components is expected to be used.

2.9.6 Topologies to have active power access during voltage dips

DVR injects the voltage required to restore the voltage to reference value during a voltage sag. This is achieved by exchanging reactive and/or active power with the system. For active power exchange the DVR needs an energy storage. Based on the energy exchange two topologies are discussed here, stored energy based and without any significant energy storage.

The stored energy can be delivered from different kinds of energy storage systems such as batteries, double-layer-capacitors, super-capacitors, flywheel storage or SMES. In the no storage DVR concept, the DVR has practically no energy storage(Weissbach et al 1999) and the energy is taken from the remaining supply voltage during the voltage dip. The four system topologies, which are presented are:

- Topologies with stored energy
 - Constant dc-link voltage.
 - Variable dc-link voltage.
- Topologies with power from the supply

- Supply side connected passive shunt converter.
- Load side shunt connected passive shunt converter.

Topologies with stored energy

In this case all the energy is stored before the voltage dip and a very small scale converter is expected to be used to re-charge the energy storage. Two different control/hardware methods are popular, which are a DVR operating with a constant dc-link voltage and a DVR operating with a variable dc-link voltage.

Constant dc-link voltage

A DVR with constant dc-link voltage, illustrated in Fig. 2.16 is expected to have superior performance and an effective utilization of the energy storage. An additional converter is expected to convert energy from the main storage to a small dc-link and thereby control and stabilize the dc-link voltage. The DVR with a constant voltage is here considered to be a reference topology by which the other DVR topologies are evaluated. It offers a constant dc-link voltage at all times and does not increase the current drawn from the supply. Power taken from the grid is reduced according to the dip.

Variable dc-link voltage

A DVR with variable dc-link voltage illustrated in Fig. 2.17 offers benefits in simplicity due to only one high rated converter and only dc-link capacitors as the only storage. The voltage injection capacity depends on the actual level of the dc-link voltage, and energy saving control strategies are urgent to fully utilize the energy storage system. The energy content in the storage can be calculated as:

$$E_{st} = \frac{1}{2} C_{dc} V_{dc-r}^2.$$
 (2.8)

Where E_{st} is the required storage, C_{dc} is the dc link capacitance and V_{dc-r} is the rated dc-link voltage. The dc-link voltage can most likely only to be utilized down to a certain dc-link voltage level and the actual energy storage can be estimated and given by (2.9):

$$\Delta E = C_{dc} (V_{dc-b}^2 - V_{dc-e}^2).$$
(2.9)



Figure 2.16: DVR topology with power from stored energy and operating with constant dc-link voltage



Figure 2.17: DVR topology with power from stored energy and operating with variable dc-link voltage.

Where V_{dc-b} is the dc-link voltage at the beginning and V_{dc-e} is the dc-link voltage at the end of sag. At severe dips a smaller portion of the stored energy, ΔE can be effectively utilized and the ability to restore the supply voltage decays.

Topologies with power from the supply

Taking power from the remaining supply voltage has the disadvantage of an increase in the supply current. The advantages are cost saving of the energy storage and the ability to compensate long duration voltage dips.

Taking power from the grid can have a negative influence on the neighboring upstream loads, because the DVR protects its downstream loads by taking more current from the supply, which can lead to an even more severe voltage dip for upstream loads.

Topologies for DVR using power from the grid can generally be characterized with the location of the shunt converter for example at the supply side of the series converter or at the load side of the series converter. Both passive and active shunt converters can be used.

Supply side connected passive converter: The supply side connected passiveconverter illustrated in Fig. 2.18. The shunt current and dc-link voltage are poorly controllable and at non-symmetrical voltage dip the current drawn by the shunt converter will be very uneven distributed between the phases. The dc-link level is proportional to the voltage dip depth and at severe voltage dips the required voltage injection is high, but the dc-voltage can here be expected to be low according to (2.10) and (2.11)

$$v_{dc} \cong \sqrt{2} |\bar{v}_s| = \sqrt{2} |\bar{v}_{dip}| \tag{2.10}$$

$$\bar{v}_{DVR} = 1 - \bar{v}_{dip} \tag{2.11}$$

where v_{dc} is the dc-link voltage, \bar{v}_s is the supply voltage \bar{v}_{DVR} is the voltage across the DVR and \bar{v}_{dip} is the voltage dip in the supply.

In the case of a voltage dip the power is not absorbed by the shunt converter until the dc-link voltage have dropped below a certain dip level. The following equations (2.12) and (2.13) express the maximum voltage for the shunt and series converter:

$$\left|\bar{v}_{sh}\right| = 1\tag{2.12}$$

$$|\bar{v}_{se}| = |1 - \bar{v}_{dip}|$$
 (2.13)

where v_{se} is the voltage rating of the series converter and v_{sh} is the voltage rating



Figure 2.18: DVR topology with energy from the grid and with a shunt converter at the supply side of the series converter.

of the shunt converter. The concept of a passive shunt converter is relatively cheap, but the coherence between the dc-link voltage and the dip size is unfavorably and the solution is expected to be unqualified for severe voltage dip compensation in general.

Load side connected passive converter A DVR with a load side connected passive converter, illustrated in Fig. 2.19, can basically keep the dc-link voltage almost constant, because the load voltage is controlled by the DVR itself. One disadvantage is the currents handled by the series converter increase significantly during a voltage dip and the load voltages can be more distorted because of the non-linear currents drawn by the passive shunt converter, which have to flow through the series converter. The DC-link voltage is equal to:

$$v_{dc} \cong \sqrt{2} |\bar{v}_{load}| = \sqrt{2} |(\bar{v}_{dip} + \bar{v}_{DVR})|.$$
 (2.14)

The voltage rating of the converters depends on the injected voltage capability and the restored load voltage level according to equations (2.15) and (2.16)

$$|\bar{v}_{se}| = |1 - \bar{v}_{dip}|$$
 (2.15)

$$\left|\bar{v}_{sh}\right| = 1\tag{2.16}$$

where v_{se} is the voltage rating of the series converter and v_{sh} is the voltage rating of the shunt converter. The current rating of the shunt converter is equal to the



Figure 2.19: DVR topology with energy from the grid and with the DVR operating with a shunt converter at the load side of the series converter.

supply side topology. At severe dips very high converter current ratings are necessary according to equations (2.17) and (2.18).

$$|\bar{i}_{series}| = \frac{1}{|\bar{v}_{dip}|} \tag{2.17}$$

$$|\bar{i}_{shunt}| = |1 - \bar{v}_{dip}| \tag{2.18}$$

where i_{se} is the current rating of the series converter and i_{sh} is the current rating of the shunt converter.

A DVR with this circuit topology, seems to be a very effective solution, the dc-link can be held relatively constant. In the case of non-symmetrical voltage dip the current can still be taken equally from each phase.

2.10 Conclusion

Power quality issues with concentration on voltage quality issues has been carried out in this chapter. Different DVR topologies have been discussed based on injection transformer, converter topologies and based on active power exchange. Out of all voltage related power quality problems, voltage sag is the most severe and frequent problem. Voltage sag can even cause the plant shut down. The major causes of voltage sag are faults and sudden switching of large motors. The depth and shape of the sag depends on the type of fault and type of load. The voltage sag can be compensated with shunt and series compensation. Series compensation is identified to be the cost effective solution for sag compensation. Different DVR topologies are discussed. If deep voltage sag is rare in a grid DVR topology without any significant energy storage is preferable. Load side connected passive converter topology is a good alternative, but the installed converter capacity will be high. DVR filter connection types are discussed in detail. The protection of the DVR is important. The DVR must be protected against downstream short circuit.

Chapter 3

DVR Based on High-Frequency Link Direct ac-ac Converter

3.1 Introduction

Conventional DVR topologies uses indirect power converter consisting of ac-dc converter, dc-link, dc-ac inverter followed by a line frequency isolation transformer. Transformers do a vital role in electric power distribution/conversion systems in order to perform many functions such as isolation, voltage transformation, noise decoupling etc.

Line frequency transformers (50Hz and 60Hz) are one of the heaviest, bulkiest and most expensive part in an electrical conversion system due to the bulky iron cores and heavy copper windings in the composition. Saturation flux density of the material used for the core maximum allowable temperature rise in the windings and core is the deciding factor for the size and weight of the transformer. Saturation flux density is inversely proportional to frequency and hence the transformer flux utilization can be increased by increasing the frequency of operation. This further reduces the transformer size as explained by McMurray (1970).

Hence, increasing the frequency allows higher utilization of the magnetic core. This further can lead to large reduction in size and weight of the transformer. This also helps to reduce the size and weight of passive components such as filter capacitances and inductances used for filtering and temporary energy storage purpose.

Utilization of power electronic converter along with a high frequency transformer gives overall size and cost advantages for a high frequency link ac-ac converter over a conventional transformer.

Small size electronic transformer using high frequency-link transformer has been widely discussed in McMurray (1970) and Han Ju Cha et al. (2003). The ferrite core used for high-frequency transformer is cheap and easily available. This helped in the implementation of high-frequency link power transformation. By operating the link at a high frequency, the system can be made compact because of large reduction in size and the weight of the transformers and the passive components needed for filtering and temporary energy storage functions. High-frequency operation also speeds up the system response and if the frequency is above the audio range, reduces acoustic noise. High-frequency link power converters are receiving increasing attention as an alternative to more conventional dc-link power conversion systems. High-frequency power conversion has been employed very successfully in dc-dc converters. Their enormous success has been demonstrated the benefits and to some extent the difficulties of working at high frequency. Research on high frequency link dc-ac converters, the high-frequency link ac-dc converters (switching mode rectifiers), and the high frequency link dc-ac inverters has been carried out in Oliveira et al. (2007). A number of high-frequency link systems have also been proposed for dc-dc and ac-ac power conversion. Research on ac-ac converters were mainly limited to non-isolated ac-ac converters. Direct matrix converter which is discussed in Rivera et al (2011), the pulse width modulated ac choppers seen in Wang et al. (2011), and the soft switched ac-link buck-boost ac-ac converter discussed in Toliyat et al (2008) have the features of single or two stages of power conversion, low voltage transmission ratio, no need of intermediate dc-energy storage components etc. The research on ac-ac converter is mainly limited to the thyristor phase controlled cycloconverters as discussed in Bose (2006) and matrix converters as seen in Casadei et al (2007) without electrical isolation.

Ac-ac converter with high frequency isolation are a leading research content of power electronics, and a key technical foundation on new type Power Electronic Transformers(PET), regulated sinusoidal ac power supplies and ac regulators. A few three-phase PETs have been reported in recent literature Manjrekar et al. (2000) and Han Ju Cha et al. (2003)). They need either too many ac-dc links, large bulky magnetic components or dc-link electrolytic capacitors. Thus they result in rather cumbersome solution and all the output loads are assumed to be balanced. The high frequency ac link ac-ac converter was first proposed in Oliveira et al. (2007). It has two cycloconverter with a high-frequency ac-link in between them. Kang et al (1999) and

Sakamoto et al (1988) has proposed H-bridge and push-pull circuits respectively.

A new DVR topology with a three phase high frequency link matrix converter is proposed in this work. In this approach, the three phase ac source is chopped to 50% duty square wave pulses and transferred through single-phase high frequency transformer and finally established as a fixed frequency utility voltage. The advantage of the proposed topology are:

- 1. Flexible voltage transfer ratio to meet several standard utility voltages
- 2. Electric galvanic isolation between the load and the DVR
- 3. Full utilization of input voltage for dc-link stage and near symmetric square wave pulse trains to the high frequency transformer regardless of the supply frequency.
- 4. High power density due to minimization of magnetic components and bulky dc link capacitors.
- 5. Controllable displacement power factor at output utility.
- 6. Lower total harmonic distortion of the input and output currents.

The proposed DVR topology is shown in Fig.3.1. The DVR power circuit topology has two power conversion stages, a line side three-phase to single phase matrix converter and load side single-phase to three-phase matrix converter with a high frequency transformer isolation in between. The line side converter chops the input utility source voltage to high frequency 50% duty square wave pulse, which is transferred to load side converter through a small and efficient high frequency transformer. The load side converter is divided into full bridge active rectifier and conventional VSI structure. This converter is similar to the ac-dc-ac converter without dc capacitors as explained in Kim et al (2000). The transformed high frequency square pulse signal is rectified by active rectifier and establishes a desired magnitude of fluctuated dc link voltage V_{dc} by proper selection of transformer turns ratio. The well known SPWM is chosen for modulation of the inverter on the load side.



Figure 3.1: Proposed converter topology for the DVR.

3.1.1 3ϕ to 1ϕ Direct Matrix Converter Modulation

This line side converter part is used to synthesize the high-frequency ac voltage denoted as V_p from the balanced three-phase input voltage and, then transfer single-phase highfrequency square wave pulses to the line side single-phase to three-phase converter part through an isolated single phase HF transformer.

The PWM scheme explained in Wei et al (2001) is expanded for the line side converter part. It is assumed that the input source voltages are balanced and described by (3.1)-(3.3).

$$V_{sA} = V_{im} \cos\theta_a = V_{im} \cos(\omega_{in} t) \tag{3.1}$$

$$V_{sB} = V_{im} \cos\theta_b = V_{im} \cos(\omega_{in} t - 2\pi/3)$$
(3.2)

$$V_{sC} = V_{im} \cos\theta_c = V_{im} \cos(\omega_{in} t + 2\pi/3)$$
(3.3)

where ω_{in} is the input angular frequency. θ_a , θ_b and θ_c are phase angle of phase voltages a, b and c respectively

Between any successive zero crossing of the input phase voltages, only one of the three phases input voltages has the maximum absolute value and the other two phase voltages have opposite polarity. Considering mode 1 as shown in Fig. 3.2 phase *a* has maximum positive voltage and the other two phases *b* and *c* have negative value and it can be shown that $|V_{sA}| = |V_{sB}| + |V_{sC}|$.



Figure 3.2: Six modes of input phase voltages

During mode-1, switch S_{ap} remains turned on and switches S_{bn} , S_{cn} are modulated within one switching period T_S . In order to satisfy full utilization of input voltage and to get unity power factor at input source side, the duty ratios d_b , d_c of switches S_{bn} and S_{cn} are given as

$$d_b = \frac{|\cos\theta_b|}{|\cos\theta_a|}, d_c = \frac{|\cos\theta_c|}{|\cos\theta_a|}$$
(3.4)

| | Duty | Positive p | oulse | Negative pulse | | |
|------|-------|-------------------|----------|-------------------|----------|-----------|
| Mode | | Turn on | V_p | Turn on | V_p | V_{dc} |
| | ratio | SW pair | | SW pair | | |
| 1 | d_b | $S_{ap} - S_{bn}$ | V_{ab} | $S_{an} - S_{bp}$ | V_{ba} | nV_{ab} |
| | d_c | $S_{ap} - S_{cn}$ | V_{ac} | $S_{an} - S_{cp}$ | V_{ca} | nV_{ac} |
| 2 | d_a | $S_{cn} - S_{ap}$ | V_{ac} | $S_{cp} - S_{an}$ | V_{ca} | nV_{ac} |
| | d_b | $S_{cn} - S_{bp}$ | V_{bc} | $S_{cp} - S_{bn}$ | V_{cb} | nV_{bc} |
| 3 | d_c | $S_{bp} - S_{cn}$ | V_{bc} | $S_{bn} - S_{cp}$ | V_{cb} | nV_{bc} |
| | d_a | $S_{bp} - S_{an}$ | V_{ba} | $S_{bn} - S_{ap}$ | V_{ab} | nV_{ba} |
| 4 | d_b | $S_{an} - S_{bp}$ | V_{ba} | $S_{ap} - S_{bn}$ | V_{ab} | nV_{ba} |
| | d_c | $S_{an} - S_{cp}$ | V_{ca} | $S_{ap} - S_{cn}$ | V_{ac} | nV_{ca} |
| 5 | d_a | $S_{cp} - S_{an}$ | V_{ca} | $S_{cn} - S_{ap}$ | V_{ac} | nV_{ca} |
| | d_b | $S_{cp} - S_{bn}$ | V_{cb} | $S_{cn} - S_{bp}$ | V_{bc} | nV_{cb} |
| 6 | d_c | $S_{bn} - S_{cp}$ | V_{cb} | $S_{bp} - S_{cn}$ | V_{bc} | nV_{cb} |
| | d_a | $S_{bn} - S_{ap}$ | V_{ab} | $S_{bp} - S_{an}$ | V_{ba} | nV_{ab} |

Table 3.1: Switch states and corresponding voltage V_P and V_{dc} according to mode of input phase voltages.

(Where $V_{ab} = V_{sA} - V_{sB}$, $V_{ba} = -V_{ab}$, $V_{bc} = V_{sB} - V_{sC}$, $V_{cb} = -V_{cb}$, $V_{ca} = V_{sC} - V_{sA}$, $V_{ac} = -V_{ca}$, $d_a = |\cos\theta_a|/\cos\theta_{max}$, $d_b = |\cos\theta_b|/\cos\theta_{max}$, $d_c = |\cos\theta_c|/\cos\theta_{max}$ $\cos\theta_{max} = max(|\cos\theta_a|, |\cos\theta_b|, |\cos\theta_c|))$

The same way the duty ratios for all the six modes can be derived. The dc-link voltage of the loadside converter is given by

$$V_{dc} = n(d_b(V_{sA} - V_{sB}) + d_c(V_{sA} - V_{sC}))$$
(3.5)

where n is the transformer turn ratio $n = N_{sec}/N_{prim}$. By substituting (3.1)- (3.3) and (3.4) into (3.5) with trigonometric transformation, V_{dc} can be averaged within a switching period T_S and is given by

$$V_{dc} = \frac{3n.V_{im}}{2|\cos\theta_a|} \tag{3.6}$$

The switching states of the bidirectional switches and corresponding voltage V_P at

the primary side of the HF transformer and the voltage at the dc-link, V_{dc} for different modes are summarized in Table 3.1.

Expanded view of Mode-1 operation for a excessively large switching time, T_S is shown in Fig. 3.3. In this case primary winding is given two square-wave pulses during each mode. V_{ab} with a duty cycle of d_b is used to synthesize the dc-link voltage at the beginning of each duty cycle T_S .

A positive dc-link pulse of magnitude V_{ab} is generated by operating bidirectional switch S_{ap} , connected to positive side and S_{bn} , connected to negative side with a duty ratio d_b at the beginning of every switching cycle. During d_bT_S the current is flowing from phase a into phase b.

A positive dc-link pulse of magnitude V_{ac} is generated by operating bidirectional switch S_{ap} , connected to positive side and S_{cn} , connected to negative side with a duty ratio d_c at the end of every switching cycle. During $d_c T_s$ the current is flowing from phase *a* into phase *c*. The flux in the HF transformer is balanced by applying a negative voltage pulse in the next switching period.

Negative pulse V_{ba} is created by turning on switches S_{an} and S_{bp} with a duty cycle d_b and negative pulse V_{ca} is created by turning on switches S_{an} and S_{cp} with a duty cycle d_c . The alternative positive and negative pulse train of 50% duty cycle is repeated as shown in Fig. 3.3. The HF transformer is used to step up/down the primary voltage V_P . It also provide isolation between the input and output. On the secondary side of the HF transformer uncontrolled diode bridge rectifier is used to get a fluctuated dc-link voltage V_{dc} as shown in Fig. 3.3.

The PWM method is chosen synchronous or asynchronous depending on the source frequency for source side converter control. It is decided using the modulation ratio given by

$$m_f = \frac{f_{sp}}{f_i} \tag{3.7}$$

Where f_{sp} is the switching frequency in Hz, and f_i is source frequency of source side converter in Hz. If the value of m_f is small the full utilization of the input voltage is possible only if the source side converter is synchronized to the source. This also improves the current waveform. Since the whole range input phase is divided into six modes, the value of m_f should be a multiple of six. This can distribute square wave pulse train to be quarter wave symmetric about each center of modes and maintain the magnetic flux balance of the HF transformer.



Figure 3.3: PWM pattern generation (a) duty cycle in input phase voltage (b) 50% duty square wave in the primary voltage V_P (c) fluctuated dc-link voltage V_{dc}

3.1.2 Load side single-phase to three-phase converter.

This converter resembles the ac-dc-ac converter without dc capacitors (Kim et al 2000). The rectifier stage is used to rectify the 50% square wave V_s into fluctuated dc-link voltage V_{dc} . The rectifier stage consists of four diodes in full bridge configuration. The diodes can be replaced with IGBT switches if bidirectional power flow is required. The rectified dc voltage is then converted to sinusoidal ac voltage of required magnitude and frequency using three single phase VSI. SPWM technique is used for the modulation of VSI.

3.2 Controller for Single-Phase Inverters

Since the voltage sag is normally accompanied with a phase shift, both magnitude and phase has to be corrected. The error between a random phase angle and the supply voltage phase angle is regulated to zero to get the phase angle information. Therefore the reference waveform tracks the supply voltage waveform and are synchronized at steady state. The controller for single phase VSI is shown in Figure. 3.4.

The reference phase angle is used to generate the reference voltage waveform. The compensation voltage to be injected is the difference of the reference voltage and the supply voltage.



Figure 3.4: Simplified control block diagram for the single phase VSI

The first stage in the control block diagram is used to get the phase angle of the supply voltage. It consists of a Zero Crossing Detector (ZCD), limitter and resettable integrator as shown in Fig. 3.5.

The magnitude and frequency information of the supply voltage is obtained from

the supply voltage measurement. Since the phase angle of the supply varies between 0 rad to 2π rad, the phase angle waveform of the supply voltage (A_{meas}) is obtained using an integrator as shown in Fig.3.5. The reference phase angle is generated in the next step. Since the reference angle varies from 0 rad to 2π rad, the reference phase angle should reset once it reaches 2π rad. This is done using a comparator and a resettable integrator. The supply voltage, the ZCD output and the corresponding



Figure 3.5: Stage-1 implementation



angle measured using stage-2 is shown in Fig. 3.6

Figure 3.6: Supply voltage and corresponding angle measured using stage-1

The stage-2 is used to find the reference phase angle. The detailed description of the stage is shown in Fig. 3.7. A random phase angle waveform of frequency 50Hz is created first. This random phase angle waveform is then compared with supply phase angle waveform to produce the error. The angle error is regulated to zero using a PI controller.



Figure 3.7: Stage-2 implementation

By adjusting angular frequency (the gradient) of the randomly generated reference phase angle waveform, the reference phase angle is synchronized with the supply phase angle measured. The synchronisation of the random generated phase angle with the reference angle is shown in Fig. 3.8, corresponding voltage synchronisation of generated voltage waveform with supply voltage is shown in Fig.3.9.



Figure 3.8: Synchronisation of generated angle with reference angle using stage-2

The Stage-3 is used to generate reference voltage waveform from the reference phase angle waveform with nominal supply voltage magnitude. Stage-3 implementation is shown in Fig.3.10.

The reference voltage waveform generated using stage-3 and its corresponding reference angle waveform is shown in Fig.3.11



Figure 3.9: Synchronisation of generated voltage with reference voltage using stage-2



Figure 3.10: Stage-3 implementation



Figure 3.11: Generated reference voltage waveform and the corresponding phase angle in stage-3

The compensation voltage to be injected is calculated in Stage-4. The difference of reference voltage and the supply voltage gives the compensation voltage. If there is no sag and there is no phase shift in the supply voltage, the compensating voltage magnitude will be zero. The compensating voltage will have a non-zero value incase there is voltage sag. The shape and magnitude of the compensation voltage depends on the type of sag.

Stage-5 generate the PWM pulses for the power electronic switches used in the VSI. The PWM pulses are generated by comparing the control voltage with triangular carrier voltage of respective magnitude and frequency.

3.3 Conclusion

The design and control of the proposed DVR is discussed in this chapter. The modulation strategy used for the primary side three phase to single phase converter is explained. By operating the isolation transformer at higher frequency the size and weight can be reduced by increasing the flux utilization in the core in addition to give flexible voltage transfer ratio. The input ac voltage is modulated such a way that dc-link voltage is made up of the peak magnitudes of the three phase input voltages.Normally the voltage sag is accompanied with a phase shift. Therefor both magnitude and phase has to be corrected. Here the phase angle is regulated to get the correct phase angle information. From the phase angle information the magnitude of voltage to be compensated is calculated. By operating at a higher frequency the filtering is made simpler. Further the filtering components capacitor and inductor size can be reduced

Chapter 4

Simulation Results

4.1 Introduction

The simulation of the proposed DVR is carried out using the industry standard power system simulation package PSACD/EMTDC. The performance such as maximum compensation range and fast dynamic response of the DVR is analyzed. The effects of different types of faults and loads in the performance of the DVR is observed. The different types of voltage sags are created by applying fault at respective phases. The fault resistance is varied to get different levels of sag voltages.

4.2 DVR Parameters Used in Simulation

The DVR parameters used for the simulation are given below.

4.2.1 Input Filter

Switching of power electronic switches generates large number of switching harmonics, which is being injected to the grid. These unwanted electric signals will affect the other electronic systems. Switching harmonics are centered around the switching frequency. A filter must be added at the power input of the power converter to reduce the effect of harmonics. Since the lower order harmonics magnitudes are relatively smaller, a LPF is used to filter the switching harmonics. A three phase LC filter is shown in Fig.4.1. Since the filter can protect the converter and the load from the transients in the supply voltage, the reliability of the system will be improved. The current drawn from the supply become smooth by adding input filter at the input side. While designing the input, the following conditions has to be taken care:

• The cut-off frequency of the filter should be much lower than the switching frequency such that the resonant frequency

$$\omega_0^2 = \frac{1}{Li.Ci} = 2\pi.f_0 \tag{4.1}$$

where L_i and C_i are inductance and capacitance values of the input filter.

- Choose the values of capacitor and inductor such that the volume and weight of the filter is minimized.
- Provide maximum voltage transfer ratio by minimizing the voltage drop across the filter inductance.

There is chances of frequency components in the input current close to the resonant frequency of the LPF at some particular operating points. It is advisable to connect resistance parallel to the filter inductance to incorporate damping as shown in Fig. 4.1 and it is discussed by Wheeler et al (1997). The value of the damping resistor should be smaller than the the inductive reactance at cut-off frequency as explained by ?.

$$R_d \le 2\pi f_c. L_i \tag{4.2}$$

The transfer function of the input filter can be derived as 4.3

$$F_i(s) = \frac{\frac{L_i s + r_i + R_d}{R_d L_i C_i}}{s^2 + (\frac{r_i}{L_i} + \frac{1}{R_d C_i})s + (\frac{r_i}{R_d L_i C_i} + \frac{1}{R_d C_i})}$$
(4.3)

4.2.2 Output Filter

The output LC filter reduces the voltage harmonics generated by the power converters. The single phase output filter schematic is shown in Fig. 4.2. By choosing higher switching frequency the size of filter components L an C can be reduced. But the switching frequency is limited by the power switches used in the power converter. The cut-off frequency of the filter is chosen appropriately to eliminate most of the dominant harmonics. To operate the power converter as an ideal voltage source, whose voltage is constant against load variation and non-linear loads, the output impedance of the



Figure 4.1: Input filter schematic diagram.

converter has to be very low. By maximizing the capacitance value and minimizing the inductance value of the filter, this condition can be achieved. But the increment in capacitance value increases the reactive power. This further increases the power rating of the converter. Therefore value of capacitor has to be limited to some value. This will proportionally increase the value of inductor. The increase in the reactance of the inductor causes a increase in the voltage drop across the filter. A trade-off between the values of capacitor and inductor has to be made to have a optimal solution to the problem. To reduce the distortion and voltage drop trial and error method is used to modify the filter design values.



Figure 4.2: Output filter schematic diagram.

| Device | Description | Abbrevation | Real value |
|----------------------------|---------------|-------------|------------|
| DVR | Rated Power | S_{DVR} | 1.5kVA |
| | Phase voltage | V_{DVR} | 230V |
| High frequency transformer | Turns Ratio | n | 1:1:1:1 |
| | | | |
| Input Filter | Inductance | L_i | 0.006H |
| | Capacitance | C_i | 47μ F |
| Output Filter | Inductance | L_o | 0.002 H |
| | Capacitance | C_o | 47μ F |

 Table 4.1: DVR parameters used in simulation

The transfer function equation of the output filter is given by (4.4).

$$F_o(s) = \frac{\frac{1}{L_o C_o}}{s^2 + \frac{r_o}{L_o}s + \frac{1}{L_o C_o}}$$
(4.4)

The DVR parameters used for the simulation can be summarized as in Table 4.1

4.3 Simulation Results for Different loading Conditions

The performance of the DVR is investigated under different loading conditions.

4.3.1 Linear Load

The static performance of the DVR against different types of linear loads such as resistive and inductive loads have been considered. Symmetric and non-symmetric loading conditions are also investigated.

4.3.2 Non-Linear Load

Non-linear load causes more distortion in the load voltage. The performance of the DVR is investigated against an uncontrolled four pulse diode bridge with a constant dc-link voltage as shown in Fig.4.3



Figure 4.3: Uncontrolled diode bridge rectifier non-linear load

4.3.2.1 Different Voltage Sag Conditions

Voltage sag is created mainly due to faults in the line. The most frequent fault is single line to ground fault. Three phase to ground fault creates symmetric voltage sag. A solid line to ground fault creates outage.

- 1. Load types
 - Linear load
 - Non-linear
- 2. Fault types
 - Single phase fault with impedance
 - Single phase solid fault
 - three phase Symmetric fault
 - Three phase Non-symmetric fault

4.3.2.2 Generation of voltage dip

Different voltage sag conditions are generated by applying a fault at respective phases. Outages are created by applying solid short circuit to the respective phase. Resistive faults do not create any phase shift in the load voltage, but inductive faults create magnitude reduction and phase jump in the load voltage. The application of fault in the source side is shown in Fig. 4.4


Figure 4.4: Voltage sag generation applying fault

4.3.3 Performance of DVR against single phase voltage dip with linear load

Here a linear load has been considered. A single phase line to ground fault is applied to get 50% sag in the supply side voltage. The fault is applied at 7.102s and ends at 7.250s. Single phase fault is the most frequent fault in a power system. Fig. 4.5 shows the three phase supply voltage without any sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.6. The control voltage generated for compensation of phase-A is shown in Fig. 4.7.



Figure 4.5: Three phase input phase voltage without sag

The injected voltage waveform is shown in Fig. 4.8. The load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.9. RMS waveforms of source and load voltages is shown in Fig.4.10. From the RMS voltage waveforms it is clear that



Figure 4.6: Three phase input phase voltage with single phase sag for linear load



Figure 4.7: Control voltages for phase-A in single phase fault, linear load case

the load voltage is maintained below the IEEE tolerance band of 10%.



Figure 4.8: Injected voltages for phase-A in single phase fault, linear load case



Figure 4.9: Single phase compensated load voltage in single phase fault, linear load case



Figure 4.10: RMS value compensated load voltages in single phase fault, linear load case

4.3.4 Performance of DVR against single phase voltage dip with Non-linear load

A single phase diode bridge with a resistive load is taken as the non-linear load. A single phase line to ground fault is applied to get 50% sag in the supply side voltage. The fault is applied at 7.152s and ends at 7.398s. Single phase fault is the most frequent fault in a power system. Fig. 4.11 shows the three phase supply voltage without any sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.12.

The control voltage required to compensate the sag is generated by the controller and is shown in Fig. 4.13. The injected voltage waveform is shown in Fig. 4.14. The



Figure 4.11: Three phase input phase voltage without sag in single phase fault nonlinear load case



Figure 4.12: Three phase input phase voltage with single phase sag in single phase fault non-linear load case



Figure 4.13: Control voltages for phase-A in single phase fault non-linear load case

load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.15. RMS waveforms of source and load voltages is shown in Fig.4.16. From the RMS voltage



Figure 4.14: Injected voltages for phase-A in single phase fault non-linear load case



Figure 4.15: Single phase compensated load voltage in single phase fault non-linear load case

waveforms it is clear that the load voltage is maintained below the IEEE standard tolerance band of 10%.

4.3.5 Performance of DVR against single phase outage

Here a linear load has been considered. A single phase solid line to ground fault is applied to get outage at one phase. The fault is applied at 7.102s and ends at 7.398s. Fig. 4.17 shows the three phase supply voltage without any sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.18.

The control voltage generated for single phase outage is shown in Fig. 4.19. The injected voltage waveform is shown in Fig. 4.20. The load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.21. RMS waveforms of source and



Figure 4.16: RMS value compensated load voltages in single phase fault non-linear load case



Figure 4.17: Three phase input phase voltage without sag in single phase outage case



Figure 4.18: Three phase input phase voltage with single phase outage

load voltages is shown in Fig.4.22. From the RMS voltage waveforms it is clear that the load voltage is maintained below the IEEE tolerance band of 10%.



Figure 4.19: Control voltages for phase-A in single phase outage case



Figure 4.20: Injected voltages for phase-A in single phase outage case



Figure 4.21: Single phase compensated load voltage in single phase outage case



Figure 4.22: RMS value compensated load voltages in single phase outage case

4.3.6 Performance of DVR against three phase symmetric voltage dip with linear load

A three phase line to ground fault is applied to get 40% sag in the supply side voltage. The fault is applied at 7.102s and ends at 7.398s. This is the most powerful fault a DVR has to compensate. Fig. 4.23 shows the three phase supply voltage without any sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.24.



Figure 4.23: Three phase input phase voltage without sag in three phase symmetric fault, linear load case

The control voltage generated for compensation of phase-A is shown in Fig. 4.25. The injected voltage waveform is shown in Fig. 4.26. The load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.27. Corresponding RMS load voltages is shown in 4.28. From the RMS voltage waveforms it is clear that the load



Figure 4.24: Three phase input phase voltage with three phase symmetric sag for a linear load



Figure 4.25: Control voltages for phase-A in three phase symmetric sag, linear load case



Figure 4.26: Injected voltages for phase-A in three phase symmetric sag, linear load case



Figure 4.27: Compensated load voltage for phase-A in three phase symmetric sag, linear load case

voltage is maintained below the IEEE tolerance band of 10%.



Figure 4.28: RMS value compensated load voltages in three phase symmetric sag, linear load case

4.3.7 Performance of DVR against three phase unsymmetric voltage dip with linear load

A three phase line to ground fault is applied to get unsymmetrical voltage sag in the supply side voltage. The fault is applied at 7.102s and ends at 7.398s. This is the most powerful fault a DVR has to compensate. Fig. 4.29 shows the three phase supply voltage without any sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.30.



Figure 4.29: Three phase input phase voltage without sag



Figure 4.30: Three phase input phase voltage with three phase unsymmetric sag



Figure 4.31: Control voltages for phase-A in three phase unsymmetric sag, linear load case

The control voltage corresponding to the sag is shown in Fig.4.31. The injected voltage waveform is shown in Fig. 4.32. The load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.33. Corresponding RMS load voltages is

shown in 4.34. From the RMS voltage waveforms it is clear that the load voltage is maintained below the IEEE tolerance band of 10%.



Figure 4.32: Injected voltages for phase-A in three phase unsymmetric sag, linear load case



Figure 4.33: Compensated load voltage for phase-A in three phase unsymmetric sag, linear load case

4.3.8 Performance of DVR against three phase symmetric voltage dip with non-linear load

A three phase line to ground fault is applied to get 40% sag in the supply side voltage. The fault is applied at 7.102s and ends at 7.398s. This is the most powerful fault a DVR has to compensate. Fig. 4.35 shows the three phase supply voltage without any



Figure 4.34: RMS value compensated load voltages in three phase unsymmetric sag, linear load case



Figure 4.35: Three phase input phase voltage without sag

sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.36.



Figure 4.36: Three phase input phase voltage with three phase symmetric sag



Figure 4.37: Control voltage for phase-A in three phase symmetric sag, non-linear load case



Figure 4.38: Injected voltages for phase-A in three phase symmetric sag, non-linear load case

The required control voltage is generated as shown in Fig. 4.37. The injected voltage waveform is shown in Fig. 4.38. The load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.39. One cycle view of the compensated voltage is shown in Fig. 4.40 and is clear from the figure that delay in compensation is less than 3ms. Corresponding RMS load voltages is shown in 4.41. From the RMS voltage waveforms it is clear that the load voltage is maintained below the IEEE tolerance band of 10%.



Figure 4.39: Compensated load voltage for phase-A in three phase symmetric sag, non-linear load case



Figure 4.40: One cycle view of instantaneous load voltage in three phase symmetric sag, non-linear load case

4.3.9 Performance of DVR against three phase unsymmetric voltage dip with non-linear load

A three phase line to ground fault is applied to get unsymmetrical voltage sag in the supply side voltage. The fault is applied at 7.102s and ends at 7.398s. This is the most powerful fault a DVR has to compensate. Fig. 4.42 shows the three phase supply voltage without any sag. Three phase input voltage waveform with the introduction of sag is shown in Fig. 4.43.

The control voltage for phase-A is shown in Fig. 4.44. The injected voltage waveform is shown in Fig. 4.45. The load voltage maintained at pre-sag voltage using DVR and is shown in Fig. 4.46. Corresponding RMS load voltages is shown in 4.48.



Figure 4.41: RMS value compensated load voltages in three phase symmetric sag, non-linear load case



Figure 4.42: Three phase input phase voltage without sag



Figure 4.43: Three phase input phase voltage with three phase unsymmetric sag

From the RMS voltage waveforms it is clear that the load voltage is maintained below the IEEE tolerance band of 10%.



Figure 4.44: Control voltages for phase-A in three phase unsymmetric sag, non-linear load case



Figure 4.45: Injected voltages for phase-A in three phase unsymmetric sag, non-linear load case

Bipolar sinusoidal PWM switching strategy is used for the three VSI to generate the compensating voltages. The switching frequency of the inverter is set at 4950Hz.The pulsating voltage produced using SPWM is filtered using low pass LC filter to produce sinusoidal voltage waveform at the output by eliminating the harmonics. The load THD is calculated to be 4.3, which is well below the limit specified by IEEE standards.



Figure 4.46: Compensated load voltage for phase-A in three phase unsymmetric sag, non-linear load case



Figure 4.47: Compensated load voltage for phase-A expanded view in three phase unsymmetric sag, non-linear load case



Figure 4.48: RMS value compensated load voltages in three phase unsymmetric sag, non-linear load case

4.4 Conclusion

The performance of the proposed DVR is analyzed using industry standard power system simulation package PSACD/EMTDC. Different kinds of loads such as linear and non-linear has been considered for the analysis. Different voltage sag conditions like single phase, three phase symmetric and three phase un-symmetric sag have been considered. The proposed DVR is found to be capable of compensating the voltage sag conditions considered effectively. The dynamic characteristics also studied.

It can be observed that the proposed DVR responds instantaneously and the load voltage is maintained constant. In case of distortion in the supply voltages, there may not be sharp zero-crossings. This may make it difficult to find the actual zero crossing oints from the source voltage. As can be seen, the rms load bus voltage reaches zero during the fault, and as the enlarged figure shows, in about half a cycle, the DVR has succeeded in restoring the PCC voltage waveshape to the normal condition. It should be noted that the amount and shape of the oscillations depend on the time of applying the fault.

Chapter 5

Concluding Remarks and Future Works

Proposed DVR topology has been simulated using industrial standard simulation tool PSCAD/EMTDC. With the introduction of more sensitive equipments, the importance of improving the power quality also increases. The quality of the power supply is also decreasing day by day with the large addition of power electronic controllers. The major power quality issues are identified to be voltage sag, voltage swell and voltage harmonics. A huge amount of loss is happening every year to the industry because of power quality issues. Power quality issues also reduces the quality of the products. The DVR location can be at the critical load terminal or at the facility that contain the critical load. It can also be placed at the distribution level.

To provide a basis for the design of the DVR the most frequent and severe power quality issues have been discussed with focus on voltage sag. The proposed DVR consists of a three phase to single phase matrix converter, an uncontrolled diode bridge and a VSI. In conventional method the DVR consists of a VSI and an injection transformer, which provides galvanic isolation and voltage boosting. In the proposed topology the line frequency injection transformer is replaced with a high frequency transformer. The energy required during sag is directly taken from the supply itself. Replacing the line frequency transformer with HF transformer gives reduction in weight and size of the DVR, making it cheaper. Since it is shunt connected converter topology there is no need of an energy storage and there is no limit on the duration of sag compensation range. But, the duration of sag compensation range is limited by the thermal stress on the semiconductors used. There is a small voltage drop due to the filter inductance and it also causes a small phase shift in the compensated load voltage. Bipolar sinusoidal PWM switching is used for the VSI.

The simulation of the proposed DVR has been presented in Chapter 4. The converter is modeled in simulation platform PSCAD. The model is used to evaluate the performance of the DVR against different loading conditions and different voltage sag conditions. Static and dynamic analysis are carried out on the DVR with linear and non-linear load. Static tests gives the performance of the DVR against different load and fault conditions. Non-linear load causes more distortion. Dynamic test gives the response time of the DVR and it is found to be less than 3ms. The voltage dip were generated by creating fault at respective phases through a controlled resistance.

Voltage dips where generated by creating a controlled short circuit at the source side. Different types of faults like single phase fault, three phase symmetrical and non-symmetrical faults were also created to test the performance of the DVR during different sag conditions.

5.1 Future works

In-depth study of several topics have not been carried out in this thesis. The scope for future works include

- Loads like motor loads, thyristor loads, and active rectifier loads can be tested to verify the robustness of the proposed topology
- Optimum damping of the switching harmonics generated by the converters can be done by doing better design and tuning of filters, hence the oscillations at non-linear load and oscillations at the beginning and at the end of the voltage sag.
- Further investigation of robustness against voltage swell, transients and harmonics.
- Calculation of voltage drop and power loss occurred by DVR
- Calculation of the cost against the voltage improvement.

Appendix Derivations

A-1 Transfer Function Calculation of Input Filter

The single phase equivalent of input filter with damping resistor R_d is shown in Fig. A.1. ' r_i ' represents the internal resistance of the inductor.



Figure A.1: Input filter schematic connected at the input of the matrix converter.

The transfer function of the filter can be represented as

$$F_i(s) = \frac{V_o(s)}{V_i(s)} \tag{A.1}$$

Substituting the input and output voltage expression for each of the circuit components,

$$V_o = \frac{1}{C_i} \int i dt = \frac{1}{C_i} \int (i_a + i_b) dt \tag{A.2}$$

$$V_{i} = L_{i}\frac{di_{b}}{dt} + ri_{b} + \frac{1}{C_{i}}\int idt = L_{i}\frac{di_{b}}{dt} + ri_{b} + \frac{1}{C_{i}}\int (i_{a} + i_{b})dt$$
(A.3)

The relationship between i_a and i_b can be found as,

$$V_{R_d} = V_{L_i} + V_{r_i}; R_d i_a = L_i \frac{di_b}{dt} + r_i i_b$$
(A.4)

$$\Rightarrow i_a = \frac{L_i}{R_d} \frac{di_b}{dt} + \frac{r_i}{R_d} i_b \tag{A.5}$$

Substituting Equation (A.5) into Equations (A.2) and Equation (A.3) and applying Laplace transform,

$$V_o(s) = \frac{(L_i s + r_i + R_d)}{R_d C_i s} I_b(s)$$
(A.6)

$$V_i(s) = \frac{R_d L_i C_i s + (r_i R_d C_i + L_i) s + (r_i + R_d)}{R_d C_i s} I_b(s)$$
(A.7)

Finally, the expression of the input filter transfer function is found as,

$$F_i(s) = \frac{\frac{L_i s + r_i + R_d}{R_d L_i C_i}}{s^2 + (\frac{r_i}{L_i} + \frac{1}{R_d C_i})s + (\frac{r_i}{R_d L_i C_i} + \frac{1}{R_d C_i})}$$
(A.8)

A-2 Transfer Function Calculation of Output Filter

The schematic diagram of the output filter is as shown in Fig.??



Figure A.2: Output filter schematic diagram.

The transfer function of the output filter can be defined by equation A.9

$$F_o(s) = \frac{V_o(s)}{V_i(s)} \tag{A.9}$$

The input and output voltage equation are given by Equation (A.11) and (A.10) respectively

$$V_o = V_{C_o} = \frac{1}{C_o} \int i dt \tag{A.10}$$

$$V_i = L_o \frac{di}{dt} + r_o i + \frac{1}{C_o} \int i dt \tag{A.11}$$

Applying Laplace transform to Equation (A.10) and Equation (A.11), the output and input voltage can be expressed as,

$$V_o(s) = \frac{I(s)}{C_o s} \tag{A.12}$$

$$V_{i}(s) = I(s)(L_{o}s + r_{o} + \frac{R}{C_{o}s})$$
(A.13)

The transfer function equation of the output filter is given by Equation (A.14).

$$F_o(s) = \frac{\frac{1}{L_o C_o}}{s^2 + \frac{r_o}{L_o}s + \frac{1}{L_o C_o}}$$
(A.14)

A-3 Load Impedance Calculation

The power per phase is given by

$$S = \frac{1500}{3} = 500VA. \tag{A.15}$$

The equivalent load impedance is given by

$$S = VI = V \cdot \frac{V}{Z_L} = \frac{V^2}{Z_L}.$$
(A.16)

where V is the rated load voltage and I is the rated load current. The load impedance Z_L is given by

$$Z_L = \frac{V^2}{Z_L} = \frac{230^2}{500} = 105.8\Omega.$$
 (A.17)

For a resistive load $Z_L = R_L$. For an inductive load, assuming a power factor of 0.8

$$|Z_L| = \sqrt{R_L^2 + X_L^2}$$
 (A.18)

The values of load resistance, R_L and load inductive reactance, X_L are given by

$$R_L = |Z|\cos\theta = 84.64\Omega \tag{A.19}$$

$$X_L = |Z|\cos\theta = 63.48\Omega \tag{A.20}$$

$$X_L = \omega L = 2\pi f L = 2\pi * 50 * L \tag{A.21}$$

Therefore the value of load inductance, \boldsymbol{L} is

$$L = \frac{X_L}{100\pi} = \frac{63.48}{100\pi} = 1.98H \tag{A.22}$$

Therefore the load impedance is $Z_L = 84.64 + j1.98\Omega$

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