INVESTIGATION AND CONTROL OF HYBRID MULTILEVEL INVERTER TOPOLOGIES WITH REDUCED PART COUNT

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

SANDEEP N

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,
SURATHKAL, MANGALURU - 575025

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DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled "Investigation and Control of Hybrid Multilevel Inverter Topologies with Reduced Part Count" which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

.....

Sandeep N, 145089EE14F05
Department of Electrical and Electronics Engineering

Place: NITK-Surathkal
Date:

CERTIFICATE

This is to *certify* that the Research Thesis entitled "Investigation and Control of Hybrid Multilevel Inverter Topologies with Reduced Part Count" submitted by Sandeep N (Register Number: EE14F05) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

Prof. Udaykumar R. Y.
(Research Guide)

Dr. B. Venkatesaperumal
(Chairman-DRPC, EEE dept.)

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Sandeep N

Dedication

Dedicated to my mother Shyla and father Nataraja

Abstract

Multilevel inverters (MLIs) have become a preferred choice for low- and medium-power dc to ac energy conversion applications to ensure high power quality. The MLIs exhibit several advantages over the conventional two-level inverter which include reduced dv/dt, lesser electromagnetic interference, and capability to handle higher voltage levels with devices of lower voltage rating. These features have enabled them to gain popularity in a variety of industrial applications like locomotives, mixers, marine propulsion, reactive power compensation, renewable energy power conversion, to name a few. At present, electric power generation from renewables is being one of the subjects of high-interest; use of MLIs leads to reduced filter size, or even eliminate completely the filter requirements in such applications. The primary challenge in employing the multilevel configurations is the increased number of power devices and the circuit intricacies which adds on to the overall control complexity resulting in a higher cost. Thus, reduced circuit complexity and improved reliability are the desirable characteristics for an MLI to be qualified as an applicable power processing unit.

Ever since the inception of MLIs, cascaded H-bridge (CHB), neutral point clamped (NPC) and flying capacitor converters are among the earliest topologies that are deemed to be well-established. Each of them has advantages and disadvantages. An NPC MLI requires additional clamping diodes for its extension whereas, CHB MLI and flying capacitor MLI needs many isolated dc sources to generate a multistep output and multiple capacitors respectively. Since then, many derivatives and refinements to these classic topologies have been proposed. The motivation for this research work stems out from the demand to generate a substantial number of voltage levels while keeping the circuit reliability as high as possible. Therefore, by taking advantage of the basic MLI configurations, a few schemes emanating as a result of combining two or more MLIs in part or fully, referred to as hybrid MLIs are proposed in this thesis for grid-connected renewables. The offered solutions exhibit considerable topological improvements with reduced control complexity.

First, efforts are made to derive an innovative power circuit that generates nine-level (9L) voltage waveform from the three-level (3L) T-type NPC converter which is widely regarded as a highly efficient solution for low-power applications. It is achieved in two ways; in one way, by using a 3L floating capacitor H-bridge (FCHB) and a two-level (2L) converter leg in conjunction with the 3L-TNPC MLI whereas, in the other, by replacing the 3L-FCHB with a 2L switched-capacitor unit. In the latter case the number of controlled switches are reduced to 8 from 10. Further, the control complexity is reduced by applying a sensorless voltage control which is devoid of voltage and current sensor(s).

Second, an active NPC (ANPC) MLI suitable for medium-power applications is considered. Two completely new 9L topologies are derived advancing the ANPC converter. A hybrid topology based on 3L-ANPC MLI is the first power circuit built by connecting it with 3L-FCHB and also employs a 2L converter leg. The second hybrid MLI serves as an upgrade of the industrial standard 5L-ANPC MLI to 9L while requiring minimum structural disruption and modification which includes the addition of the 2L converter leg to the 5L-ANPC MLI. A simple logic-form-equations (LFE)-based closed-loop floating capacitor (FC) voltage balancing scheme is implemented by using the redundant switching states.

Third, a new hybrid stacked multi-cell (SMC) MLI is proposed. The power circuit is formed as a cascade connection of 5L-SMC and 3L-FCHB. This way the required number of capacitors are reduced to 3 from 8 as compared to the conventional extension of SMC MLI resulting in an increased reliability. The LFE-based voltage balancing scheme achieves the capacitors voltage regulation.

Last, the reliability of the proposed topologies is systematically evaluated and are compared. It is seen that each of the topologies qualify as a promising solution for multilevel voltage generation.

All the developed schemes are simulated in MATLAB/Simulink for grid-connected and stand-alone modes. The topologies are tested experimentally using dSPACE 1104 controller. Results validating the operability of the proposed topologies and the developed control schemes are presented.

Contents

List of Figures

List of Tables

List of Abbrevations

ANPC	Active neutral-point-clamped
CCIL	Cross-connected intermediate level
CHB	Cascaded-H-bridge
DFCM	Double flying capacitor multi-cell
FC	Floating capacitor
FCC	Flying capacitor converter
FCHB	Floating capacitor h-bridge
FIT	Failure in time
FMS	Fault management system
FTC	Fault-tolerant capability
HMC	Hybrid multicell converter
HV	High-voltage
LFE	Logic-form-equations
LFSs	Line frequency switches
LSR	Level-to-switch ratio
LV	Low-voltage
MLDCL	Multilevel dc link inverter
MTTF	Mean time to failure
MV	Medium-voltage
NPC	Neutral-point-clamped
PF	Power factor
PR	Proportional resonant
PV	Photovoltaic
PWM	Pulse width modulation
QFCM	Quadruple flying capacitor multi-cell
SANPC	Stacked active neutral-point-clamped
SC	Switched-capacitor
SMC	Stacked multi-cell
TBV	Total blocking voltage
THD	Total harmonic distortion
TM	Transition matrix
TNPC	T-type neutral-point-clamped

VDF	Voltage diversity factor
2L	Two-level
3L	Three-level
5L	Five-level
7L	Seven-level
8S-TNPC	8 switch TNPC
10S-ANPC	10 switch ANPC
10S-TNPC	10 switch TNPC
12S-ANPC	12 switch ANPC
12S-SMC	12 switch SMC

Chapter 1

INTRODUCTION

This chapter presents an introduction of the thesis, including an overview, features and topological aspects of MLIs. Following to the discussion on advantages and challenges confronted with the current MLIs, a critical review on hybrid MLI topologies is presented. At the end, the research objectives and organization of the thesis are included.

1.1 Overview

Nowadays, use of renewable energy sources like PVs and wind energy as a supplement to the conventional fossil fuel-based electric power generation has gained much attention in order to reduce the harmful effects of burning fossil fuels (Bose, 2013). For a reliable and efficient power extraction, the majority of such green power sources are expected to be grid-interactive (Eltawil and Zhao, 2010). In such an environment, power electronics converters play a significant role by serving as an integrator for dispersed generation into the grid with high efficiency and performance (Blaabjerg et al., 2004, Carrasco et al., 2006, Romero-Cadaval et al., 2013). Since the utility grid is of type ac, an inverter becomes an inevitable part of the grid-connected green sources (Kouro et al., 2015). With the deployment of these inverters for reliable power transactions, it further becomes essential to comply the standards set by the IEEE std-512 (1992) on the harmonic limit owing to their discrete switching actions resulting in harmonics. As a result, several variations in their structures are evident in the literature to satisfy such regulations (Kjaer et al., 2005). However, many of these topologies require higher filtering, or they operate with higher switching frequency

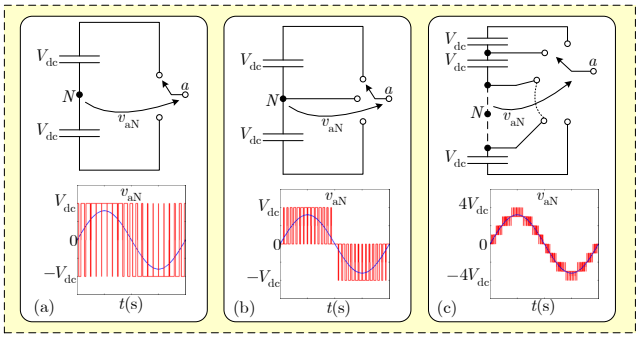


Figure 1.1: The functional diagram and evolution of an MLI (a) 2L (b) 3L, and (c) 9L output voltage

to meet the stringent harmonic limits. These setbacks are overcome using the MLIs which have not only superseded the use of a conventional 2L inverter in the field of grid-integration, but also in motor drives, traction, FACTS, HVDC and many others (Kouro et al., 2010).

1.2 MLI

An MLI is an array of semiconductor devices and isolated voltage sources that are controlled suitably to generate a multistep voltage waveform with variable and controllable amplitude, phase and frequency, as shown in Figure 1.1 (Rodriguez et al., 2002, 2009). The features like capability to handle high voltages with reduced device stresses, low switching, and conduction losses, enhanced power quality with less harmonic distortion are the main reasons for their widespread acceptance. Over the years, several MLI topologies are reported which can be broadly classified as shown in Figure 1.2. Among the many, a few of the recommended topologies that are regarded as applicable and classic MLIs are discussed as under.

1.2.1 NPC MLI

An NPC converter consists of two traditional 2L converters stacked one over the other and are fed by series connected capacitors (Nabae et al., 1981). A 5L power circuit is shown in Figure 1.3(a). It can be seen that it requires the generation of only four gate pulses for the upper four switches, whereas the lower ones receive inverted gating signals to avoid dc-link short-circuit. The NPC topology can be extended

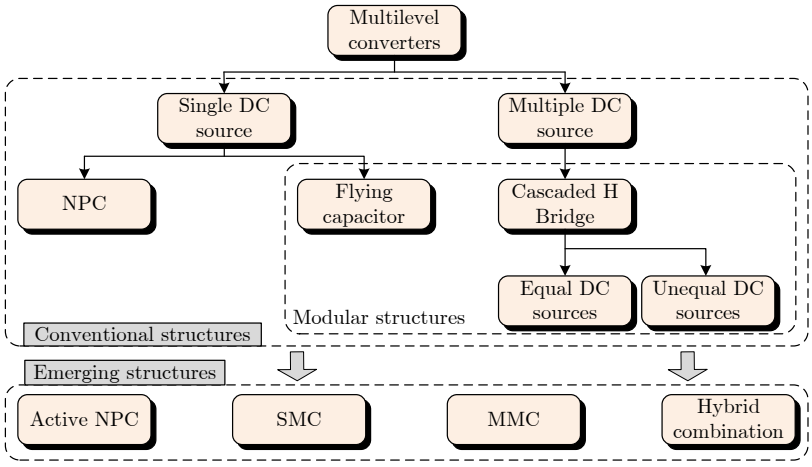


Figure 1.2: Broad classification of MLIs

to higher power rating and more output voltage levels by adding additional power switches and clamping diodes. As the number of output voltage level increases, the required number of clamping diodes increases dramatically. This fact, together with the increasing complexity to control the dc-link capacitor unbalance, has hindered the application of an NPC to a higher number of levels (>3) by the industries.

1.2.2 Flying capacitor MLI

The flying capacitor topology is slightly similar to the NPC, with the main difference that the clamping diodes are replaced by flying capacitors, as shown in Figure 1.3(b). As like an NPC, it also requires only four gating pulses. However, the complementary device positions are not the same. In comparison to an NPC, FC has a modular structure which enables its extension to extend to a higher voltage levels effortlessly. This also adds to the extra degree of freedom to control the converter with the help of many available redundant states.

1.2.3 CHB MLI

A CHB MLI is devised by connecting two or more 3L single-phase H-bridge inverters as shown in Figure 1.4(c) (Marchesoni et al., 1990). Each H-bridge can generate three different voltage levels ($0, V_{\mathrm{dc}}$, and $-V_{\mathrm{dc}}$). The output voltage is synthesized by adding each of the isolated dc voltage sources resulting in the generation of a stepped output voltage with a step size equal to the magnitude of the connected dc sources. It

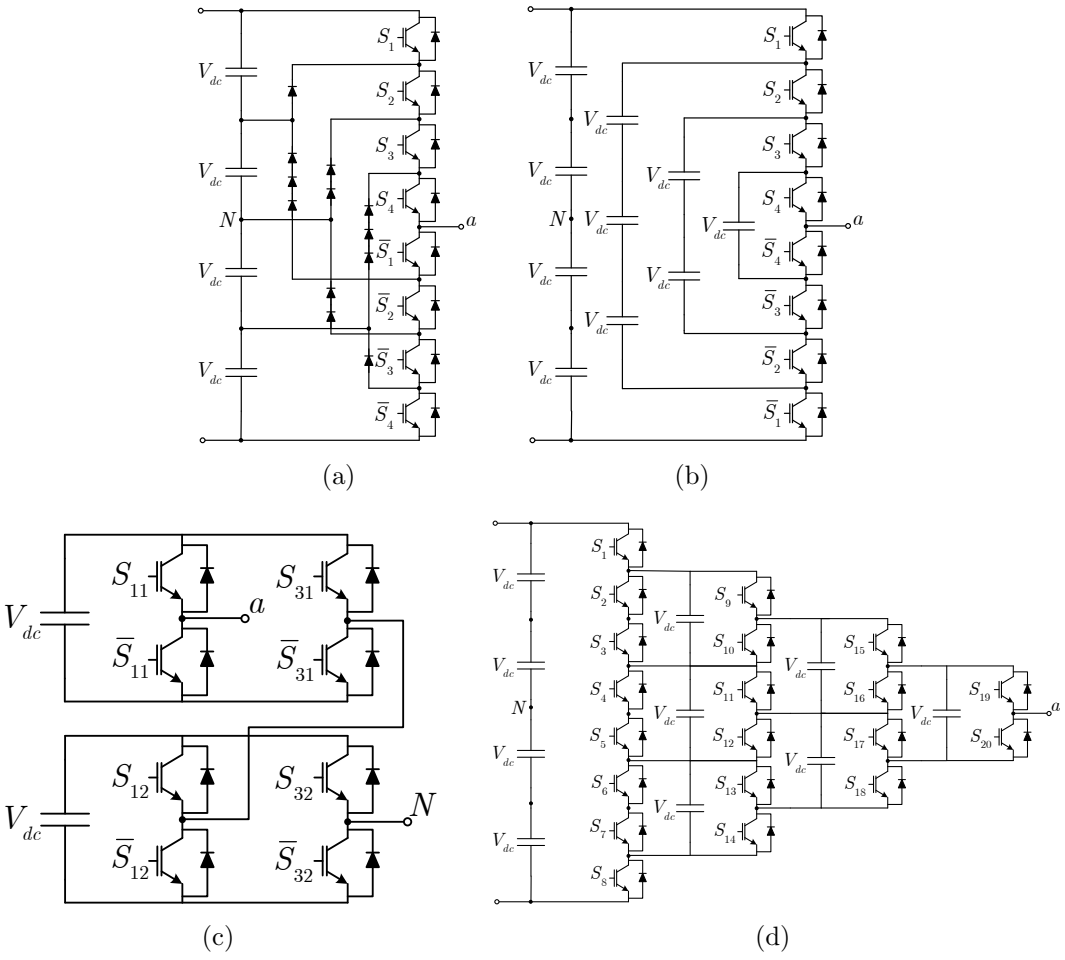


Figure 1.3: Classic MLI topologies (a) NPC (b) FC (c) CHB (d) generalized

is one of the highly regarded MLI as far as modularity and scalability are considered.

1.2.4 Generalized MLI

The generalized MLI shown in Figure 1.4(d) is composed of many 2L cells with capacitors placed at its dc-link (Peng, 2001). Any arbitrary type of MLI can be derived from this structure. One of the main features of this topology is the self-balancing capability of the capacitors. However, it requires a substantial quantity of devices and passive elements which makes it not so attractive for industrial application.

On the whole, these topologies serve as the primary building blocks for the multilevel voltage generation and are beneficial up to a certain number of voltage levels. Further, an attempt to increase the number of voltage levels call for a significant addi-

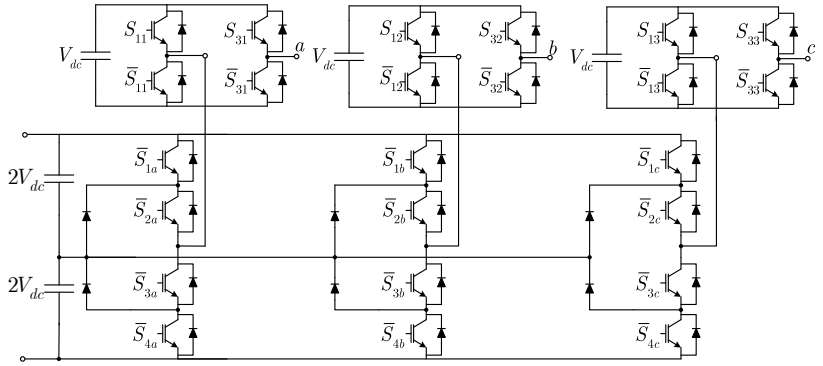


Figure 1.4: Cascaded hybrid MLI

tion of many semiconductor switches, diodes, and reactive components like capacitors. This escalates the intricacy of the circuit, which also the lead to the issues like dc-link voltage unbalance, higher losses and control complexity needs to be combated. With this background, emerging MLIs are introduced next.

1.2.5 Emerging MLIs

In the recent past, the idea of using different voltages on the intermediate circuit element (capacitor) has risen and is popularly known as asymmetric MLIs. This concept has been applied successfully to CHB MLI with unequal H-bridge's dc voltage (Mueller and Park, 1994, Lipo and Manjrekar, 1999, Steimer and Manjrekar, 2001). It is applied to other family of MLIs as well (Damiano et al., 1997). Structurally there is no difference between the symmetric and asymmetric MLI except the different capacitor voltages in the latter case. The main advantage of such an alteration is the generation of a higher number of voltage levels with an identical part count as that of a symmetric MLI.

Further, the combination of several MLIs, either two of them or just a part of an individual structure is termed as hybrid MLI. Theoretically, there are innumerable such possible combinations. With such an ingenious arrangement, the advantage of both the topologies can be extracted when put together, which is not achievable by considering them individually. As an example, a combination of a 2L inverter with a 3L-FCHB (Malinowski et al., 2010) or a 3L-NPC MLI in series with a 3L-FCHB is shown in Figure 1.4.

1.3 Research motivation

In practice, it is strenuous to assess various hybrid topologies as they are diverse in nature and represent a vast family (Rufer et al., 1999, Manjrekar et al., 2000a). Among the wide-ranging available hybrid MLIs, it is apparent that no specific solution seems to stand out from the others remarkably. Various factors that influence the selection of a particular topology are the cost, intended application and lifespan. Some of the critical topological aspects that are to be considered while justifying the merits of a hybrid MLI are as follows:

1. The part count (switches, diodes, capacitors).

2. The total standing voltage of the converter (summation of voltage across all the switches).

3. The controllability of the converter i.e., the degree of freedom in regulating the capacitor voltages.

On this line, the research work in this thesis aims to investigate the hybrid MLIs, and to synthesize possible topological variations for enhancing the structural and operational behavior of the selected emerging converter families. Besides, it also aims at developing suitable control strategies for the developed structures for their reliable operation. For this study, three converter families are considered; they are TNPC, ANPC, and SMC MLI. Further, a nonexhaustive but comprising the main topological variants pertaining to these selected converter topologies is briefly reviewed.

1.3.1 TNPC MLI

The TNPC MLI is very similar to NPC MLI except for use of bidirectional switches in place of clamping diodes (Guennegues et al., 2009). Addition of a single switch and four diodes as a bidirectional switch connected to the midpoint of one of the two 2L converter leg of a conventional 3L H-bridge inverter is demonstrated by (Selvaraj and Rahim, 2009). This modification enables the inverter to generate a 5L output voltage and is applied to a grid-connected PV system. Several other variations based on the same principle of using bidirectional switches is reported in (Rahim and Selvaraj, 2010, 2011).

1.3.2 ANPC MLI

An ANPC MLI is one of the widely used converter structure for both medium- and high- voltage applications. The commercial availability of the 5L-ANPC MLI as ACS2000 is the proof for its technical viability (Barbosa et al., 2005). A 9L inverter is realised using the cascade connection of a 3L-FCHB and NPC (Veenstra and Rufer, 2005). It requires a sophisticated common mode voltage control for regulating the capacitor voltage thereby limiting the maximum modulation index to 0.95 at nominal power. Another variation is the CCIL topology, which comprises of an ANPC and cross-connected switches (Chaudhuri et al., 2007, Chaudhuri and Rufer, 2010). Despite of their advantage in reducing the number of switches, use of a fuzzy logic control adds on to the control effort required for the latter structure thereby limits the maximum modulation index to 0.91. Use of cross-connected stage presented in (Chaudhuri et al., 2010) requires a larger number of devices of different voltage ratings and the maximum modulation index attainable is only 0.925. An interesting way of generating more voltage levels is discussed in (Xu et al., 2017) by combining ANPC and TNPC MLI through connecting switches. The key attractive feature of this topology is the use of low voltage devices while generating higher voltage levels (>7). Similarly, the topology in (Viju et al., 2017) is realized by stacking lower-space vector multilevel structures and are connected in series with a FCHB through a 2L convereter leg. Although the voltage stress across the devices is reduced, the number of FCs required is higher for more voltage levels. The idea of separating the level and polarity generation part while reducing the number of dc sources and power switches for a given number of voltage levels proposed by (Najafi and Yatim, 2012) is applied for the ANPC in (Wang et al., 2017). Although they operate at line frequency, the number of devices rated for full dc-link voltages are high in both the former and the latter structures.

1.3.3 SMC MLI

The increase in the number of voltage levels escalates the energy associated with the circuit. SMC MLI is one of the topologies intended to lessen the stored energy (Gateau et al., 2001). A new configuration with reduced number of switches and a single dc source-based SMC is proposed in (Hosseini et al., 2010). An innovative extension of 5L SMC to 9L using a 2L converter leg is presented in (Hosseini and Sadeghi, 2011).

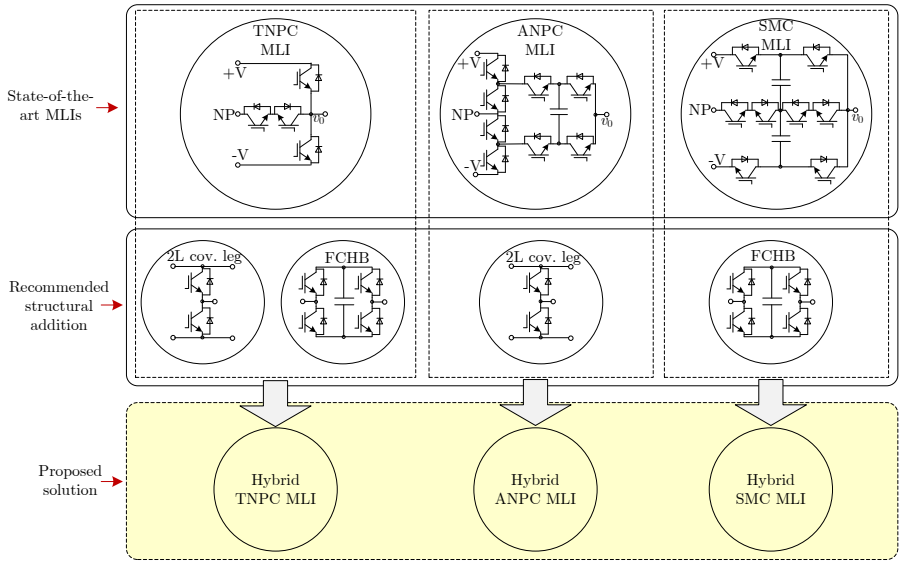


Figure 1.5: Proposed methodology for topology synthesis

Application of a single dc source-based SMC as a custom power device to enhance the power quality is demonstrated in (Dargahi et al., 2012).

Having outlined the variants and limitations of the hybrid topologies, this research is oriented on developing novel MLI configurations and control strategies to enhance their operational performance in grid-connected applications. Considering the optimization of converter topologies and generating higher number of voltage levels, the thesis aims at developing 9L-MLI topologies since 9L voltage waveform is found to exhibit a global compliance on the whole range of standard imposed (Chaudhuri, 2008). A bird's-eye view of the methodologies developed to improve the existing three converters of interest are shown in Figure 1.5.

1.4 Thesis objectives

The main objectives of this thesis are:

1. To develop novel 9L hybrid topologies based on the TNPC, ANPC, and SMC converter families.

2. To propose and verify sensorless voltage balancing strategy to control the proposed TNPC-based MLI.

3. To introduce and validate sensor-based voltage balancing method to control the proposed ANPC and SMC-based MLI.

4. To systematically evaluate, quantify and compare the reliability of the developed topologies.

1.5 Thesis organization

There are six chapters and three appendices in this thesis document. The outline of this thesis is highlighted in Figure 1.6.

Chapter 1: Presents a brief introduction to state-of-the-art MLI topologies and in particular, critically reviews the MLIs with reduced part count and their associated intricacies concerning grid-connected application.

Chapter 2: Proposes two variants of hybrid 9L-TNPC MLIs which have reduced power circuit complexity. Besides, a sensorless voltage balancing control to regulate the FC voltage is elaborated. Detailed simulation and experimental studies are carried out to validate the proof of controllability of the proposed topologies. A single-phase grid-connected case study is presented as an evidence of satisfactory application-oriented performance. Furthermore, a detailed comparison in terms of the number of power switches, FCs, and their ratings is deliberated in detail.

Chapter 3: Proposes two variants of hybrid 9L-ANPC MLIs which have reduced power circuit complexity. A simple LFE-based FC voltage balancing controller is developed. Simulation and experimental results are exemplified to validate the proposed system. The proposed topology and control strategy is verified through MATLAB simulations on a three-phase grid-connected case study. The possible extensions of the proposed topologies for a higher number of voltage levels are also presented. Finally, a comprehensive comparative study with other well-established MLIs is included.

Chapter 4: In this chapter, a hybrid 9L-SMC MLI with reduced part count is proposed. A detailed simulation of a three-phase grid-connected system

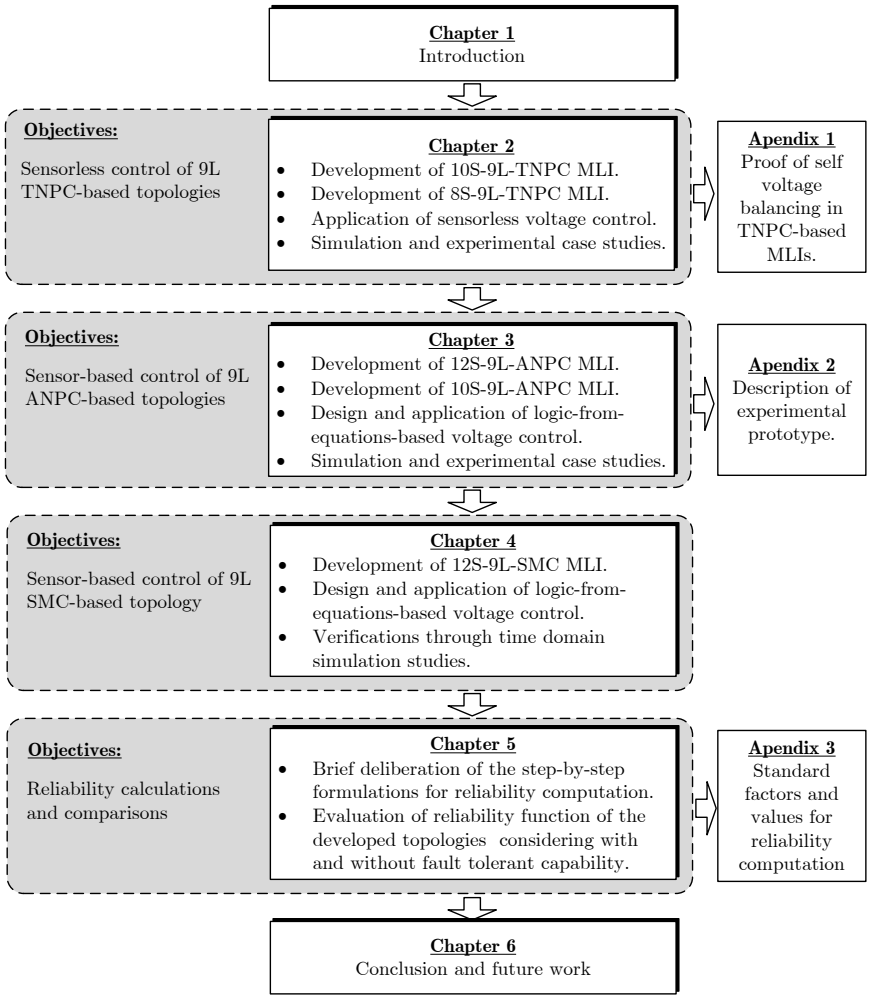


Figure 1.6: The outline of the thesis

comprising of the proposed SMC MLI topology and the developed LFE-based controller is elucidated. Following a thorough comparison with other MLIs, the results are presented.

Chapter 5: The fault-tolerant capability of the topologies introduced in chapter- 2, 3, and 4 are analyzed. A step-by-step methodology for the evaluation of the reliability of the developed topology is presented. The simulation results are shown to verify the fault-tolerant operations. Further, a comprehensive reliability comparison is performed.

Chapter 6: Summarizes the thesis major contributions and includes some discussions on possible future research.

Chapter 2

HYBRID TNPC CONVERTER

2.1 Introduction

This chapter introduces a new 9L MLI referred to as hybrid TNPC MLI comprising of a 3L-TNPC converter, 3L-FCHB, and a 2L converter leg. As the proposed MLI includes an FC, for generating an output voltage with equal-steps and less harmonic distortion, its voltage regulation is imperative and for this, a control strategy devoid of voltage/current sensor is developed to maintain the same around the reference value. The advantages of such a sensorless control are reduced control requirement, cost, and overall system intricacies.

In this chapter, first, the topological details of the proposed hybrid TNPC topology is described in detail, followed by the sensorless PWM technique. Secondly, an improved version of the topology is introduced. The simulation and experimental results pertaining to both the circuits are provided with a detailed comparative evaluation.

2.2 Problem formulation

The 3L-NPC proposed by (Nabae et al., 1981) is considered as an early ingenious MLI for MV applications. However, its application is limited to voltage levels of three, since the circuit performance gets considerably affected by the increased number of clamping switches and unbalance of dc-link capacitor voltage for more than three levels. Furthermore, recent literature advocates the use of NPC for high-efficiency low-power

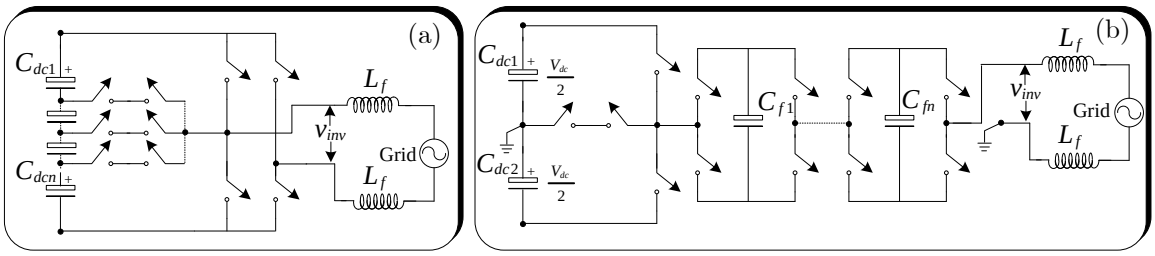


Figure 2.1: Possible ways of extending 3L-TNPC MLI to a higher number of voltage levels

applications by replacing the clamping switches with bi-directional switches (Dixon and Moran, 2006, Schweizer and Kolar, 2013). Although for 3L voltage generation, a TNPC MLI is found to be an attractive and viable solution, its extension to a higher number of voltage levels is strenuous. One of the widely adopted methods for such an extension in the literature is by appending more number of dc-link capacitors (Rahim et al., 2011, Alishah et al., 2015, 2017). Such an extension leads to increased component count and also, more importantly, dc-link voltage unbalance. The objective of this research work is to present an unprecedented hybridization approach with reduced part count and control complexity as compared to the other prior-art TNPC-based 9L topologies. With this motivation, on the first hand, the proposed hybrid 10S-TNPC MLI, and the associated control strategy are detailed. On the second hand, an innovative way to further reduce the required number of switches referred to as hybrid 8S-TNPC MLI is demonstrated and validated.

Figure 2.1 shows two possible ways of extending a 3L-TNPC MLI to generate more number of voltage levels. The first way is by appending additional dc-link capacitors as depicted in Figure 2.1(a). In this case, the number of voltage levels (N_{L}) is related to the number of dc-link capacitors (N_{cap}) which is given as,

$$N_{\mathrm{L}} = (2N_{\mathrm{cap}}) + 1. \tag{2.1}$$

Another way is to preserve the basic 3L-TNPC unit and extend it for higher voltage levels by adding 3L-FCHBs (refer Figure 2.1(b)). Hence, the number of levels depends on the number of FCHBs (m) and is given as,

$$N_{\mathrm{L}} = 2^{\mathrm{m}+1} + 1. \tag{2.2}$$

Both of the methods have their advantages and disadvantages. For a given number

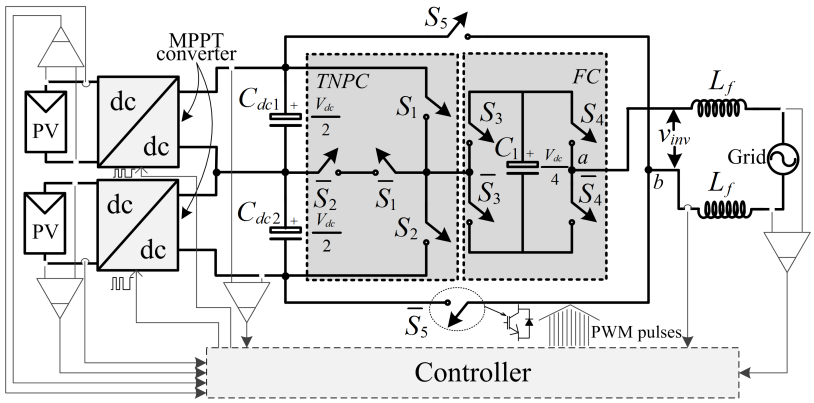


Figure 2.2: Functional diagram of the proposed 9L 10S-TNPC MLI

of voltage levels, the former structure requires a lesser number of switches than the latter. However, the dc-link unbalance arrises with post addition of multiple dc-link capacitors in the former case which calls for an extra voltage balancing circuit thus, increases the overall cost. Whereas, the latter case requires additional sensors for regulating the FC voltage to its corresponding reference value. Thus, this shows that a structure amalgamating the characteristics of both of the notions mentioned above is worth investigating.

2.3 Hybrid 10S-TNPC MLI topology synthesis

The first step in the hybridization is to delicately analyze the converter unit to be retained as a fundamental power electronic building block. In this proposed work, 3L- TNPC unit is kept unaltered, and a 3L-FCHB is connected in cascade. This particular combination results in the generation of a 5L output voltage. However, 9L voltage generation being the prime focus of the thesis, a 2L inverter leg is appended, whose midpoint is employed as another ac terminal. The resulting structure as shown in Figure 2.2 consists of the following subsystems:

- The 3L-TNPC unit is capable of generating the following three voltage levels: $V_{\mathrm{dc}}/2$ (switch S_1 is ON), $-V_{\mathrm{dc}}/2$ (switch S_2 is ON), and 0 (switches $\bar{S}_1$, and $\bar{S}_2$ are ON). The outer switches S_1 and S_2 need to block the full dc-link voltage whereas, the inner bidirectional switches are rated for half the dc-link voltage.

- The FC of the FCHB is to be regulated at one-fourth of the dc-link voltage, i.e.,

$V_{dc}/4$. It generates the following three voltage levels; $V_{dc}/4$ (switches $\bar{S}_3$ and S_4 are ON), $-V_{dc}/4$ (switches S_3, and $\bar{S}_4$ are ON), and 0 (switches S_3, and S_4 are ON or switches $\bar{S}_3$, and $\bar{S}_4$ are ON). The standing voltage across all the four switches of FCHB unit is equal to $V_{dc}/4$.

- Contrary to the general practice of utilizing dc-link midpoint as another ac terminal, here, the midpoint of the 2L inverter leg is used as the load terminal. Such an arrangement leads to doubling the number of voltage levels while offering a reduced switch count.

In a hybrid MLI, it is desirable to have the power devices with higher blocking voltage with low frequency switching and vice versa (Manjrekar et al., 2000b). Hence, as the tradition goes, the 2L inverter which withstands the full dc-link voltage operate in a square wave mode (fundamental frequency) and thus the losses due to switching is very less. The 3L-FCHB operate at highest switching frequency. The operating frequency of the switches corresponding to TNPC unit lies between the operating frequency of the 2L converter and 3L-FCHB.

By choosing proper switching combinations, a multilevel waveform at the output of the MLI can be generated. Besides, it is vital to understand the effect of such switching combination on the FC voltage beforehand to exercise the corrective actions for ensuring FC voltage around the reference value. Therefore to aid this process of understanding the holistic behavior of the proposed MLI, the various switching states and their effect on FC voltage is summarized and tabulated in Table 2.1. It is evident from Table 2.1 that there are 16 states which provide a different path for the current from the dc source to the load. Among which, a few of the combinations result in same output voltage level while having an opposite effect on FC voltage are commonly referred to as redundant states. In general, the FC voltage starts discharging when the dc source and FC are connected in additive polarity, and the effect reverses with the reversal of load current. The FC voltage remains unaltered when the FCHB is in bypass mode since it neither connects FC to the load nor to the source. Once the effect of each switching states is analyzed thoroughly, the switching strategy required for the generation of the multilevel waveform is developed.

One of the key issues in developing the switching strategy is to maintain the FC voltage at its reference value, since in the process of generating output voltage levels, the voltage across FC gets diverged from its desired value. Thus a dedicated

Table 2.1: Switching states and their impact on FC voltage of the proposed 10S-TNPC MLI

States	S_1	S_2	S_3	S_4	S_5	Output voltage	FC voltage
L_{4+}	1	0	1	1	0	V_{dc}	No effect
L_{31+}	0	0	0	1	0	$3V_{\mathrm{dc}}/4$	Discharging
L_{32+}	1	0	1	0	0	$3V_{\mathrm{dc}}/4$	Charging
L_{2+}	0	0	1	1	0	$V_{\mathrm{dc}}/2$	No effect
L_{11+}	0	1	0	1	0	$V_{\mathrm{dc}}/4$	Disharging
L_{12+}	0	0	1	0	0	$V_{\mathrm{dc}}/4$	Charging
L_{0+}	0	1	1	1	0	0	No effect
L_{0-}	1	0	1	1	1	0	No effect
L_{11-}	1	0	1	0	1	$-V_{\mathrm{dc}}/4$	Discharging
L_{12-}	0	0	0	1	1	$-V_{\mathrm{dc}}/4$	Charging
L_{2-}	0	0	1	1	1	$-V_{\mathrm{dc}}/2$	No effect
L_{31-}	0	0	1	0	1	$-3V_{\mathrm{dc}}/4$	Discharging
L_{32-}	0	1	0	1	1	$-3V_{\mathrm{dc}}/4$	Charging
L_{4-}	0	1	1	1	1	$-V_{\mathrm{dc}}$	No effect

controller is essential to take care of this issue. Since the proposed MLI exhibits sufficient redundancies, the necessity of an additional controller and a sensor can be confronted by integrating the capacitor balancing feature with the modulation technique as demonstrated in (Vahedi et al., 2016) for a packed-U-cell converter. This obviates the need for complex computations and simplifies the control implementation in the real-time. The interesting fact as obvious from Table 2.1 is that the FC can be charged and discharged in both the positive half and negative half cycle. Therefore it is decided to charge the FC during positive half cycle and discharge during the negative half. The repetition of the above process naturally regulates the FC voltage to $V_{\mathrm{dc}}/4$. A detailed derivation validating the natural balancing of FC is included in Appendix A.

2.4 Multilevel PWM with integrated FC voltage balancing

As highlighted above, the proposed switching strategy aims to amalgamate the FC voltage balancing with PWM technique. The methodology is derived from (Vahedi et al., 2016) and is adapted accordingly. Contrary to multi-carrier PWM proposed in (Vahedi et al., 2016), a single carrier-based gate pulse generation is developed. The

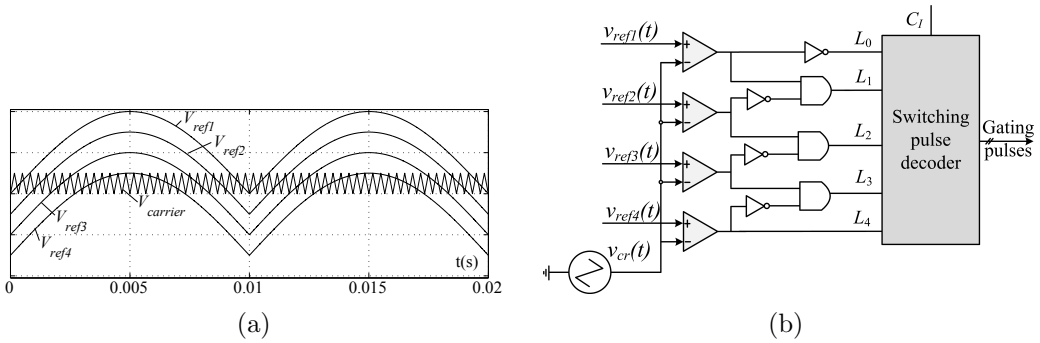


Figure 2.3: (a) Multilevel PWM reference and carrier signals (b) PWM modulator

9L PWM scheme includes a single high-frequency carrier, and four rectified sinusoidal reference waveforms as depicted in Figure 2.3. The sinusoidal reference waveforms ($V_{ref1}(t), V_{ref2}(t), V_{ref3}(t)$ and $V_{ref4}(t)$) are of same amplitude and phase, except the dc offset of magnitude equal to the maximum amplitude of the carrier signal ($V_{carrier}(t)$) as shown in Figure 2.3(a) (Sandeep et al., 2014). Each of the reference signals is compared with the carrier waveform and the information regarding the voltage levels is constructed from these comparator outputs by applying suitable logic operation (see Figure 2.3(b)). Wherein L_0, L_1, L_2, L_3, and L_4 are the binary interpretation corresponding to the voltage step to be generated. At a given instance either of the five variables is '1'. For example, if $L_3 = 1$, then output voltage level $V_{\rm dc}/2$ is to be generated. Owing to the rectified nature of the reference sinusoidal waveforms, one needs to know the half cycle change. Therefore, a cycle separation/identification unit is incorporated which is designated as C_I. The output voltage levels correspond to positive values and negative values if $C_I = 1$ and $C_I = 0$ respectively. With these underlying principles, a look-up table is developed whose row index refers to the binary variables corresponding to voltage levels and column index refer to the cycle separator output. Based on these values the switching state is chosen, and the corresponding combination is applied. It is worth mentioning that the developed procedure is independent of the modulation technique. Thus, it can be used for either carrier-based or non-carrier ones. Consider, for example, if $L_3 = 1$, and $C_I = 1$, indicate the output voltage level required to be generated is $V_{\rm dc}/4$ and thus switching combination corresponding to state L_{32^+} is applied as evident from 2.2.

Table 2.2: Binary interpretation of the logic embedded in the switching pulse decoder

L_0	L_1	L_2	L_3	L_4	Switching state to be selected	
					$C_I = 1$	$C_I = 0$
1	0	0	0	0	L_{0+}	L_{0-}
0	1	0	0	0	L_{12+}	L_{11-}
0	0	1	0	0	L_{2+}	L_{2-}
0	0	0	1	0	L_{32+}	L_{31-}
0	0	0	0	1	L_{4+}	L_{4-}

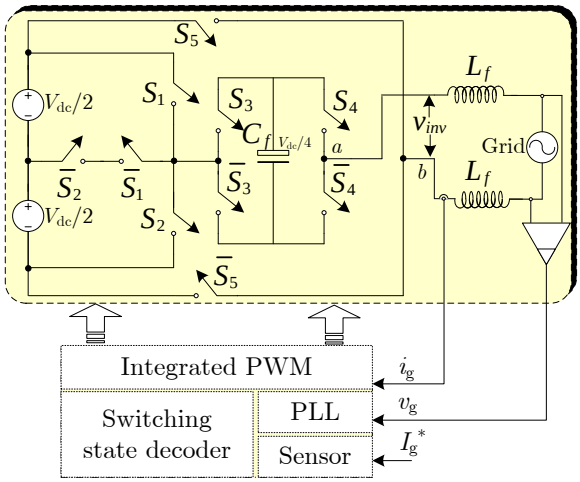


Figure 2.4: Grid-connected setup of the proposed 9L-10S-TNPC MLI

2.5 Simulation and experimental results

2.5.1 Grid-connected mode

Firstly, the proposed MLI is tested for its performance considering a single-phase grid-connected case study. The test setup is shown in Figure 2.4. A simple PR controller is assigned with the job of maintaining the grid current at the set value. In general, the reference current grid i_g^* is derived from the outer dc-link voltage control loop. Since, the focal point of the simulation is to verify the performance of the developed integrated PWM controller for regulating the FC voltage, it is assumed that the dc-link voltage is fixed and hence the dc-link capacitors are replaced with a constant dc source. The entire system is simulated using the MATLAB/Simulink (MATLAB, 2010). The sensed grid voltage template is passed to the grid voltage estimator which produces two output signals; one aligned with the grid voltage ($\sin\theta$) and the other leading the grid voltage by 90^0 ($\cos\theta$) (Zong, 2011). In Figure 2.4, I_g^* is the peak value

Table 2.3: Simulation parameters of the grid-connected setup

Parameter	Value
Power rating	3.5 kVA
dc source voltage (V_{dc})	200 V
Grid voltage (v_g)	230 V(rms)
Grid frequency (f_g)	50 Hz
FC capacitance (C_f)	2.5 mF
Carrier frequency (f_{sw})	2.5 kHz

of grid current to be injected. The reference sinusoidal grid current (i_g^*) is constructed as,

$$i_g^* = I_{g,d}^* \sin(\theta) + I_{g,q}^* \cos(\theta), \tag{2.3}$$

where $I_{g,d}^*$ and $I_{g,q}^*$ are the parallel and orthogonal components of the grid current to be injected. The operating PF of the MLI is given as,

$$\cos(\phi) = \tan^{-1}\left(\frac{I_{g,q}^*}{I_{g,d}^*}\right). \tag{2.4}$$

If the MLI is desired to operate at unity PF, then $I_{g,q}^*$ is set to zero. For any other operating PF, for example, PF = 0.866, and $I_g^* = 20$ A, $I_{g,d}^*$, and $I_{g,q}^*$ are set to 17.32 A and 10 A respectively. Once the i_g^* is constructed, it is compared with the actual grid current and the error is processed through a PR controller to minimize the steady-state error and enables the MLI injected current to track the set reference current. The output of the PR controller is the reference sinusoidal modulation signal which is further sent to the integrated PWM stage. The set values of $I_{g,d}^*$, and $I_{g,q}^*$ controls the active and reactive power exchange between the MLI and grid. The simulation parameters employed are enlisted in Table 2.3.

The developed grid-connected setup is tested under different applicable situations including active power injection mode, reactive power injection/absorbing mode, and transient conditions. Figure 2.5 consolidates the responses of the system under the situations mentioned above. It is to mention that, the grid current and grid voltage waveforms are scaled by a factor of 5 and 0.5 respectively for better visibility. The simulation is carried out considering the following cases:

- Case I: The MLI is operated at unity PF, i.e., $I_{g,q}^* = 0$ A. Initially, $I_{g,d}^* = 15$

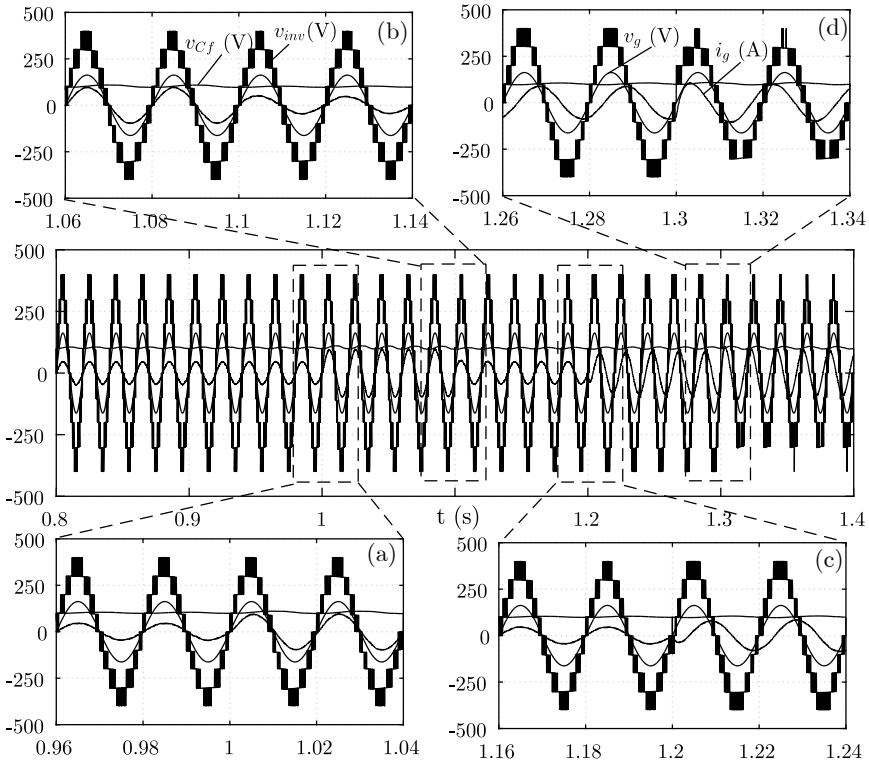


Figure 2.5: Performance of the proposed 9L-10S-TNPC MLI in grid-connected mode

A, and at $t = 1$ s, a step change is applied by increasing its value to 25 A. As evident from the Figure 2.5(a), the injected grid current tracks successfully the set values both in steady-state and transient conditions while remaining in-phase with the grid voltage. Further, at $t = 1.1$ s, the value of $I^*_{g,d}$ is reduced back to 15 A (see Figure 2.5(b)). In both the cases the system response time in tracking the reference value is very minimal. Besides, the MLI generates multilevel output voltage leading to reduced harmonic distortion (THD = 2.3%) in the grid current.

- Case II: The MLI is operated to inject/absorb reactive power in addition to the injection of active power. At $t = 1.2$ s, a step change in $I^*_{g,q}$ is applied from 0 A to -15 A. The negative value of $I^*_{g,q}$ indicates that the MLI generates reactive power. As seen from the Figure 2.5(c) the phase angle of the grid current is adjusted which corresponds to PF of 0.707 (lag) without a significant delay. This indicates the fast dynamic response of the developed integrated PWM. Additionally, at $t = 1.3$ s, the value of $I^*_{g,q}$ is stepped from -15 to 15 A. Without

Table 2.4: System attributes considered for simulation and experiment

Parameter	Value
dc source voltage (V_{dc})	40 V
Fundamental output voltage frequency (f_0)	50 Hz
Capacitance of FC (C_f)	1000 μF
Carrier frequency (f_{sw})	2.5 kHz
Load resistance and inductance (R, L)	30 Ω, 5 mH

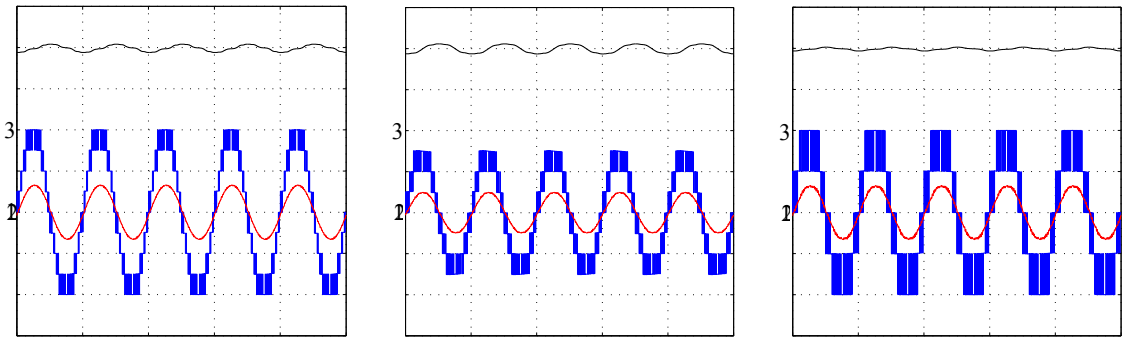
any latency the MLI starts absorbing the reactive power as illustrated in Figure 2.5(d).

It is noteworthy that the voltage across FC remains well regulated around 100 V in all the above cases substantiating the satisfactory operation of the PWM and sensorless control. Due to the high-quality voltage waveform at the output of the MLI, the grid current exhibits lower harmonic content without the need for extra bulky filters.

2.5.2 Stand-alone mode

In this section, in order to observe the consistency in the simulation and experimental results, stand-alone operation of the proposed MLI is considered. In this mode, the MLI is operated to feed power to a passive $R-L$ load, and the values chosen for the simulation and experiments are listed in Table 2.4. Refer Appendix C for the description of the laboratory setup.

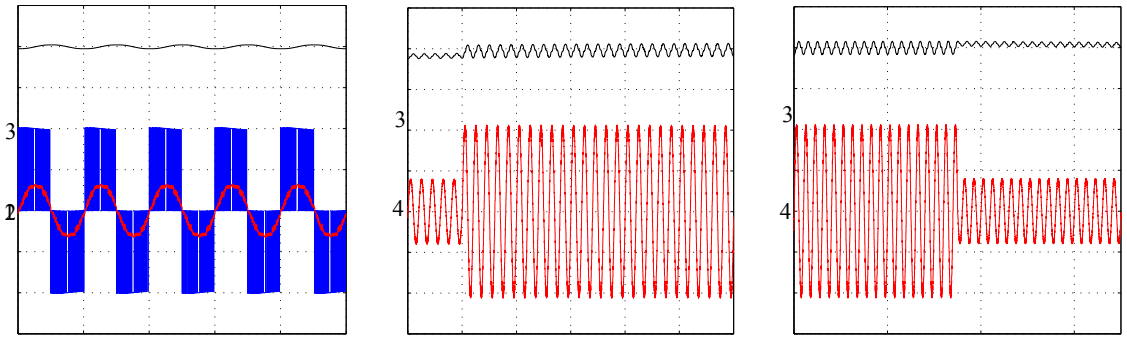
Figure 2.6(a)-(d) and Figure 2.7(a)-(d) shows the simulated and experimental steady state inverter output voltage, voltage across FC and load current for different modulation indices respectively. It is evident from the waveforms that the number of output voltage levels decreases with decreasing modulation index. The dynamic performance of the sensorless voltage control strategy is verified by applying a step change in load. Figure 2.6(e) and (f) shows the corresponding simulation results and Figure 2.7(e) and (f) shows the experimental waveforms. Figure 2.8(a) and Figure 2.9(a) illustrates the response of FC voltage for a rapid 50% increase in dc source amplitude from 20 V to 40 V. It is evident from Figure 2.8(a) and Figure 2.9(a) that the FC voltage remains stabilized at its requisite value (10 V) against variations in the modulation indices. Further, the system is subjected to a rapidly decreasing dc source amplitude, and the results are found satisfactory (see Figure 2.8(b) and Figure 2.9(b)). Moreover, in another test, the FC voltage remains around its reference value



(a) 1:(20V/div), 2:(2A/div), 3:(5V/div), x-axis:10 ms/div

(b) 1:(20V/div), 2:(2A/div), 3:(5V/div), x-axis:10 ms/div

(c) 1:(20V/div), 2:(2A/div), 3:(5V/div), x-axis:10 ms/div

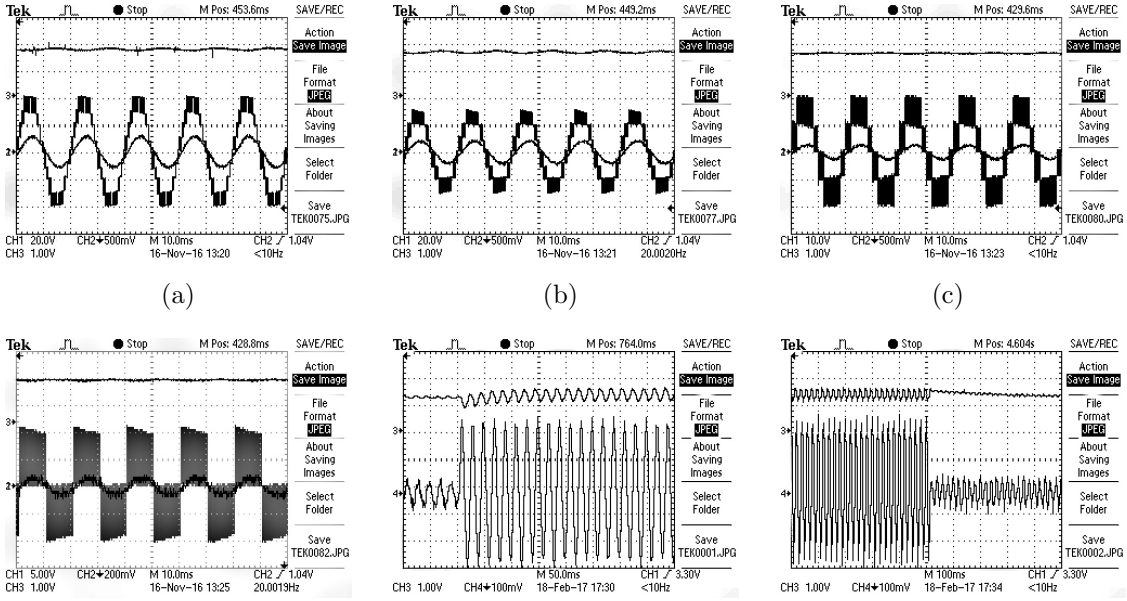


(d) 1:(20V/div), 2:(2A/div), 3:(5V/div), x-axis:10 ms/div

(e) 4:(1A/div), 3:(5V/div), x-axis:100 ms/div

(f) 4:(1A/div), 3:(5V/div), x-axis:100 ms/div

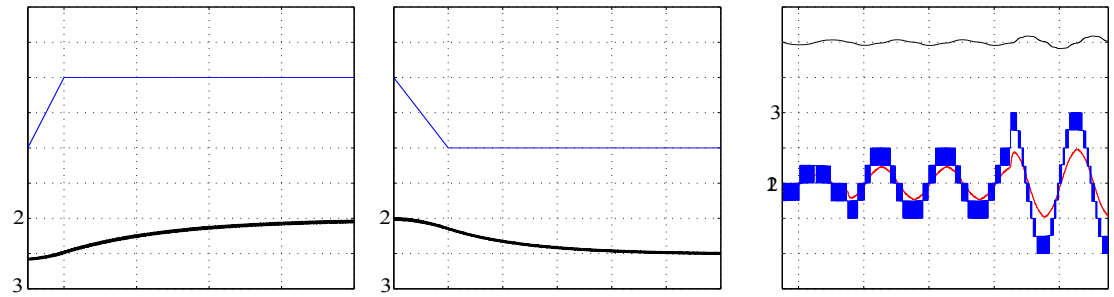
Figure 2.6: Simulation results for (a) 9L (b) 7L (c) 5L (d) 3L (e) step increse in load (f) step decrease in load



(a) (b) (c)

(d) (e) (f)

Figure 2.7: Experimental results for (a) 9L (b) 7L (c) 5L (d) 3L (e) step increse in load (f) step decrease in load

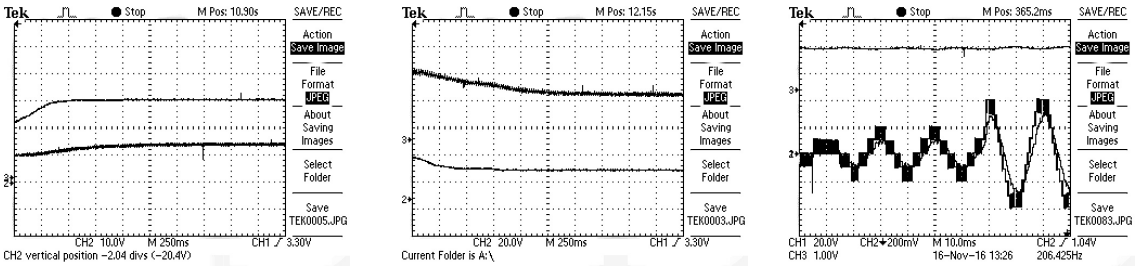


(a) 2:(10V/div), 3:(5V/div), x-axis:250 ms/div

(b) 1:(20V/div), 2:(2A/div), 3:(5V/div), x-axis:20 ms/div

(c) 1:(10V/div), 2:(10V/div), x-axis:5 ms/div

Figure 2.8: Simulation results for (a) rapid increase in dc-link voltage (b) rapid increase in dc-link voltage (c) varying modulation index



(a) (b) (c)

Figure 2.9: Experimental results for (a) rapid increase in dc-link voltage (b) rapid increase in dc-link voltage (c) varying modulation index

despite varying modulation index (see Figure 2.8(c) and Figure 2.9(c)) confirming the correctness of the developed integrated PWM controller. An explicit agreement between the simulation and experimental results is witnessed.

2.6 Hybrid 8S-TNPC MLI topology synthesis

With the underlying principle of the proposed 10S-TNPC MLI, an opportunity for a further reduction in the part count is explored in the current section. With carefull examination of the switching states listed in Table 2.1, it is discerned that the requirement for the switching state $S_3 = 1$, and $S_4 = 0$ never arises in the process of maintaining the natural balancing of FC and producing the multilevel output voltage. In other words, a 2L SC would be sufficient and can readliy replace the FCHB unit. With this notion, a further reduction of two number switches and associated

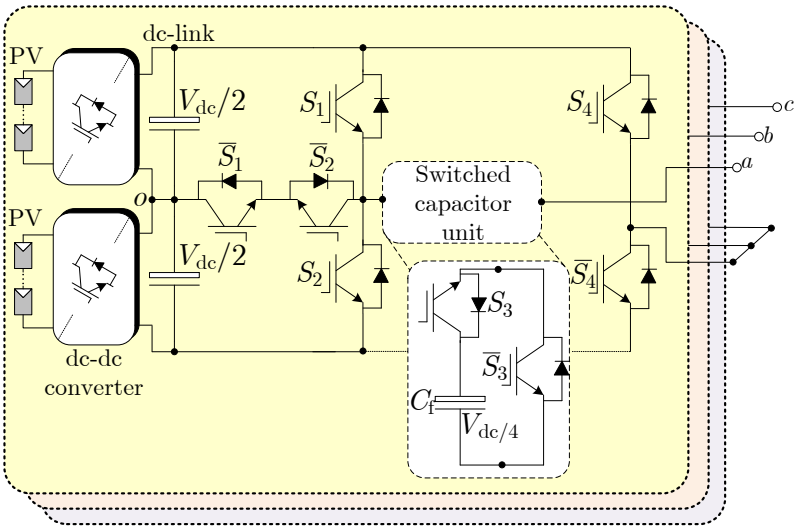


Figure 2.10: Functional diagram of the proposed 9L-8S-TNPC MLI

Table 2.5: Switching states and their effect on FC voltage at each output voltage level of the proposed 8S-TNPC MLI

Voltage levels	S_1	S_2	S_3	S_4	FC voltage
V_{dc}	1	0	0	0	No effect
$3V_{dc}/4$	1	0	1	0	Charging
$V_{dc}/2$	0	0	0	0	No effect
$V_{dc}/4$	0	0	1	0	Charging
0	0/1	1/0	0	0/1	No effect
$-V_{dc}/4$	1	0	1	1	Discharging
$-V_{dc}/2$	0	0	0	1	No effect
$-3V_{dc}/4$	0	0	1	1	Discharging
$-V_{dc}$	0	1	0	1	No effect

gate drivers is achieved effortlessly. Except the replacement of FCHB with a SC unit, the other structural and operating principle remains unaltered. The corresponding switching states are shown in Table 2.5. As like in the previous topology, owing to the cyclic energy balance, the FC voltage remains regulated at the value $V_{dc}/4$ naturally. Unlike the previously discussed look-up table-based sensorless integrated PWM, a LFE-based control strategy is developed for the control of 8S-TNPC MLI.

A fundamental frequency switching PWM is used for the generation of gating pulses. The transition angles are obtained as,

$$\theta_n = \sin^{-1}\left(\frac{2n-1}{N_L}\right), n = 1, 2, ..., \frac{N_L - 1}{2}, 0 \leq \theta_n \leq \frac{\pi}{2}, \tag{2.5}$$

where N_{L} is the number of output voltage levels. Nonetheless, other PWM techniques like selective harmonic elimination or selective harmonic minimization are also equally applicable. The sinusoidal reference voltage ($v_{\mathrm{ref}} = v_m \sin(\omega t)$) generated by the PR controller is used for the pulse modulation. This reference signal is compared with four dc signals which corresponds to the switching angles obtained using one of the above mentioned PWM technique. The output of the comparators is designated as C_1 through C_5. Further, the gating signals for each of the switches is derived using the switching combination listed in Table 2.5 and by applying suitable boolean operation on the comparator outputs to match the generic output voltage shown in Figure 2.11. The rationale behind developing a boolean logic-based switching function of switch S_1 is detailed and using the same, the switching fuctions of remaining switches are constructed. As illustrated in Figure 2.11, switch S_1 is ON for output voltage levels of $3V_{\mathrm{dc}}/4$, V_{dc}, and $-V_{\mathrm{dc}}$. By inspection, it is evident that during the positive half cycle of the output voltage, portion of S_1 is similar to C_3 and during the negative half, it can be constructed using the combination of C_1 and negation of C_2. Thus, the overall switching function is given as,

$$\begin{aligned} S_{F1} &= (C_3 \times \bar{C}_5) + (C_1 \times \bar{C}_2 \times C_5), \\ S_{F2} &= (C_1 \times \bar{C}_2 \times \bar{C}_5) + (C_3 \times C_5), \\ S_{F3} &= (C_1 \times \bar{C}_2) + (C_3 \times \bar{C}_4), \\ S_{F4} &= C_5, \end{aligned} \tag{2.6}$$

where the operators "×" and "+" correspond to logical AND and logical OR operations respectively. It must be remarked that the developed controller with LFE is adaptable for other well established PWM methods and does not involve complex cost function minimization.

2.7 Sizing of the FC

Determining the capacitance of FC is crucial as it contributes the overall size of the converter. With the developed sensorless voltage control, the FC is charged during the positive half cycle of the output voltage and discharged during the negative cycle, a voltage ripple of frequency 50 Hz appears across it. Given the magnitude of allowable ripple voltage (ΔV) which, in general, is chosen to be 5-10% of the nominal voltage

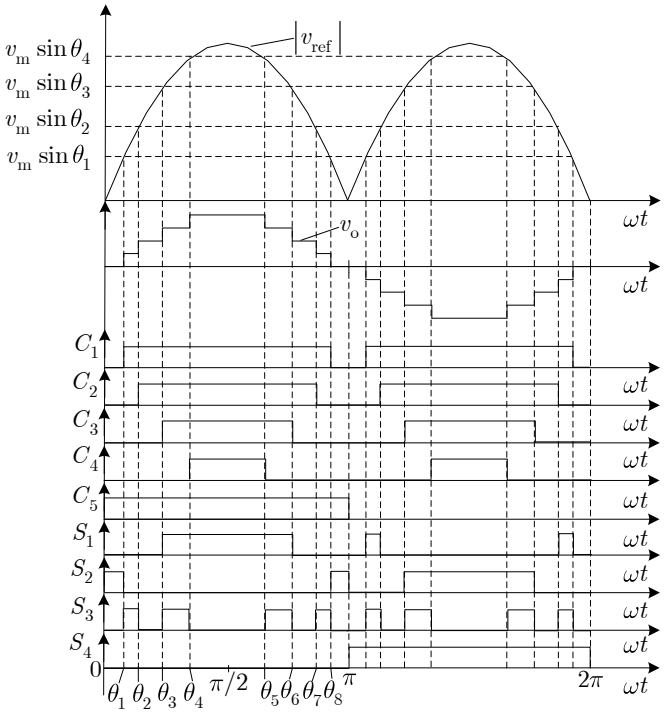


Figure 2.11: Reference voltage, output voltage and gate pulses of the proposed 8S-TNPC MLI operated using fundamental switching method

Table 2.6: System attributes considered for simulation and experiments

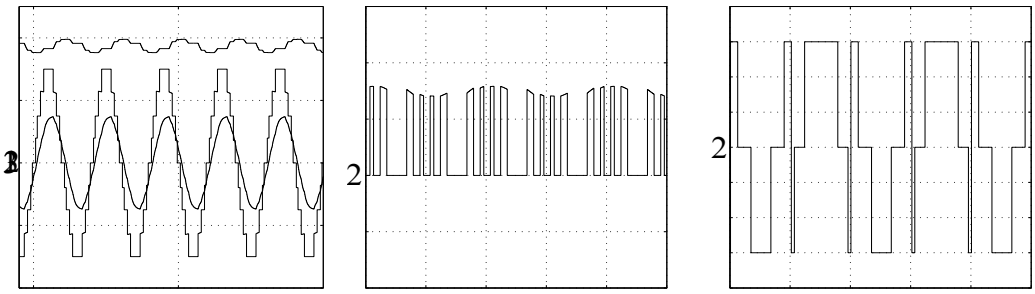
Parameter	Value
dc source voltage ($V_{\rm dc}$)	30 V
Fundamental output voltage frequency (f_0)	50 Hz
Capacitance of FC ($C_{\rm f}$)	1000 μF
Load resistance and inductance (R, L)	30 Ω, 5 mH

across the FC. The capacitance of FC is related to the peak current ($i_{\rm p}$) flowing through it, ΔV and the ripple frequency ($\Delta_{\rm f}$); they are mathematically related as,

$$C_{\rm f} = \frac{i_{\rm p}}{\Delta V \times \Delta_{\rm f}}. \tag{2.7}$$

2.8 Simulation and experimental study

The system parameters considered for the simulation and experimental studies are tabulated in Table 2.6. Waveforms in Figure 2.12(a) and Figure 2.13(a) refers to the simulated and experimentally obtained steady-state output voltage, load current,

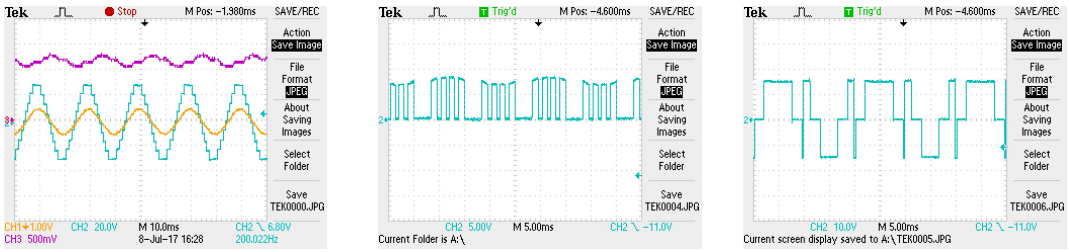


(a) 1:(20V/div), 2:(2A/div), 3:(5V/div), x-axis:50 ms/div

(b) 2:(5V/div), x-axis:10 ms/div

(c) 2:(5V/div), x-axis:10 ms/div

Figure 2.12: Steady state simulation results



(a) v_0, i_0, v_C

(b) v_{SC}

(c) v_{TNPC}

Figure 2.13: Steady state experimental results

and voltage across FC. As apparent from the stipulated results, the MLI generates an output voltage with nine levels, and the voltage across FC is well regulated. The simulated and experimentally measured 2L voltage (0 and V_{dc}) generated by the SC unit is shown in Figure 2.12(b) and Figure 2.13(b) respectively. The 3L voltage (0, $V_{\mathrm{dc}}/2$, and $-V_{\mathrm{dc}}/2$) generated by the TNPC unit shown in Figure 2.12(c) and Figure 2.13(c) corresponds to the simulation and experimentaly obtained waveforms. The experimental results are found to have a close agreement with the simulation waveforms.

2.9 Comparative study

It is customary to compare the developed MLI with other existing prevalent topologies from several aspects to attest the merits of the proposed topology. With this notion, a detailed comparative study is carried out in this section. To have a broader scale of comparison, the classic and recently published reduced part count topologies

are taken into account. The comparison results are tabulated in Table 2.7. It is assumed that number of output voltage levels, peak-to-peak output voltage and rating of the topologies are identical for ensuring an unbiased meaningful comparison. The following figures of merit are considered:

1. *LSR*: The number of switches is a crucial part of the MLI which influences the overall cost. A factor referred to as LSR is calculated by evaluating the ratio of the number of voltage levels to the individual switch number is devised to quantify the competency of a given topology. From the definition of LSR, it is apparent that an MLI that exhibits a higher value of LSR outperforms others. The value of LSR is evaluated for each of the topologies under consideration. The power switch being the weakest link in a power converter from the reliability point of view, it entitles to be critical in ascertaining the merit of the topologies (Yang et al., 2011). According to Table 2.7 the proposed 8S-TNPC MLI has the highest LSR value followed by the 10S-TNPC MLI and topologies in Dargahi et al. (2015), Chaudhuri et al. (2010), Lee et al. (2017) , Sadigh et al. (2010a). Thus, the least value of switch number in the proposed MLI supports the assertion that reliability of the developed topologies is on a higher side and thus is appreciative in comparison to their counterpart topologies.

2. *Number of FCs*: Capacitors being one of the necessary components of a power converter like MLI, thus, is a significant contributor to the overall size, cost, and reliability of the converter. Capacitors being the second vulnerable component, it is desirable to restrict their number in the circuit. Thus, the number of FCs qualifies to be one of the prominent measures of the MLI's merit of competency. From Table 2.7, it is noticeable that both the proposed topologies require only one FC for the 9L voltage generation and is the least value amongnst all.

3. *Number of dc sources*: In general, a lesser number of dc sources is preferred since it aid in reducing the number of transformer windings and rectifier units. For both the proposed topology two number of isolated power supply suffices the circuit operation and thus has a better performance.

4. *VDF*: It is to remark that, in addition to the number of capacitors, their voltage ratings, and diversity profoundly influence the size and cost of the converter.

The VDF is devised to attribute such an effect numerically and is given as,

$$\text{VDF} = \frac{\sum_{i=1}^{k} V_{\text{C}k}}{V_{\text{dc}}}, k = 1, 2, ..., \text{m}, \tag{2.8}$$

where "m" is the number of capacitors with distinct voltage ratings. Further, the energy stored in the capacitors is given as,

$$E_{\text{C}_\text{f}} = \frac{1}{2} \times C_{\text{f}} \times V_{\text{C}_\text{f}}^2. \tag{2.9}$$

Using (2.7), (2.9) is rewritten as,

$$E_{\text{C}_\text{f}} = \frac{1}{2} \times \frac{i_{\text{p}}}{\Delta V \times \Delta_{\text{f}}} \times V_{\text{C}_\text{f}}^2, \tag{2.10}$$

where V_{C_f} is the voltage across C_f. Since i_{p} is assumed identical, the stored energy has a positive correlation with the voltage across FC. Thus, in this regard also the proposed topologies outperform others since the voltage across FC is only $V_{\text{dc}}/4$. Therefore, the energy associated with the proposed topologies is substantially less, leading to a compact structure of the converter.

5. *TBV*: The blocking voltage of a semiconductor device is an indicator of the silicon requirement, losses, and cost of the power converter. As it is evident from Table 2.7, the proposed topologies have an improved performance owing to their least blocking voltage requirement.

Overall, the proposed topologies exhibit an improved performance. However, with regard to the requirement of four number of switches to be rated to withstand full dc-link voltage for 9L output voltage, both the proposed topologies are recommended for LV application fields. The commercial availability of IGBTs of rating 1.2 kV to 1.7 kV enables their successful application. However, for applications of MV range, another family of hybrid topologies is introduced in the next chapter.

Table 2.7: Comparison of the proposed TNPC-based hybrid MLIs with other topologies

	Multilevel inverter type													
	1	2	3	4	5	6	7	8	9	10	11	12	**10S- TNPC**	**8S-TNPC**
LSR	0.56	0.75	0.9	0.64	0.64	0.75	0.56	0.9	0.75	0.64	0.9	0.9	**0.9**	**1.125**
No. of FCs	-	2	2	2	2	3	-	2	3	3	0	3	**1**	**1**
No. of DC sources	8	2	1	2	2	2	4	2	2	2	4	1	**2**	**2**
VDF	-	0.75	0.75	0.75	0.75	0.375	-	0.58	3	0.625	-	1.5	**0.25**	**0.25**
TBV (p.u.)	6	7	3.5	7.5	9	3.5	6	8	6	4	6.5	4	**2.5**	**2**
% Device reduction	37.5	16.66	0	28.57	28.57	16.66	37.5	0	16.66	28.57	20	20	**20**	-
No. of sensors	-	3	0	3	3	4	-	3	4	4	0	0	**0**	**0**

1. Nabae et al. (1981)
2. Li et al. (2011)
3. Dargahi et al. (2015)
4. Chaudhuri et al. (2007)
5. Veenstra and Rufer (2005)
6. Rajeevan et al. (2013)
7. Marchesoni et al. (1990)
8. Chaudhuri et al. (2010)
9. Barbosa et al. (2005)
10. Viju et al. (2017)
11. Lee et al. (2017)
12. Sadigh et al. (2010a)

Chapter 3

HYBRID ANPC CONVERTER

3.1 Introduction

In the previous chapter, TNPC-based hybrid MLIs with reduced part count and sensorless control were presented. The suitability of those topologies is found pertinent to LV application fields. In this chapter, the same principle is extended to ANPC converter family for MV level applications. Unlike sensorless control, an uncomplicated sensor-based voltage balancing with LFE is developed for the converter control.

This chapter is organized as follows: Firstly, the topological details of the proposed hybrid ANPC topology is described, followed by the developed sensor-based PWM strategy. Secondly, an improved version of the presented hybrid ANPC topology is introduced. Further, the simulation and experimental results pertaining to both the circuits are provided with a detailed comparative evaluation.

3.2 Problem formulation

The advent of ANPC MLI has outdone the use of NPC MLI for MV applications (Barbosa et al., 2005). For 9L output voltage, it requires three flying capacitors with voltage ratio 1:2:3 with respect to half the dc-link voltage. These capacitor voltages are to be balanced using a dedicated voltage controller. Though efforts are made in devising ANPC-based novel topologies to negate the detriment of a higher number of capacitors and switches; such an effort calls for a total structural disruption and reconfiguration.

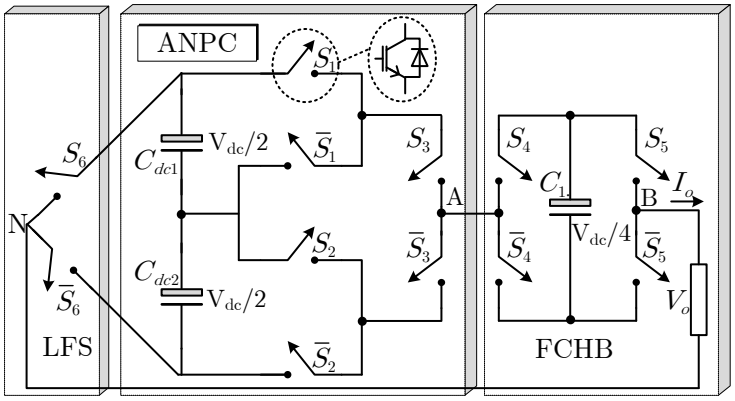


Figure 3.1: Functional diagram of the proposed 9L-12S-ANPC MLI

On this line, with a motivation to synthesize an MLI capable of generating nine levels while retaining the pertinent characteristics of an ANPC MLI (high reliability and power density), two new topologies are proposed.

3.3 Hybrid 12S-ANPC MLI topology synthesis

The process of devising a 9L hybrid ANPC MLI is inducted by considering the 3L-ANPC MLI as the fundamental building block. Further, the 3L-FCHB and the 2L converter leg are appended as shown in Figure 3.1. The functionality of each of these units are as follows:

- 3L-ANPC MLI: Capable of generating three distinct voltage levels (0, -$V_{\rm dc}/2$, and $V_{\rm dc}/2$). It consists of three pair of complementary switches.
- 3L-FCHB: Capable of generating three distinct voltage levels (0, -$V_{\rm dc}/4$, and $V_{\rm dc}/4$). It comprises two pair of complementary switches and one FC.
- 2L converter leg: Capable of generating two distinct voltage levels (-$V_{\rm dc}$, and $V_{\rm dc}$). It consists of a single pair of complementary LFS.

Contrary to the use of a 3L-NPC in cascade with FCHB as presented in (Steimer and Veenstra, 2003, Veenstra and Rufer, 2005), the proposed work connects a 3L-ANPC with FCHB. In addition, a 2L converter leg appended, eventually leads to doubling of the number of the voltage levels to nine which otherwise will be five. It must also be remarked that owing to the deficiency of redundant switching states,

Table 3.1: Switching states and their effect on the FC Voltage of the proposed 12S-ANPC MLI

Switching state	ANPC switches			FCHB switches		LFS	Output voltage	FC
	S_1	S_2	S_3	S_4	S_5	S_6		$I_0 > 0$
V_1	1	0	1	**0**/1	**0**/1	0	V_{dc}	-
V_2	1	0	1	1	0	0	$3V_{\mathrm{dc}}/4$	C
V_3	0	**1**/0	**0**/1	0	1	0	$3V_{\mathrm{dc}}/4$	D
V_4	0	1/**0**	0/**1**	**0**/1	**0**/1	0	$V_{\mathrm{dc}}/2$	-
V_5	0	**1**/0	**0**/1	1	0	0	$V_{\mathrm{dc}}/4$	C
V_6	0	0	0	0	1	0	$V_{\mathrm{dc}}/4$	D
V_7	**0**/1	**0**/1	**0**/1	**0**/1	**0**/1	**0**/1	0^+	-
V_8	0/**1**	0/**1**	0/**1**	0/**1**	0/**1**	0/**1**	0^-	-
V_9	0	0/**1**	1/**0**	0	1	1	$-V_{\mathrm{dc}}/4$	D
V_{10}	1	0	1	1	0	1	$-V_{\mathrm{dc}}/4$	C
V_{11}	0	**0**/1	**1**/0	0/**1**	0/**1**	1	$-V_{\mathrm{dc}}/2$	-
V_{12}	0	0	0	0	1	1	$-3V_{\mathrm{dc}}/4$	D
V_{13}	0	0/**1**	1/**0**	1	0	1	$-3V_{\mathrm{dc}}/4$	C
V_{14}	0	0	0	0/**1**	0/**1**	1	$-V_{\mathrm{dc}}$	-

complex controller like model predictive control (Steimer and Veenstra, 2003) and fuzzy logic controller (Veenstra and Rufer, 2005) are employed. The notable features of the proposed hybrid ANPC-based MLIs are:

1. It requires lesser components for the generation of the same number of voltages levels.

2. The modification identified is to add a 2L converter leg while the precursor ANPC and FCHB is retained without any alteration.

3. The redundant switching states are self-sufficient to maintain the FC voltage, and unlike the proposed TNPC-based topologies, the dc-link is made up of capacitor voltage divider network. Since the power sourced by both the capacitors is identical, the voltage across them is naturally balanced.

4. For a given number of voltage levels and output peak-to-peak voltage value, the required number of dc sources and their magnitudes are halved.

Table 3.1 summarizes all the possible output voltage levels and the switching combinations ("0" for OFF and "1" for ON state of a switch) that can be generated

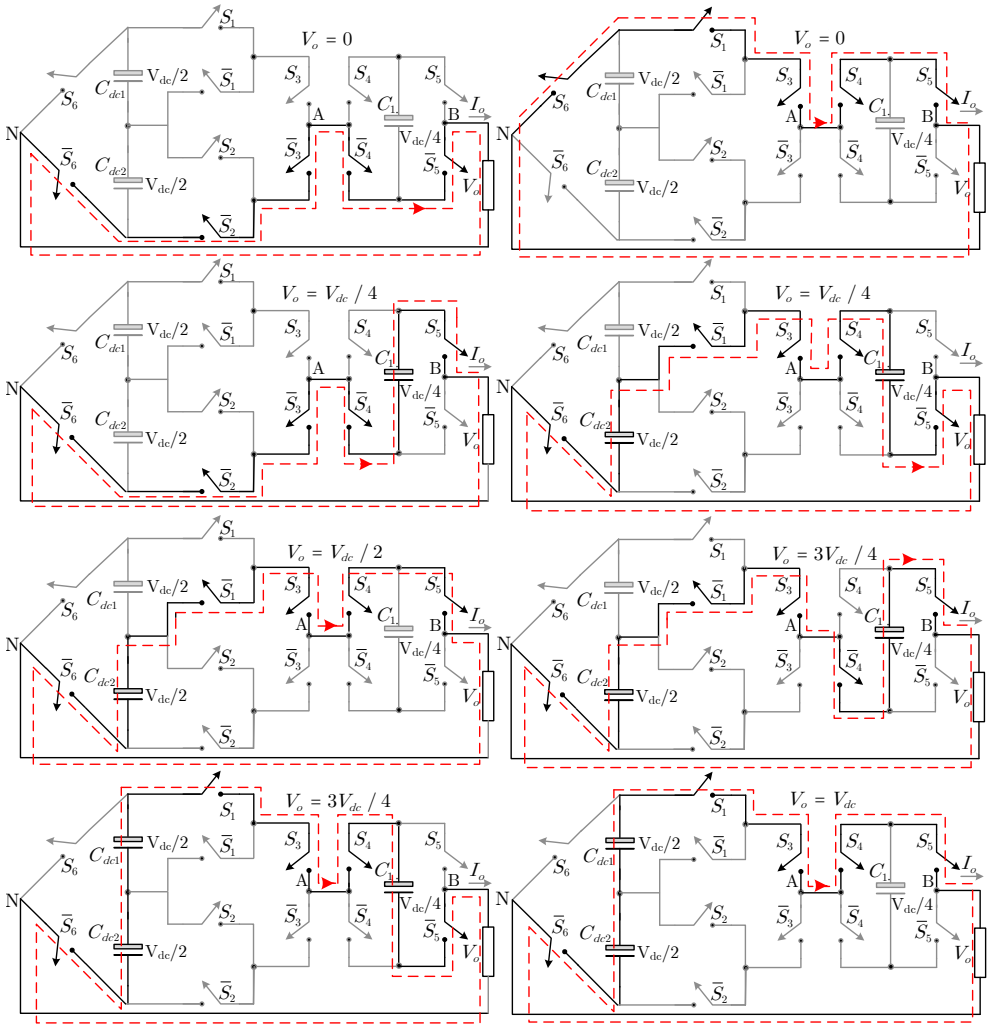


Figure 3.2: Operating modes of the proposed 9L-12S-ANPC MLI during positive half cycle of the output voltage

with the topology. While maintaining the FC voltage to half the dc-link voltage, nine levels of the output voltage can be synthesized with a provision to have enough charging and discharging states for FC. Further, to have a comprehensive understanding of these switching states, path for the load current, active switches and the effect of each state on FC voltage are shown in Figure 3.2 (only for positive half cycle of the output voltage). As evident from Table 3.1 and Figure 3.2 there exist sufficient redundancies to ensure the regulation of FC voltage.

3.4 LFE-based FC voltage balancing strategy

Different to sensorless voltage balancing mechanism presented in Chapter 2, the FC voltage is regulated instantaneously with the help of LFE-based voltage controller. Unlike the conventional methods, the authors in (Khoshkbar-Sadigh et al., 2016, Sadigh et al., 2016) have developed the LFE-based voltage balancing for the first time. However, the use of high-frequency multicarrier signals is employed for the generation of reference voltage steps. Contrary to this, a single carrier is used in this proposed work.

Firstly, the sensed FC voltage (V_{C1}) is compared with the reference value (V_{C1}^{*}), and the error is processed through a hysteresis controller. The output of hysteresis controller, from now on, H_1 has two distinct values; "1" indicating that the FC voltage is lesser than the reference value and thus needs charging and "0" for vice versa given as,

$$H_1 = \begin{cases} 1, & \Delta V_{\mathrm{C1}} \geq \mathrm{UB} \\ 0, & \Delta V_{\mathrm{C1}} < \mathrm{LB} \end{cases} \tag{3.1}$$

where $\Delta V_{\mathrm{C1}} = V_{\mathrm{C1}}^{*} - V_{\mathrm{C1}}$, UB and LB stands for upper band and lower band limit of the hysteresis controller. It is to note in Table 3.1, that the effect of each state on FC voltage is tabulated assuming that the load current is flowing out of the converter. Thus it is vital to have the information on the polarity of the converter current for the exercise of appropriate switching state. Therefore, a zero crossing detector, from now on, I_{dir} is employed and is given as,

$$I_{\mathrm{dir}} = \begin{cases} 1, & I_0 > 0 \\ 0, & I_0 < 0. \end{cases} \tag{3.2}$$

Secondly, binary interpretation of the comparison outputs (C_1 through C_5) of the reference sinusoidal signals and the carrier signal is carried out (refer Table 3.2). The data in Table 3.2 is stored as a lookup table. It is to be read as follows; if $C_3\bar{C}_4 = 1$ and $Z_c = 1$, then the output voltage level to be generated is $3V_{\mathrm{dc}}/4$. With this background, the procedure for developing a LFE-based switching function is described further. Only those output voltage levels (in Table 3.1) where the entry for a particular switch is "1" are considered.

1. Switching function of S_1: S_1 is ON for positive output voltage levels $3V_{\mathrm{dc}}$ and

Table 3.2: Binary interpretation of individual comparator outputs and the output voltage level

Level (p.u.)	$\bar{C}_1$	$C_1\bar{C}_2$	$C_2\bar{C}_3$	$C_3\bar{C}_4$	C_4	Z_c
+4	0	0	0	0	1	1
+3	0	0	0	1	0	1
+2	0	0	1	0	0	1
+1	0	1	0	0	0	1
0	1	0	0	0	0	-
-1	0	1	0	0	0	0
-2	0	0	1	0	0	0
-3	0	0	0	1	0	0
-4	0	0	0	0	1	0

V_{dc}. Since S_1 is to be ON during the voltage level V_{dc}, the term C_4 is to be included. Coming to voltage level $3V_{\mathrm{dc}}$, S_1 is ON when the FC needs charging and if one of the following conditions are fulfilled

- $I_{\mathrm{dir}} = 1$ and $H_1 = 1$ which equals $I_{\mathrm{dir}} \cdot H_1$.
- $\bar{I}_{\mathrm{inv,dir}} = 1$ and $\bar{H}_1 = 1$ which equals $\bar{I}_{dir} \cdot \bar{H}_1$.

The above condition are logically expressed as $I_{\mathrm{dir}} \cdot H_1 + \bar{I}_{dir} \cdot \bar{H}_1$. Since it is applicable only during voltage level $3V_{\mathrm{dc}}/4$, the term $C_3\bar{C}_4Z_c$ is multiplied with it. The same principle is applicable during the negative half cycle as well.

2. Switching function of S_2: S_2 is ON for positive output voltage levels $V_{\mathrm{dc}}/4$ and $3V_{\mathrm{dc}}/4$. The term to be included for voltage level $V_{\mathrm{dc}}/4$ is same as that of S_1. Coming to voltage level $3V_{\mathrm{dc}}/4$, S_2 is ON when the FC needs charging and if one of the following conditions is fulfilled.

   - $I_{\mathrm{dir}} = 1$ and $\bar{H}_1 = 1$ which equals $I_{\mathrm{dir}} \cdot \bar{H}_1$.
   - $\bar{I}_{\mathrm{dir}} = 1$ and $H_1 = 1$ which equals $\bar{I}_{\mathrm{dir}} \cdot H_1$.

   The above condition are logically expressed as $I_{\mathrm{dir}} \cdot \bar{H}_1 + \bar{I}_{\mathrm{dir}} \cdot H_1$. Since it is applicable only during voltage level $3V_{\mathrm{dc}}/4$, the term $C_3\bar{C}_4Z_c$ is multiplied with it. The same principle is applied during the negative half cycle as well.

The switching functions derived using the principle underlined above for all the six

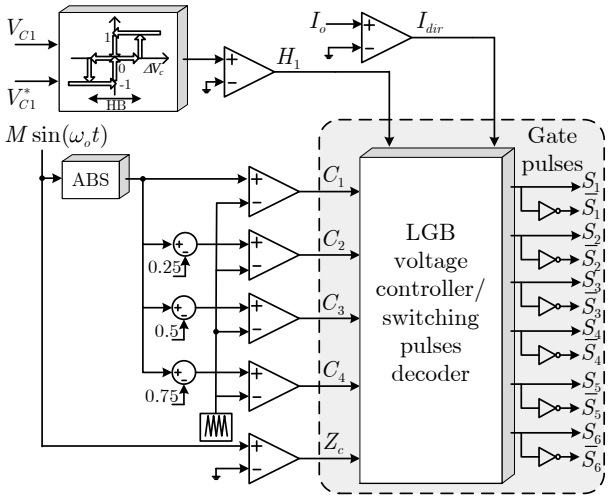


Figure 3.3: LFE based PWM controller with integrated FC voltage balancing mechanism

switches is as follows:

$$S_{F1} = \Big(X_2 \cdot \big[C_3\bar{C}_4Z_c + C_1\bar{C}_2\bar{Z}_c\big]\Big) + C_4Z_c \tag{3.3}$$

$$S_{F2} = \Big(X_1 \cdot \big[C_1\bar{C}_2Z_c + C_3\bar{C}_4\bar{Z}_c\big]\Big) + \Big(X_2 \cdot \big[C_3\bar{C}_4Z_c + C_1\bar{C}_2\bar{Z}_c\big]\Big) \tag{3.4}$$

$$S_{F3} = \Big(X_1 \cdot \big[C_3\bar{C}_4Z_c + C_1\bar{C}_2\bar{Z}_c\big]\Big) + C_2\bar{C}_3 + C_4Z_c \tag{3.5}$$

$$S_{F4} = \Big(X_1 \cdot \big[C_1\bar{C}_2 + C_3\bar{C}_4\big]\Big) + C_2\bar{C}_3Z_c + C_4\bar{Z}_c \tag{3.6}$$

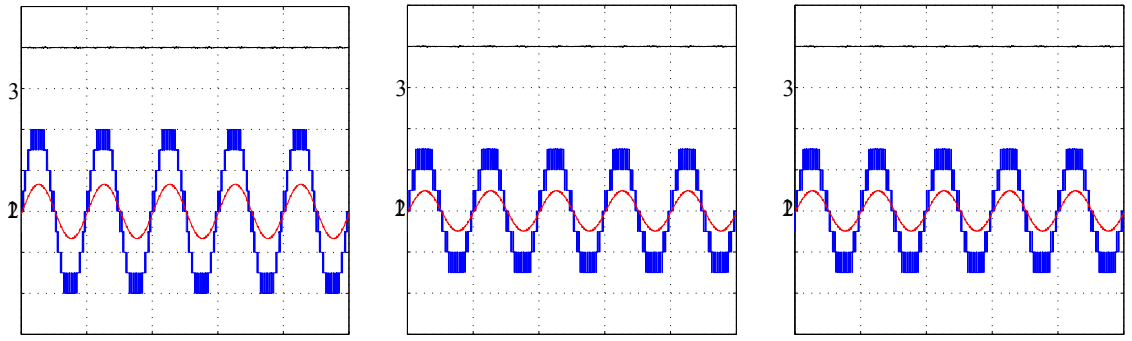
$$S_{F5} = \Big(X_2 \cdot \big[C_1\bar{C}_2 + C_3\bar{C}_4\big]\Big) + C_2\bar{C}_3Z_c + C_4\bar{Z}_c \tag{3.7}$$

$$S_{F6} = \bar{Z}_c \tag{3.8}$$

where, $X_1 = (I_{\text{dir}} \cdot \bar{H}_1 + \bar{I}_{\text{dir}} \cdot H_1)$ and $X_2 = (\bar{I}_{\text{dir}} \cdot \bar{H}_1 + I_{\text{dir}} \cdot H_1)$. The integrated FC voltage balancing mechanism with a single carrier PWM controller embedding the above set of equations is shown in Figure 3.3.

3.5 Simulation and experimental results

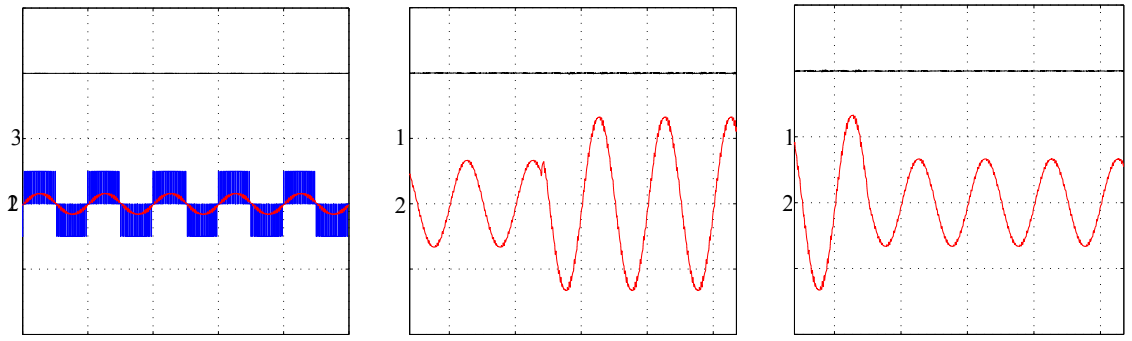
The developed LFE along with the proposed 9L-12S-ANPC MLI is simulated using MATLAB/Simulink. The system parameters employed are same as that of used for the simulation study in Chapter 2. Figure 3.4(a)-(d) and Figure 3.5(a)-(d) shows the



(a) 1:(20V/div), 2:(2A/div), 3:(10V/div), x-axis:10 ms/div

(b) 1:(20V/div), 2:(2A/div), 3:(10V/div), x-axis:10 ms/div

(c) 1:(20V/div), 2:(2A/div), 3:(10V/div), x-axis:10 ms/div

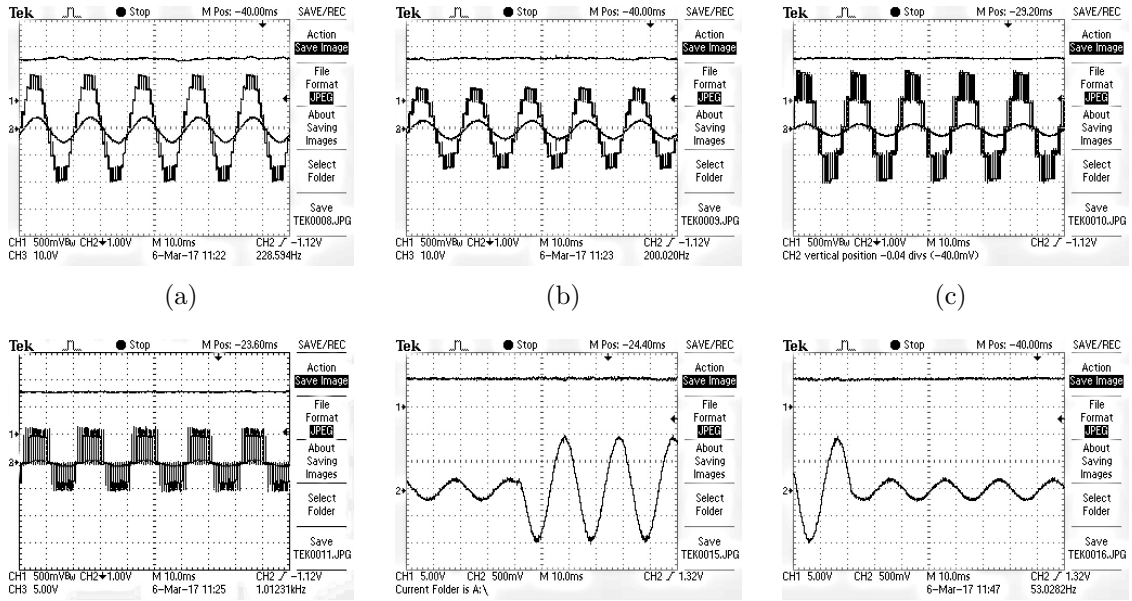


(d) 1:(20V/div), 2:(2A/div), 3:(10V/div), x-axis:10 ms/div

(e) 4:(1A/div), 3:(10V/div), x-axis:100 ms/div

(f) 4:(1A/div), 3:(10V/div), x-axis:100 ms/div

Figure 3.4: Simulation results for (a) 9L (b) 7L (c) 5L (d) 3L (e) step increse in load (f) step decrease in load



(a) (b) (c)

(d) (e) (f)

Figure 3.5: Experimental results for (a) 9L (b) 7L (c) 5L (d) 3L (e) step increse in load (f) step decrease in load

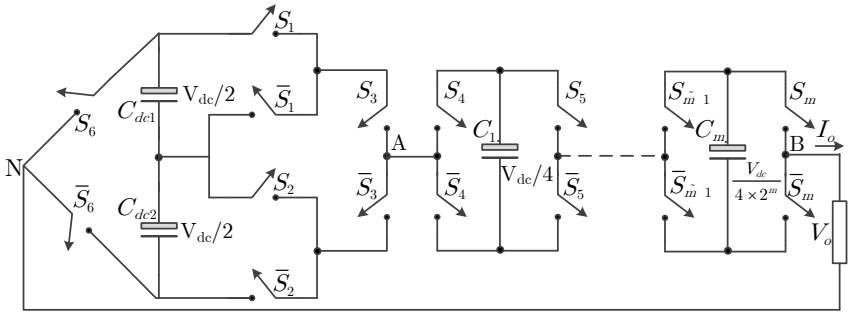


Figure 3.6: Proposed extension based on method-1

simulated and experimental steady state inverter output voltage, voltage across FC and load current for different values of modulation index respectively. Following a step change in load, the load current increases as shown in Figures 3.4(e) and 3.5(e) while the voltage across FC remains intact. Also, unlike sensorless control, the FC voltage does not possess an increased voltage ripple since the control is exercised at every switching period. Same is the response to a step decrease in load (see Figures 3.4(f) and 3.5(f)). An explicit agreement between the simulation and experimental results is witnessed.

3.6 Methods to extend the proposed 12S-ANPC MLI topology

For generating a higher number of voltage levels (>9), two methods are proposed in this section.

3.6.1 Method-1

Adding more number of FCHBs in cascade enables the proposed topology to produce more number of output voltage levels as shown in Figure 3.6. The relation between the number of FCHBs (m) and the number of voltage levels (N_{L}) is given as,

$$N_{\mathrm{L}} = (8 \times 2^{\mathrm{m}-1}) + 1. \tag{3.9}$$

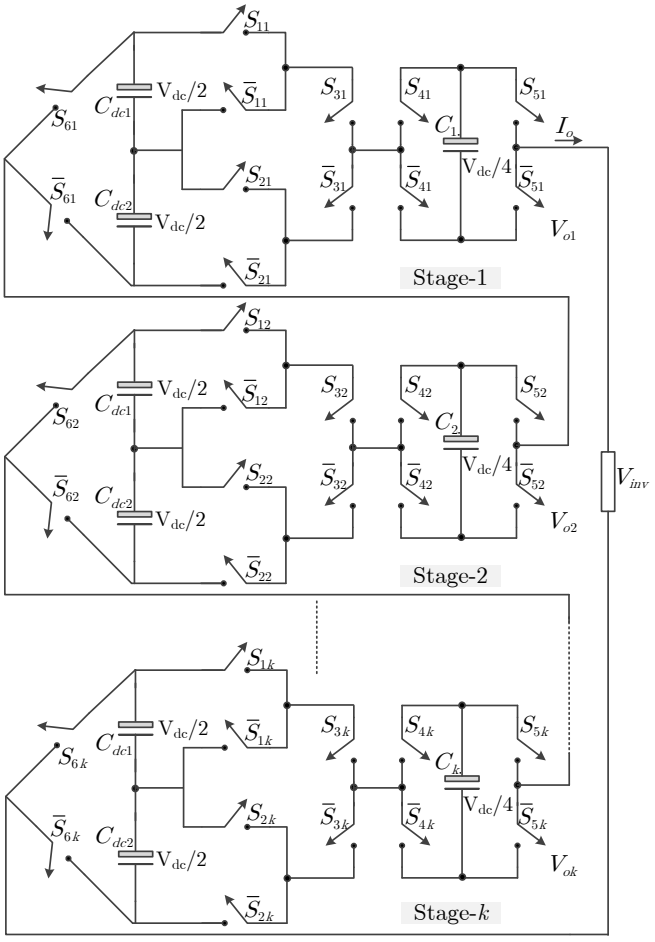


Figure 3.7: Proposed extension based on method-2

The voltage across the appended FCs of the FCHBs are to be regulated to the value obtained by using,

$$V_{Cn} = \frac{V_{\mathrm{dc}}}{4 \times 2^{n-1}}, n = 1, 2, 3, \cdots, \mathrm{m}. \tag{3.10}$$

As a consequence of such an addition, the topology is modular and easily scalable. Which also translates in higher reliability since failure in any of the FCHB will not shut down the entire MLI instead enables it to operate at a lower number of voltage levels by bypassing the defective cell(s).

3.6.2 Method-2

In this method, a facility to integrate multiple sources is achieved by considering the proposed 9L topology as a fundamental MLI unit connected in cascade as shown in

Figure 3.7. The voltage across the multiple dc-links is designated as V_{dc1}, V_{dc2}, $\cdots$, $V_{\mathrm{dc}k}$. The total output voltage is the sum of individual 9L-12S-ANPC MLI outputs expressed as,

$$V_{\mathrm{inv}} = V_{o1} + V_{o2} + \cdots + V_{ok}. \tag{3.11}$$

Based on the ratio of dc-link voltages of each cascaded subsystem, the overall MLI can operate in two modes namely

- Symmetric mode: The ratio of the total dc-link voltage of each cascade unit is equal to one in this mode. In other words $V_{\mathrm{dc1}} = V_{\mathrm{dc2}} = \cdots = V_{\mathrm{dc}k} = V_{\mathrm{dc}}$. The value of N_{L} is same as that of configuration in method-1.

- Asymmetric mode: The ratio of the total dc-link voltage of each cascade units varies in the order of two. In other words $V_{\mathrm{dc1}} = 2^0 \times V_{\mathrm{dc}}, V_{\mathrm{dc2}} = 2^1 \times V_{\mathrm{dc}} = \cdots = V_{\mathrm{dc}k} = 2^k \times V_{\mathrm{dc}}$. The value of N_{L} is calculated as,

$$N_{\mathrm{L}} = \left(2 \times \frac{V_{\mathrm{inv,max}}}{V_{C1}}\right) + 1. \tag{3.12}$$

  where $V_{\mathrm{inv,max}} = \sum_{i=1}^{k} 2 \times V_{\mathrm{dc}i}$.

3.7 Hybrid 10S-ANPC MLI topology: operation and control

In this section with the same concept of adding a 2L converter leg another variant of ANPC MLI is derived. For this, instead of cascading a 3L-FCHB to a 3L-ANPC, a standard 5L-ANPC is considered. The objective is to devise a method for upgrading 5L-ANPC to 9L with minimum topological modifications. Authors (Li et al., 2011) have connected a 3L-FCHB to the output of 5L-ANPC MLI resulting in the 9L output voltage and is considered to be one of the most feasible solutions. However, an alternate way to achieve the same with a reduced number of components in comparison to that used by (Li et al., 2011) is the principle motivation. The topology so developed is shown in Figure 3.8. It comprises of a standard 5L-ANPC MLI and a 2L converter leg. The following are a few pertinent distinctive features in comparison to other topologies bearing the same idea.

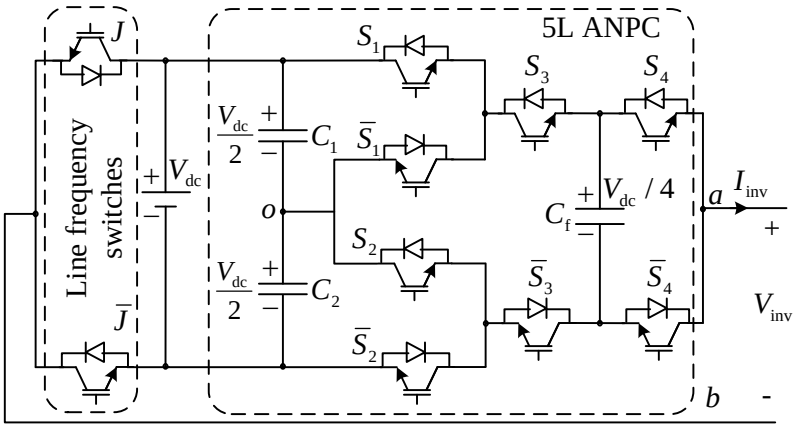


Figure 3.8: Functional diagram of the proposed 9L-10S-ANPC MLI

1. The 5L-ANPC topology is commercially available as ACS5000 and thus reduces the potential technical risk associated with the innovation suggested.

2. The proposed modification only needs the appending of two switches while no amendments on the precursor circuit configuration are required.

3. The voltage across the inherent FC of the 5L-ANPC can be regulated using the redundant switching states. Besides, the balancing of the dc-link capacitors is preserved.

The various output voltage levels are generated by adding the voltage across the dc-link capacitors and FC. Using the switching combinations as listed in Table 3.3 the multilevel output voltage is synthesized. The influence of each switching state on the FC voltage are analyzed to select an appropriate combination for maintaining the FC voltage at reference value. The operating mode during the positive half cycle of the output voltage are as follows:

1. *Zero output*: Two switching combinations are available for generation of this level: all the lower switches are ON or all the upper switches are ON. In both the cases, the load terminal *ab* is short circuited, and the voltage across load is zero.

2. *One-fourth positive output*: Two switching combinations are available for generation of this level: switches $\bar{J}, \bar{S}_2, \bar{S}_3$ and S_4 are ON or switches $\bar{J}, \bar{S}_1, S_3$ and $\bar{S}_4$ are ON, resulting in a voltage of $V_{\mathrm{dc}}/4$ across the load terminal *ab*.

Table 3.3: Switching states and their effect on the FC voltages of the proposed 10S-ANPC MLI

	Power switches state					Output voltage	ΔV_{C_f}	
	S_1	S_2	S_3	S_4	J	(V_{inv})	$I_{\text{inv}}>0$	$I_{\text{inv}}<0$
V_1	0	0	0	0	0	0	-	-
V_2	1	1	1	1	1	0	-	-
V_3	0	0	0	1	0	$V_{\text{dc}}/4$	$\downarrow$	$\uparrow$
V_4	0	0	1	0	0	$V_{\text{dc}}/4$	$\uparrow$	$\downarrow$
V_5	0	0	1	1	0	$V_{\text{dc}}/2$	-	-
V_6	1	1	0	1	0	$3V_{\text{dc}}/4$	$\downarrow$	$\uparrow$
V_7	1	1	1	0	0	$3V_{\text{dc}}/4$	$\uparrow$	$\downarrow$
V_8	1	1	1	1	0	V_{dc}	-	-
V_9	0	0	0	0	1	-V_{dc}	-	-
V_{10}	0	0	0	1	1	-$3V_{\text{dc}}/4$	$\uparrow$	$\downarrow$
V_{11}	0	0	1	0	1	-$3V_{\text{dc}}/4$	$\downarrow$	$\uparrow$
V_{12}	1	1	0	0	1	-$V_{\text{dc}}/2$	-	-
V_{13}	1	1	0	1	1	-$V_{\text{dc}}/4$	$\uparrow$	$\downarrow$
V_{14}	1	1	1	0	1	-$V_{\text{dc}}/4$	$\downarrow$	$\uparrow$

3. *One-half positive output*: Switches $\bar{J}, \bar{S}_1, S_3$ and S_4 are ON, connecting terminal a to midpoint of dc-link and terminal b to negative of dc-link resulting in a voltage of $V_{\text{dc}}/2$ across the load terminal ab.

4. *Three-fourth positive output*: Two switching combinations are available for generation of this level: switches $\bar{J}, S_2, \bar{S}_3$ and S_4 are ON or switches $\bar{J}, S_1, S_3$ and $\bar{S}_4$ are ON, resulting in a voltage of $3 \times V_{\text{dc}}/4$ across the load terminal ab.

5. *Maximum positive output*: Switches $\bar{J}, S_1, S_3$ and S_4 are ON, connecting terminal a to positive of dc-link and terminal b to negative of dc-link resulting in a voltage of V_{dc} across the load terminal ab.

As it can be seen, not at every level of output voltage there exists redundancy, and thus the FC voltage is affected with only a few switching states. Using the same principle describe in Section 3.4, the LFE developed for the proposed 10S-ANPC

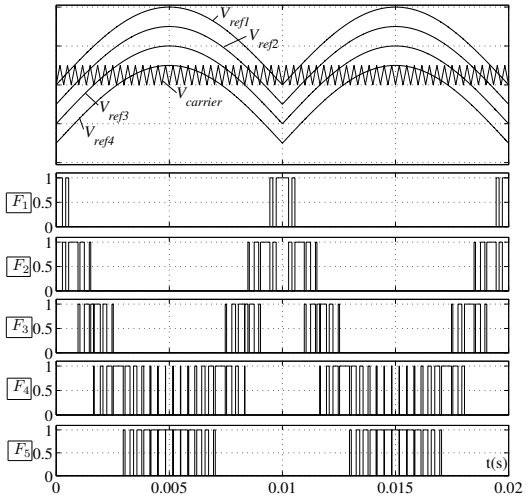


Figure 3.9: Multicarrier PWM signals

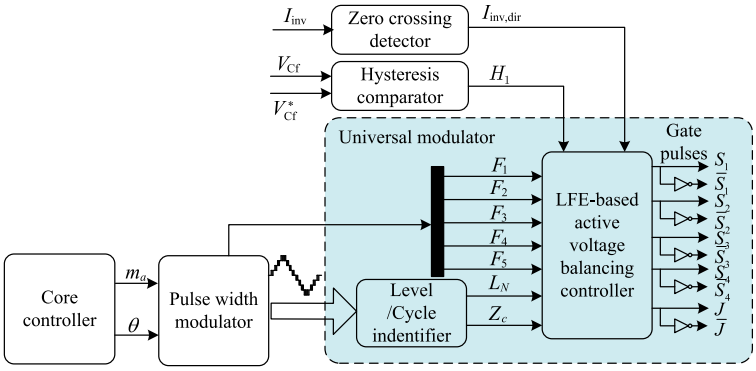


Figure 3.10: PWM generation scheme with integrated FC voltage balancing mechanism

MLI are as follows:

$$S_{F1} = (F_4 + F_5) \cdot Z_c + (F_1 + F_2) \cdot \bar{Z}_c \tag{3.13}$$

$$S_{F2} = S_{F1} \tag{3.14}$$

$$S_{F3} = X_2 \cdot [F_2 + F_4] + F_3 + F_5) \cdot Z_c + X_1 \cdot [F_2 + F_4] + F_5) \cdot \bar{Z}_c \tag{3.15}$$

$$S_{F4} = X_1 \cdot [F_2 + F_4] + F_3 + F_5) \cdot Z_c + X_2 \cdot [F_2 + F_4] + F_5) \cdot \bar{Z}_c$$

$$S_{FJ} = \bar{F}_1 + ((F_2 + F_3 + F_4 + F_4) \cdot \bar{Z}_c) \tag{3.16}$$

where $F_1 = \bar{C}_1$, $F_2 = \bar{C}_1 \cdot C_2$, $F_3 = \bar{C}_2 \cdot C_3$, $F_4 = \bar{C}_3 \cdot C_4$, and $F_5 = C_4$ (refer Figure 3.9). The corresponding PWM scheme and the associated subsystem is shown in Figure 3.10.

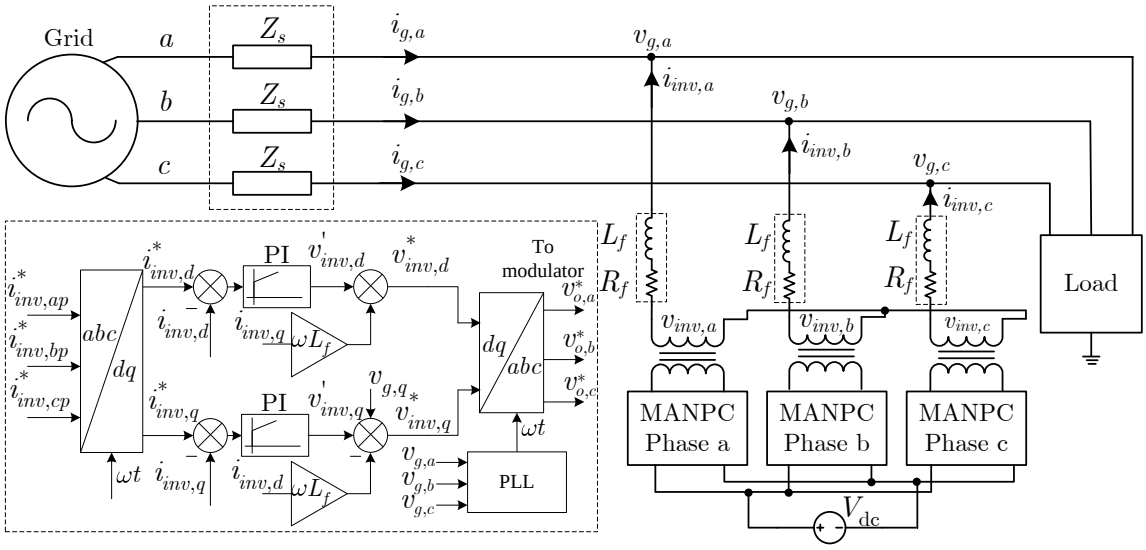


Figure 3.11: Grid-connected proposed hybrid 10S-ANPC-MLI

3.8 Simulation study of the grid-connected 10S-ANPC MLI and experimental results

Firstly, a three-phase grid-connected case study is considered to validate the proposed topology. The system under consideration is shown in Figure 3.11. The MLI is controlled to inject the active power and exchange reactive power with the grid. A standard *dq*-based current controller is employed for the control of grid current. In Figure 3.11, $i^*_{\text{inv,xp}}$ $(x = a, b, c)$ refers to the reference value of the peak grid current. A dc source of voltage 5 kV, grid voltage of line-line rms value 4.16 kV, FC with capacitance of 1.2 mF, switching frequency of 2.5 kHz is considered. Following are the cases investigated:

Case 1 The MLI is operated to inject a constant active power of 2.5 MW. The output voltage of the inverter, grid current, injected grid current are shown in Figure 3.12(a). As evident, the grid current is in phase with the grid voltage confirming the unity PF operation of the MLI. The voltage across the FCs are shown in Figure 3.12(b) which are well regulated at 1.25 kV.

Case 2 It is beneficial to have the MLI to inherit the property of reactive power generation/absorbing capability to support the grid during voltage ride through conditions. Hence, in this case, the MLI is operated to feed a reactive power

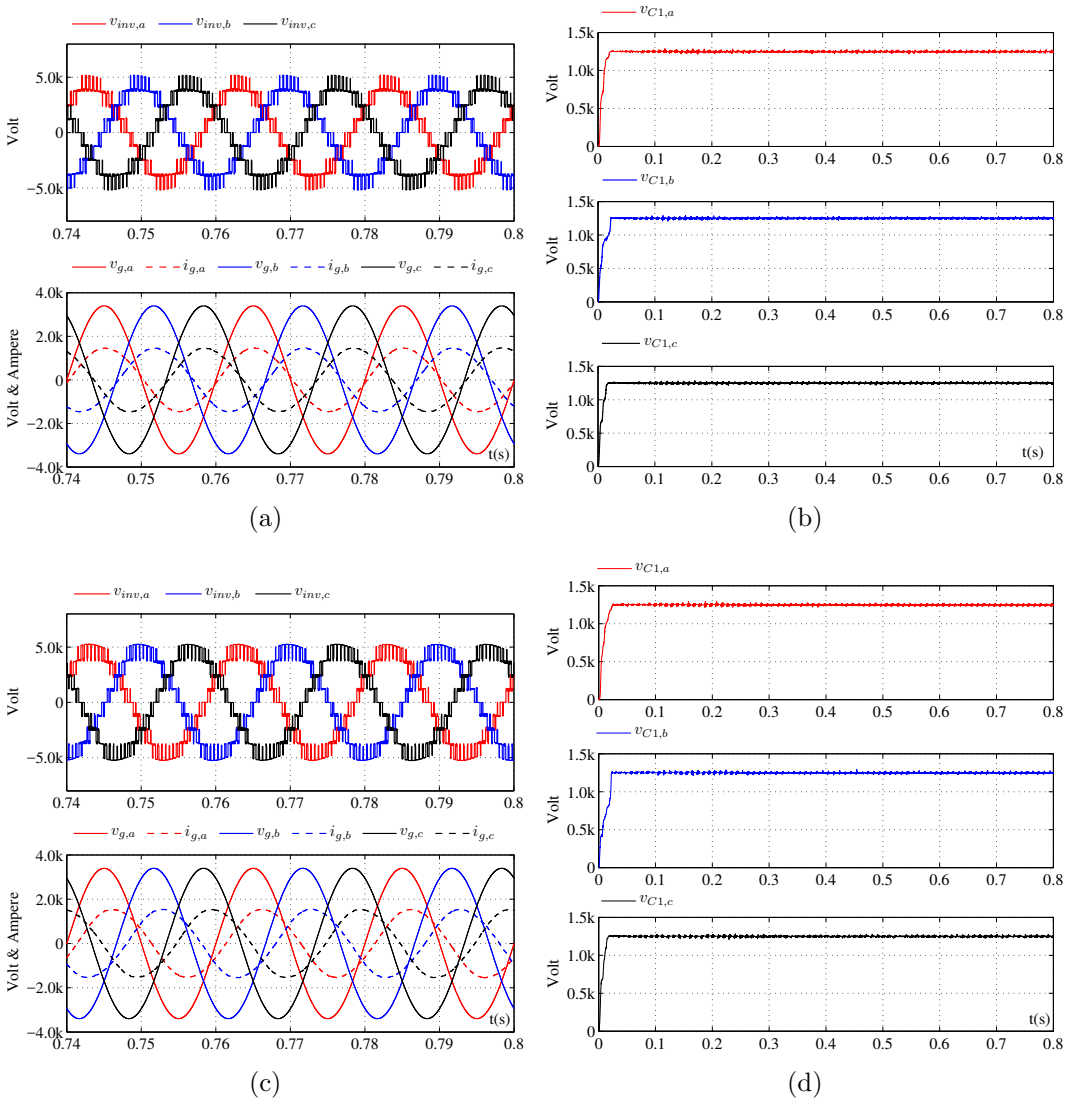


Figure 3.12: Simualtion results (a) MLI output voltage, grid voltage and grid current operating at UPF operation (b) Voltage across FCs under UPF operation (c) MLI output voltage, grid voltage and grid current operating at non UPF operation (d) Voltage across FCs under non UPF operation, k = 1×10^3

of 1 MVAr in addition to 2.5 MW of active power injection. The injected grid current lags the utility voltage validating the reactive power injection (refer Figure 3.12(c)) and the voltage across FCs remains at their reference value irrespective of the operating PF (refer Figure 3.12(d)).

Case 3 The system is tested for its satisfactory dynamic state performance. Firstly,

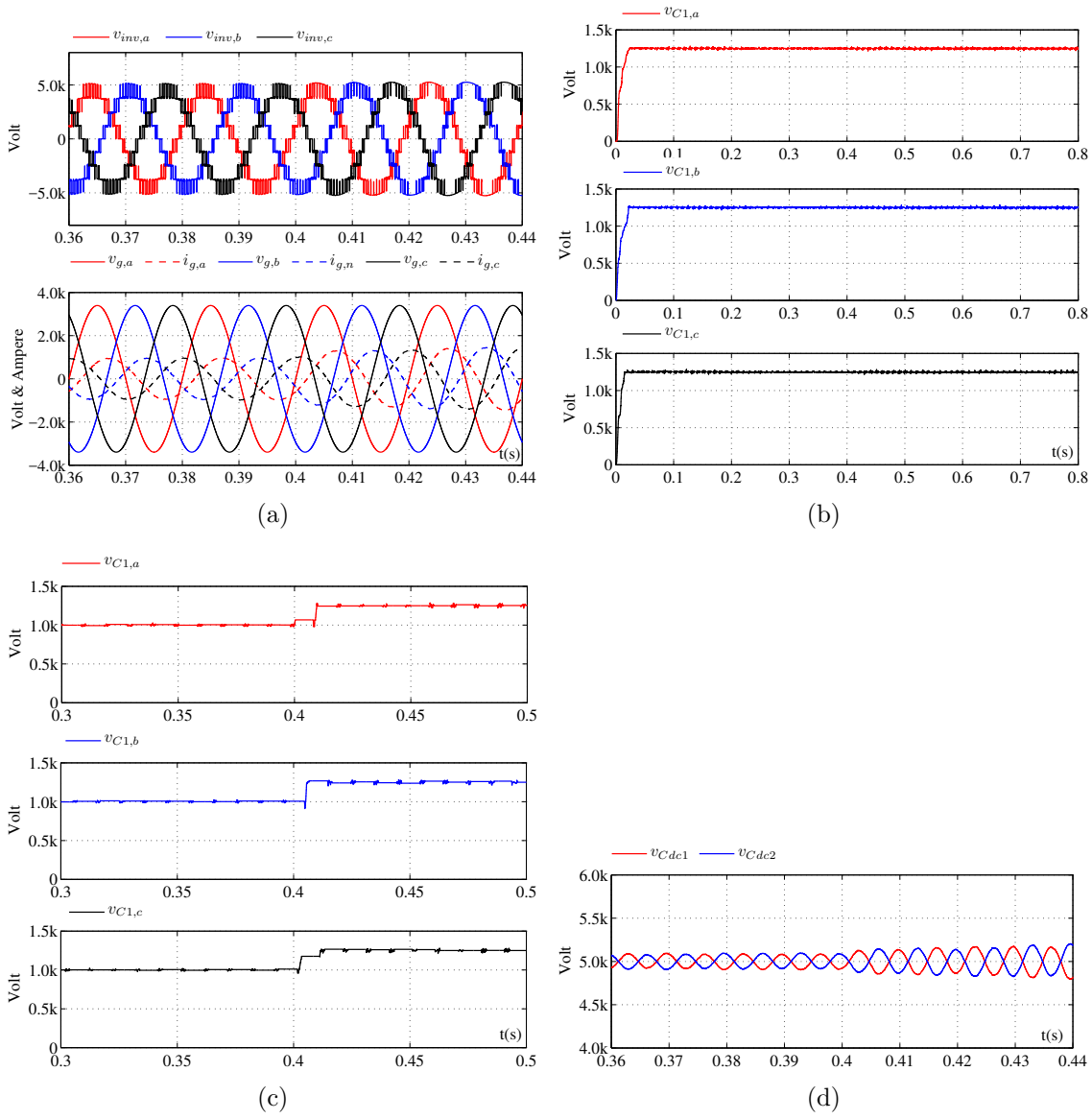


Figure 3.13: Simulation results (a) MLI output voltage, grid voltage and grid current operating at non UPF operation for step change in reference active power at $t = 0.4$ s (b) Voltage across FCs under non UPF operation for step change in reference active power at $t = 0.4$ s (c) Voltage across FCs for step change in dc-link voltage at $t = 0.4$ s (d) MLI output voltage, grid voltage and grid current operating at non UPF operation for step change in modulation index at $t = 0.4$ s, k = $1{\times}10^3$

a step change in reference active power is applied at $t = 0.4$ s while the MLI operating at a PF of 0.707 (lag). The corresponding responses are shown in Figure 3.13(a)-(b). It is evident from the waveforms, the response of the system is found competent. Secondly, a step change in dc-link voltage (4 kV to 5 kV) is applied at $t = 0.4$ s. The FC voltages gradually raise and settles promptly at their new reference value of 1.25 kV from 1 kV (refer Figure 3.13(c)). The natural balancing of the dc-link capacitors obviates the need of an additional balancing circuit is shown in Figure 3.13(d).

Further, the measurement results obtained from the laboratory prototype as described in Appendix C is shown in the Figure 3.14.

3.9 Comparative study

In this section both the proposed ANPC-based topologies are compared with those presented in the literature. The comparison is performed considering the following aspects:

- Switch count and rating: As it can be seen from Table 2.4 the proposed 10S-ANPC MLI topology requires the least number of switches. Though the topologies by (Chaudhuri et al., 2010) and (Sadigh et al., 2010a) need lesser number of switches than the proposed 12S ANPC topology, the former has a limitation on the maximum modulation index achievable while the blocking voltage of the latter structure is high.

- FC count and rating: It is inferred from the Table 2.4 that both the proposed topologies require only one (least among all the topologies under consideration) FC for 9L operation, and needs to withstand a voltage of only $V_{\mathrm{dc}}/4$. Thus the size and therefore cost of the proposed topologies are less.

- TBV: Further, it is essential to evaluate the total standing voltage or blocking voltage (expressed in p.u.) as it reflects to the silicon requirement and thus the cost of a converter. As an example, the typical rating of the power devices required for a 5-6 MW wind turbine system is demonstrated. The proposed AnPC-based topologise is found to exhibit the lowest value of TBV in comparison to other topologies.

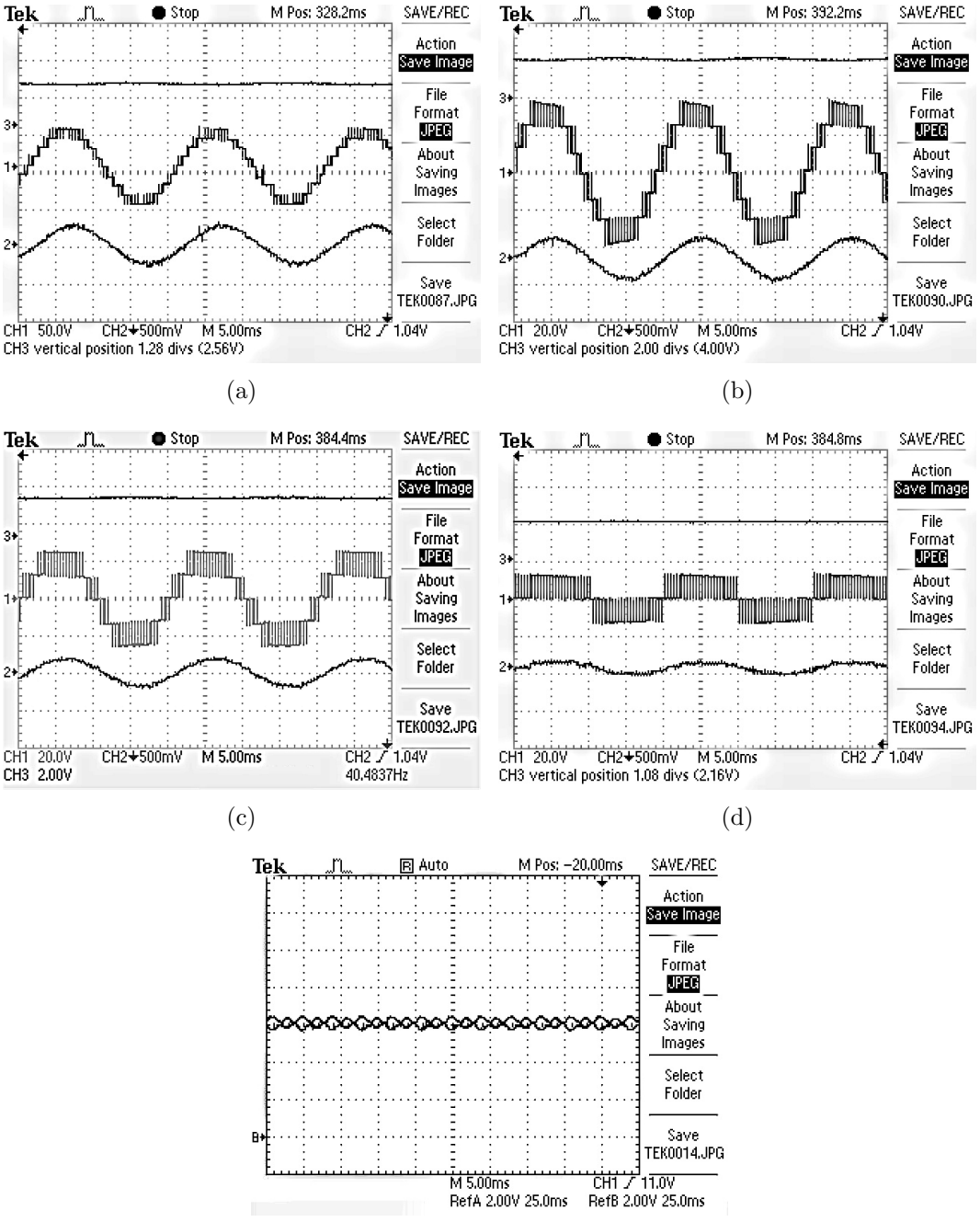


Figure 3.14: Experimental results of 10S-ANPC MLI: inverter output voltage, load current, FC voltage for (a) $m_a = 1$ (b) $m_a = 0.74$ (c) $m_a = 0.48$ (d) $m_a = 0.24$ (e) dc-link capacitor voltages

Table 3.4: Comparison of the proposed ANPC-based MLIs with other topologies

Topologies	No. of Switches	TBV (p.u.)	Selected commercial devices					No. of FCs	Voltage rating of FCs				No. of dc sources		Maximum modulation index
			6.5 kV	4.5 kV	3.3 kV	1.7 kV	1.2 kV		$3V_{dc}/4$	$V_{dc}/2$	$V_{dc}/4$	$V_{dc}/8$	$V_{dc}/2$	V_{dc}	
1.	12	6	4	-	-	8	-	3	1	1	1	-	-	2	1.0
2.	14	9	6	-	4	4	-	2	-	1	1	-	-	2	1.0
3.	14	7.5	4	-	4	6	-	2	-	1	1	-	-	2	1.0
4.	10	8	-	4	4	2	-	2	-	1	1	-	-	2	0.925
5.	12	7	4	-	4	4	-	3	-	1	1	-	-	2	1.0
6.	12	7	-	-	4	4	4	3	-	-	-	3	-	2	1.0
7.	10	8	2			8		3	1	1	1		1	-	1.0
8.	14	6	-	-	2	8	4	3	-	-	2	1	-	2	1.0
12S ANPC	12	7	2	-	6	-	4	1	-	-	1	-	2	-	1.0
MANPC	10	5	2	-	4	4	-	1	-	-	1	-	2	-	1.0

1. Barbosa et al. (2005)

2. Veenstra and Rufer (2005)

3. Chaudhuri et al. (2007)

4. Chaudhuri et al. (2010)

5. Li et al. (2011)

6. Rajeevan et al. (2013)

7. Sadigh et al. (2010a)

8. Viju et al. (2017)

Chapter 4

HYBRID SMC CONVERTER

The advent of the SMC MLI which is a hybridization of FCC has gained a significant research interest due to its reduced number of capacitors. Structurally, SMC MLI is built by stacking two or more FCCs. A few of the switches and FCs are shared among stacked units thus reducing the component demand. Although SMC has outperformed FCC, for higher number of voltage levels, increased energy density trivializes it to dispense its industrial presence (Kouro et al., 2010).

4.1 Classic SMC MLI

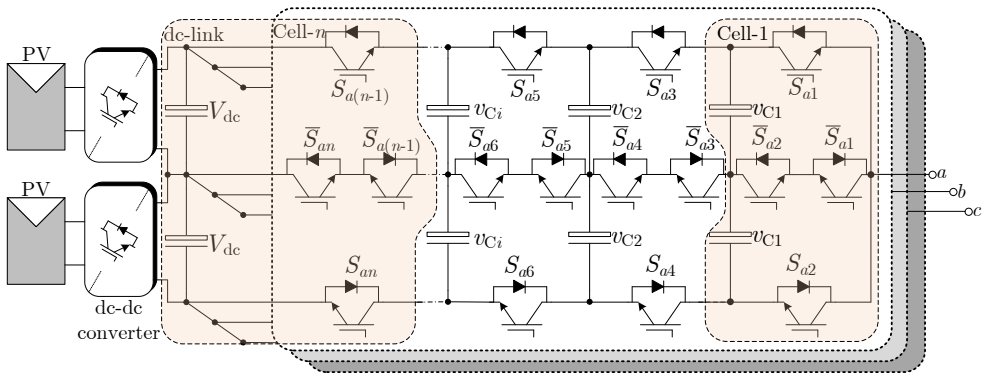


Figure 4.1: Generalized topology of an n-cell $(2n + 1)$-level SMC

Figure 4.1 shows the general structure of the classic SMC. It comprises "n" number of cells. Each cell is made up of four switches and two FCs. The voltage across the FCs belonging to a single cell are identical. The dc-link is made up of two capacitors,

each of them is regulated to half of the dc-link voltage. Further, it is imperative to maintain the average voltage across FCs at a predefined value to enable the SMC MLI to generate a multilevel output voltage with uniform steps. The voltage across the FCs to be maintained is given as,

$$v_{Ci} = \frac{i \times V_{\mathrm{dc}}}{2 \times \mathrm{n}} \text{ for } i = 1, 2, ..., \mathrm{n} - 1. \tag{4.1}$$

For instance, with n = 3, the SMC generates a 7L voltage i.e., $-V_{\mathrm{dc}}$, $-V_{\mathrm{dc}}/3$, $-V_{\mathrm{dc}}/6$, 0, $V_{\mathrm{dc}}/6$, $V_{\mathrm{dc}}/3$, and V_{dc}. It requires four FCs whose voltage values are $V_{\mathrm{C1}} = \frac{V_{\mathrm{dc}}}{6}$ and $V_{\mathrm{C2}} = \frac{V_{\mathrm{dc}}}{3}$. It is worth noting that the upper and lower stack operates during the positive and negative half cycle of the fundamental output voltage respectively. The number of output voltage levels (N_{L}) as a function of n is given as,

$$N_{\mathrm{L}} = 2\mathrm{n} + 1. \tag{4.2}$$

The required number of capacitors (N_{C}) expressed as a function of n is given as,

$$N_{\mathrm{C}} = 2\mathrm{n}. \tag{4.3}$$

Further, to extend the SMC MLI for more number of voltage levels, additional cells are required to be cascaded. As a result, four switches and two capacitors are added which in turn leads to an increased structural and control complexity. In addition, the diversified voltage ratings of capacitors result in increased energy density, size and volume of the circuit. Hence, a methodology to combat the necessity of more number of capacitors and switches is essential. In this thesis, an approach to hybridize the SMC MLI by conflating it with other standard power electronic converter unit(s) is presented. A 3L-FCHB is used as an additional converter block for extending the generic SMC to generate higher voltage levels. The generalized structure of the proposed hybrid SMC referred to as a 12S-SMC MLI is shown in Figure 4.2.

A generic 5L-SMC MLI is retained as a front-end converter. For supplementing the generation of higher voltage levels, 3L-FCHBs are cascaded as demonstrated in Figure 4.2. The relation between N_{L} and the number of FCHBs (m) of the proposed

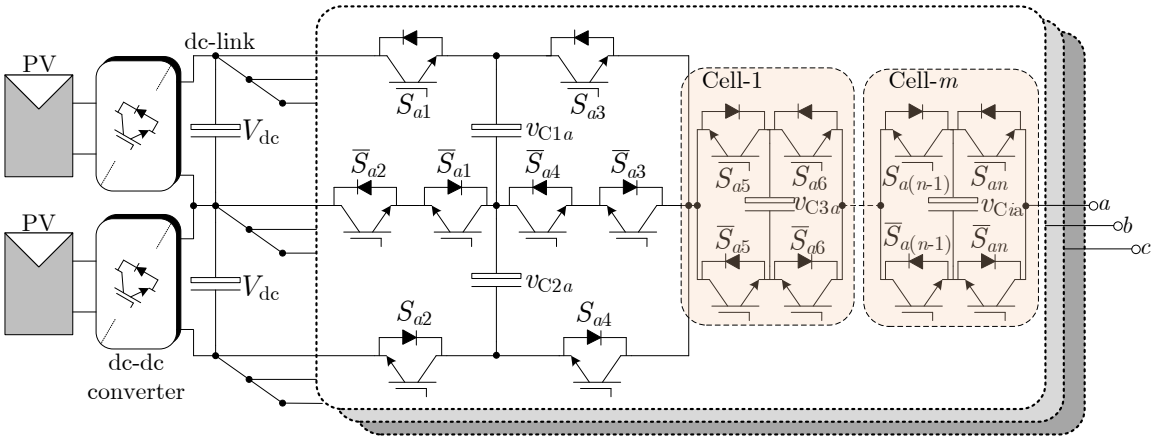


Figure 4.2: Generalized topology of the proposed m-cell 12S-SMC MLI

12S-SMC MLI is given as,

$$N_{\rm L} = (4 \times 2^{\rm m}) + 1. \tag{4.4}$$

The relation between $N_{\rm C}$ and m is given as,

$$N_{\rm C} = 2 + {\rm m}. \tag{4.5}$$

Following the underlying structural description of the proposed 12S-SMC MLI, it is worth noting its distinctive advantages which are outlined below.

- The structure is modular; if any of the FCHB fails (it can be replaced), the MLI operation is preserved with a reduced number of voltage levels by bypassing the faulty cell.
- The voltage stress across the switches corresponding to FCHB units are lesser and thus leads to reduced power losses. This reduction becomes more significant as the number of voltage level increases.
- The developed topology require a lesser number of switches and capacitors for a given number of voltage levels.

In the present case, for 9L output voltage, a single FCHB unit is adequate. Thus, the 12S-SMC MLI consists of three capacitors and a suitable active voltage balancing control strategy for regulating their voltages at reference values. To develop a voltage

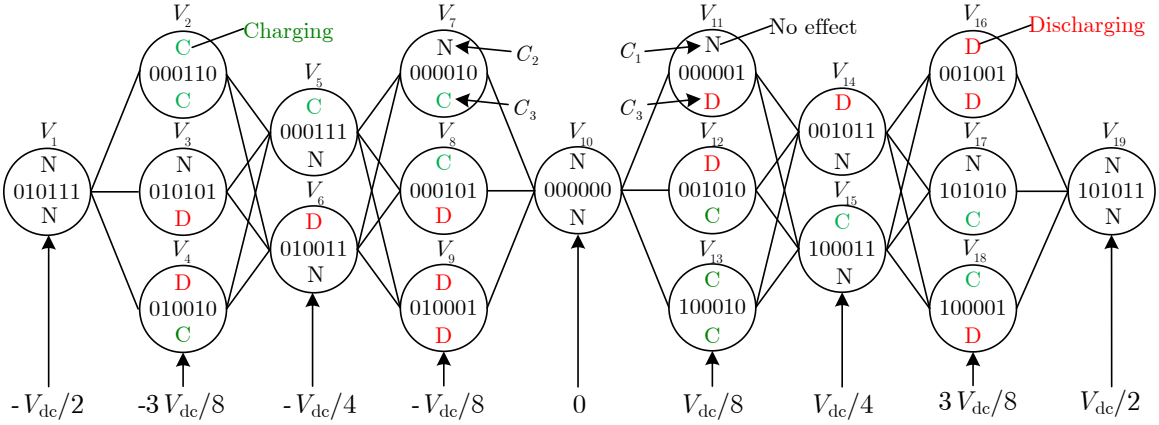


Figure 4.3: Switching flow diagram of the proposed 9L-12S-SMC MLI

balancing mechanism, firstly the various switching states corresponding to each of the output voltage levels and their effect on the capacitor voltages are examined. Figure 4.3 depicts the various switching combinations and the effect of each state on the capacitor voltages. The following are the noteworthy points from the allowable transition states between levels.

- There are 19 distinct switching states for the developed 9L 12S-SMC MLI.
- The switching status of each of the switch is represented using a binary bit i.e., "0" for OFF and "1" for ON condition of a particular switch
- The most significant bit (inside the circle earmarked for each possible switching combination) corresponds to the switch placed near dc-link and the remaining bits follows the order of switches from there on to the switch near to the load point.
- A few of the voltage levels can be realized by using more than one switching states (for e.g., $3V_{dc}/8$) referred to as redundant states. Such states have an opposing effect on the capacitor voltages, thus helps in their regulation.
- The capacitor C_1 and C_2 are involved in the level generation during the positive and negative half cycle of the output voltage respectively, whereas, C_3 plays a role in both the half cycles.

4.2 Active voltage balancing of capacitor voltages

As a first step, since there are two capacitors involved in each of the positive and negative half cycles of the output voltage, it is essential to determine the capacitor which needs to be addressed at a given sampling instance and this process is referred to as capacitor prioritizing. To facilitate the selection process, per unit voltage deviation ($\Delta_{V_{\mathrm{Cx}}}$) of the capacitors is computed as follows:

$$\Delta_{V_{\mathrm{C1}}} = \frac{V^*_{\mathrm{C1}} - |V_{\mathrm{C1}}|}{V^*_{\mathrm{C1}}}, \tag{4.6}$$

$$\Delta_{V_{\mathrm{C2}}} = \frac{V^*_{\mathrm{C2}} - |V_{\mathrm{C2}}|}{V^*_{\mathrm{C2}}}, \tag{4.7}$$

$$\Delta_{V_{\mathrm{C3}}} = \frac{V^*_{\mathrm{C3}} - |V_{\mathrm{C3}}|}{V^*_{\mathrm{C3}}}, \tag{4.8}$$

where $V^*_{\mathrm{C1}}, V^*_{\mathrm{C2}}$, and V^*_{C3} are the reference voltages to be maintained across C_1, C_2, and C_3 respectively. $V_{\mathrm{C1}}, V_{\mathrm{C2}}$ and V_{C3} are the actual sensed voltages. A priority factor (P_{Cx}) is employed to rightly distinguish and select the capacitor that has a comparatively higher voltage deviation and is defined as follows:

$$P_{\mathrm{C13}} = \begin{cases} 1, & \Delta_{V_{\mathrm{C1}}} > \Delta_{V_{\mathrm{C3}}} \\ 0, & \Delta_{V_{\mathrm{C1}}} \leq \Delta_{V_{\mathrm{C3}}} \end{cases} \tag{4.9}$$

$$P_{\mathrm{C23}} = \begin{cases} 1, & \Delta_{V_{\mathrm{C2}}} > \Delta_{V_{\mathrm{C3}}} \\ 0, & \Delta_{V_{\mathrm{C2}}} \leq \Delta_{V_{\mathrm{C3}}} \end{cases} \tag{4.10}$$

$P_{\mathrm{C13}} = 1$ implies that the voltage deviation across C_1 is higher than that of C_3, thus C_1 needs attention otherwise C_3 needs attention. Similar to the strategy as discussed in Chapter 3, a single carrier-based PWM is generated. The procedure to develop the LFE-based switching function is detailed for the switch S_1, and the same process is repeated for the remaining switches. From Figure 4.3, S_1 is ON during the states $V_{13}, V_{15}, V_{17}, V_{18}$, and V_{19}. The condition to be satisfied for the switching ON of S_1 is illustrated in Table 4.1. The variables X_1, X_2, X_3, and X_4 in the Table 4.1

are given as,

$$\begin{aligned}
X_1 &= I\bar{\Delta}_{V_{\mathrm{C1}}} + \bar{I}\Delta_{V_{\mathrm{C1}}},\\
X_2 &= \bar{I}\bar{\Delta}_{V_{\mathrm{C1}}} + I\Delta_{V_{\mathrm{C1}}},\\
X_3 &= I\bar{\Delta}_{V_{\mathrm{C2}}} + \bar{I}\Delta_{V_{\mathrm{C2}}},\\
X_4 &= \bar{I}\bar{\Delta}_{V_{\mathrm{C2}}} + I\Delta_{V_{\mathrm{C2}}},\\
X_5 &= I\bar{\Delta}_{V_{\mathrm{C3}}} + \bar{I}\Delta_{V_{\mathrm{C3}}}, \text{and}\\
X_6 &= \bar{I}\bar{\Delta}_{V_{\mathrm{C3}}} + I\Delta_{V_{\mathrm{C3}}}.
\end{aligned} \tag{4.11}$$

The corresponding simplified switching functions for S_1 and for the remaining switches are derived as,

$$S_{F1} = \left[C_1\bar{C}_2(X_1P_{\mathrm{C13}} + X_3\bar{P}_{\mathrm{C13}}) + C_2\bar{C}_3X_1 + C_3\bar{C}_4(X_1P_{\mathrm{C13}} + X_3 + X_4\bar{P}_{\mathrm{C13}}) + C_4\right]Z_{\mathrm{CI}}, \tag{4.12}$$

$$S_{F2} = \left[C_1\bar{C}_2(X_5P_{\mathrm{C23}} + X_3\bar{P}_{\mathrm{C23}}) + C_2\bar{C}_3X_2 + C_3\bar{C}_4(X_3\bar{P}_{\mathrm{C23}} + X_5P_{\mathrm{C23}} + X_6) + C_4\right]\bar{Z}_{\mathrm{CI}}, \tag{4.13}$$

$$S_{F3} = \left[C_1\bar{C}_2(X_4\bar{P}_{\mathrm{C13}} + X_1P_{\mathrm{C13}}) + C_2\bar{C}_3X_2 + C_3\bar{C}_4(X_2P_{\mathrm{C13}} + X_4\bar{P}_{\mathrm{C13}} + X_3) + C_4\right]Z_{\mathrm{CI}}, \tag{4.14}$$

$$S_{F4} = \left[C_1\bar{C}_2(X_5\bar{P}_{\mathrm{C23}} + X_3P_{\mathrm{C23}}) + C_2\bar{C}_3X_5 + C_3\bar{C}_4(X_6P_{\mathrm{C23}} + X_3\bar{P}_{\mathrm{C2}} + X_4) + C_4\right]\bar{Z}_{\mathrm{CI}}, \tag{4.15}$$

$$\begin{aligned}
S_{F5} = {} & \Big(\left[C_1\bar{C}_2(X_4\bar{P}_{\mathrm{C13}} + (X_1 + X_2)P_{\mathrm{C13}}) + C_3\bar{C}_4X_4\right]\Big)Z_{\mathrm{CI}}\\
& + \Big(C_1\bar{C}_2(X_4 + X_5P_{\mathrm{C12}}) + C_3\bar{C}_4(X_4\bar{P}_{\mathrm{C12}} + (X_5 + X_6)P_{\mathrm{C12}})\Big)\bar{Z}_{\mathrm{CI}},
\end{aligned} \tag{4.16}$$

$$\begin{aligned}
S_{F6} = {} & \Big(C_1\bar{C}_2X_4 + C_3\bar{C}_4(X_4\bar{P}_{\mathrm{C13}} + (X_1 + X_2)P_{\mathrm{C13}})\Big)Z_{\mathrm{CI}}\\
& + \Big(C_1\bar{C}_2(X_3\bar{P}_{\mathrm{C23}} + X_6P_{\mathrm{C23}}) + C_3\bar{C}_4X_3\Big)\bar{Z}_{\mathrm{CI}}.
\end{aligned} \tag{4.17}$$

These uncomplicated switching functions entirely take care of capacitor voltage balancing. Further, a grid-connected case study is performed to verify the performance of the developed LFE-based voltage balancing control method.

Table 4.1: Variables required for the logical formulation of switching function of S_1

	$P_{\text{C13}} = 1$				$P_{\text{C13}} = 0$			
States	X_1	X_2	X_3	X_4	X_1	X_2	X_3	X_4
V_{13} $(C_1\bar{C}_2)$	1	0	0	0	0	0	1	0
V_{15} $(C_2\bar{C}_3)$	1	0	0	0	1	0	0	0
V_{17} $(C_3\bar{C}_4)$	1	0	1	0	0	0	1	1
$V_{19}(C_4)$	0	0	0	0	0	0	0	0

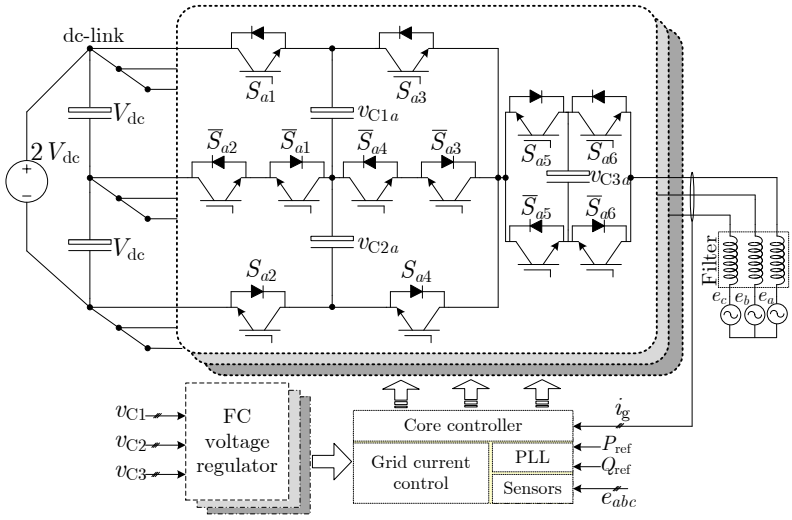


Figure 4.4: Grid-connected 12S-SMC MLI and its associated system components

Table 4.2: Main parameters considered for simulation

Parameter	Value
dc source voltage (V_{dc})	5 kV
Grid voltage (e_{ab})	4.16 kV(rms)
Capacitances ($C_1, C_2, C_3, C_{\text{dc}}$)	1.1 mF, 1.1 mF, 2.2 mF, 1.2 mF
Carrier frequency (f_{sw})	2.5 kHz

4.3 Simulation results

In this section, the developed LFE-based voltage balancing strategy is integrated with the grid current control strategy. The three-phase version of the proposed 12S-SMC MLI connected to grid is shown in Figure 4.4 and the corresponding essential system parameters are enlisted in Table 4.2. The 12S-SMC MLI and its associated control scheme are simulated using the MATLAB/Simulink. Firstly, the steady-state waveforms are presented (see Figure 4.6). The various plots depicted as a subset of

each test conditions are as follows: plot (a) 12S-SMC MLI phase voltages (b) phase-a grid voltage and injected current (c) voltage across capacitors of 12S-SMC MLI phase-a (d) phase-b grid voltage and injected current (e) voltage across capacitors of 12S-SMC MLI phase-b (f) phase-c grid voltage and injected current (g) voltage across capacitors of 12S-SMC MLI phase-c (h) active and reactive power pushed into the grid (i) voltage across dc-link capacitors. The active reference power (P_g^*) and reactive reference power (Q_g^*) are set to 10 MW and 0 MVAr respectively, as the steady state value of power to be injected into the grid. Figure 4.5 (a) shows the phase voltages of the 12S-SMC MLI comprising of nine levels (0, $\pm$1250 V, $\pm$2500 V, $\pm$3750 V, and $\pm$5000 V). Figures 4.5(b), (d), (f) show the grid voltages and currents injected by the 12S-SMC MLI. It is evident from the plots that the injected currents are in phase with the grid voltages, thus, active power alone in pumped into the grid. The voltage across the various capacitors as depicted in Figures 4.5(c), (e), (g) attest the satisfactory performance of the developed voltage balancing mechanism for regulating the capacitor voltages. The actual active and reactive power injected into the grid shown in Figure 4.5(h) confirms the successful tracking of the desired P_g^* and Q_g^* value. The natural balancing of the dc-link capacitors is witnessed in Figure 4.5(i). Further, the system is subjected to three test conditions in order to visualize its performance under the dynamic conditions as discussed under:

1. Step change in P_g^*: Firstly, at $t = 0.55$ s, a step change is applied in P_g^* from 4 MW to 10 MW. As a response, the magnitudes of injected grid currents are increased and reaches a value corresponding to P_g^*=10 MW validating the fast and satisfactory performance of the controller (see Figure 4.6). Despite such perturbation, the voltage across the various capacitors remain intact validating the correctness of the developed voltage balancing controller.

2. Step change in Q_g^*: Secondly, a grid-connected distributed generation system is quite often expected to source/sink reactive power in addition to the active power injections from the renewable sources. To verify the reactive power handling capability, a step change in Q_g^* is applied at t =0.55 s from 0 to 5 MVAr. As a consequence, the 12S-SMC MLI supplies the demanded reactive power while keeping the active power injection intact. Further, at t =0.6 s, Q_g^* is changed from 5 MVAr to -5 MVAr; the 12S-SMC MLI starts absorbing the desired reactive power. During the entire preceding events, the capacitor voltages

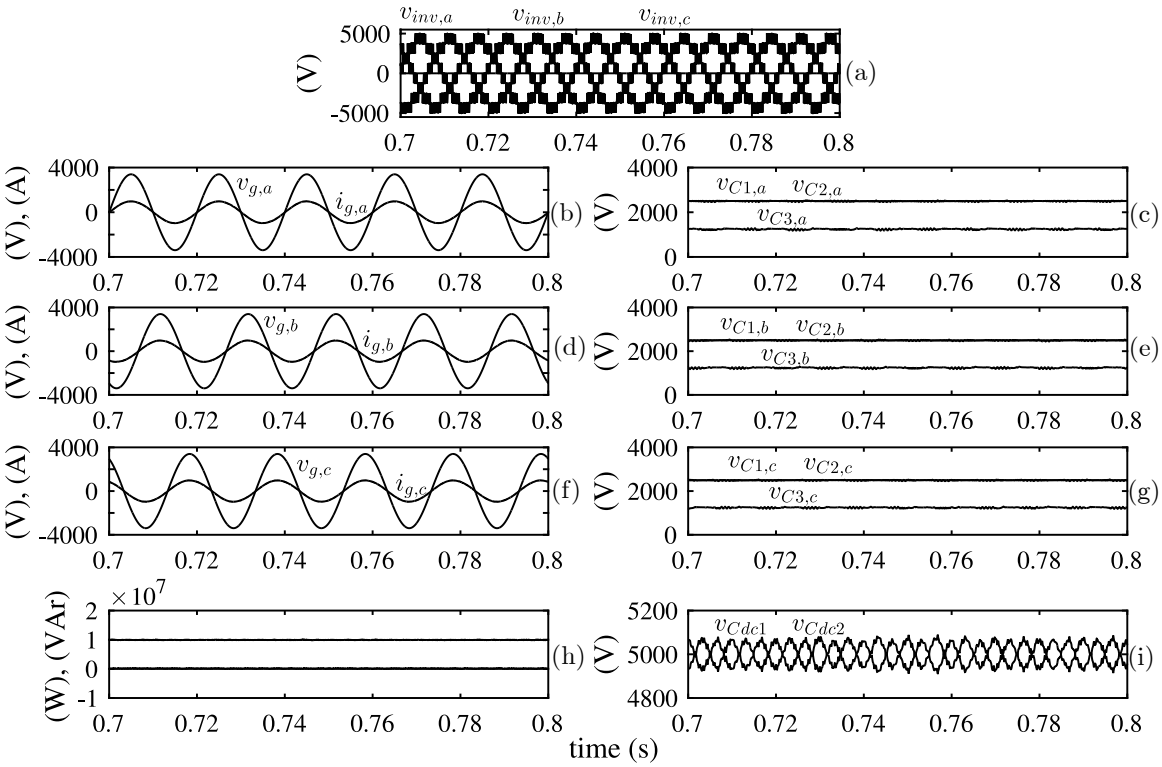


Figure 4.5: Steady state waveforms

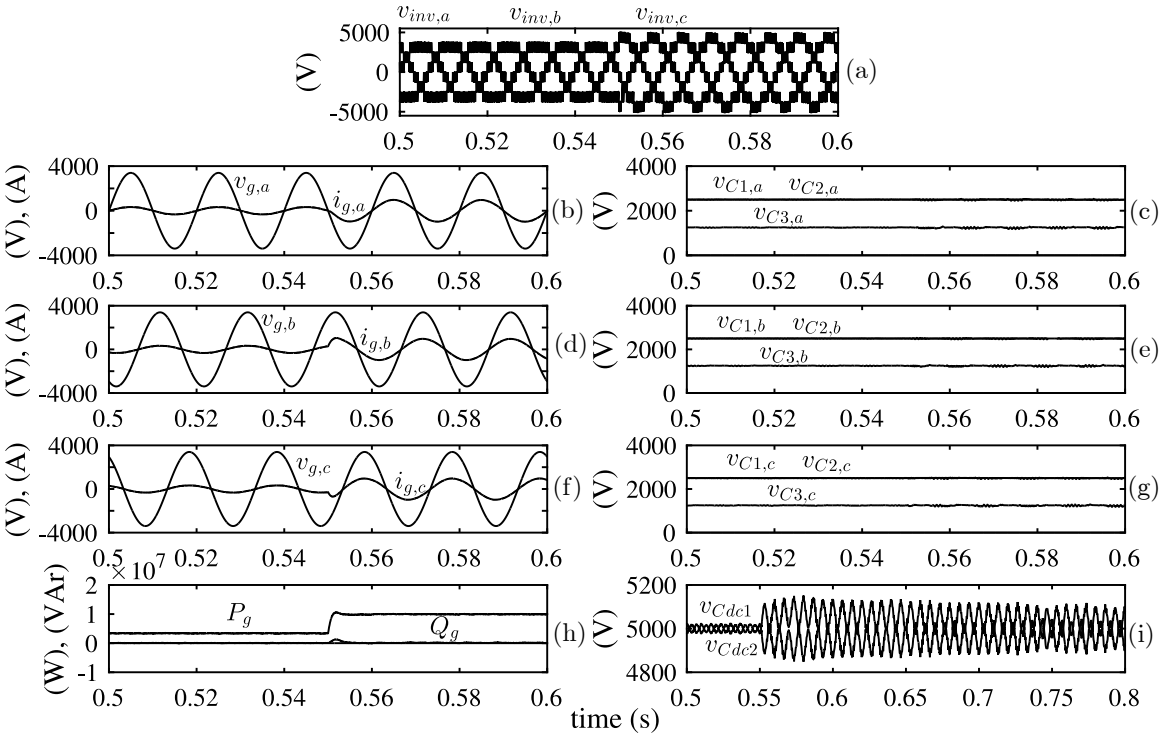


Figure 4.6: Results pertaining to step change in P_g^* (4 MW to 10 MW) at $t = 0.55$ s

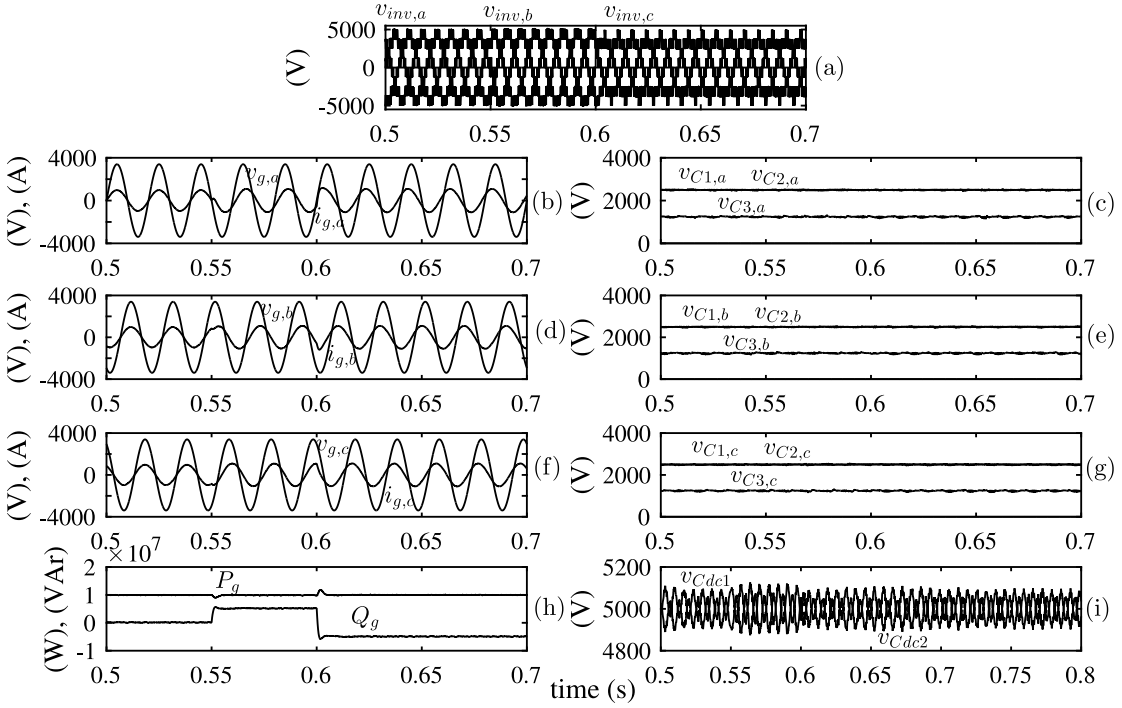


Figure 4.7: Results pertaining to step change in Q_g^* (0 MVAr to 5 MVAr) at $t = 0.55$ s and 5 MVAr to -5 MVAr at t=0.6 s

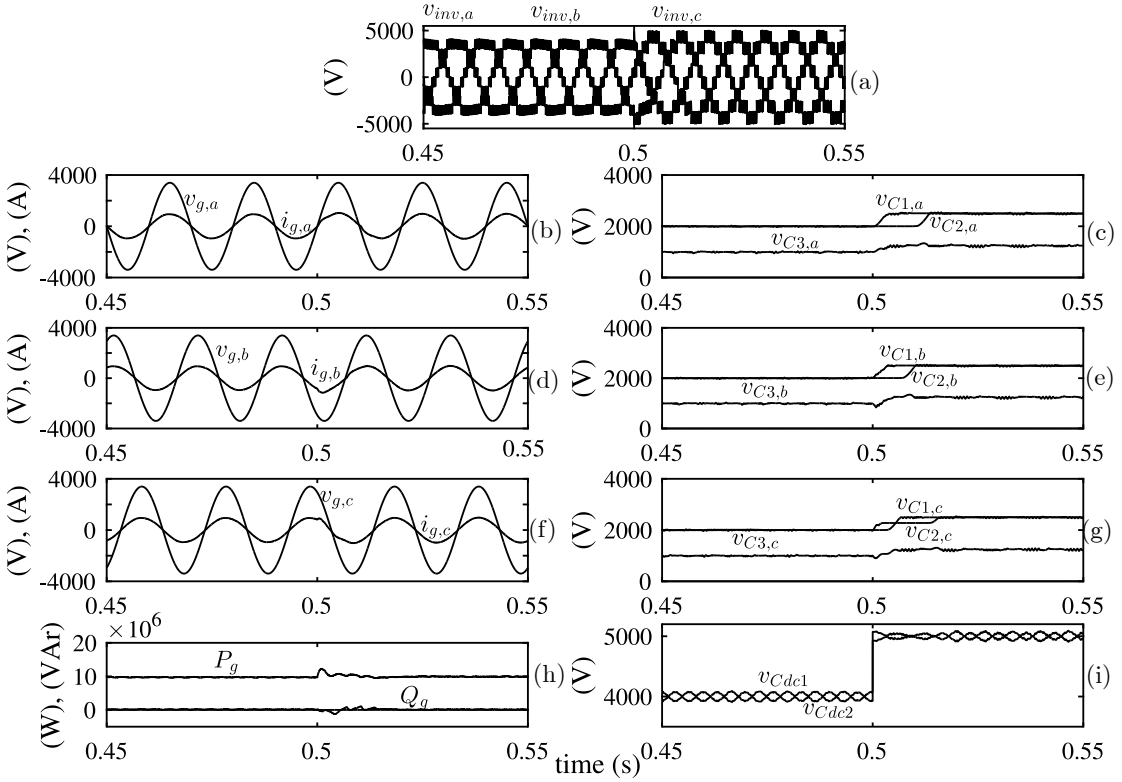


Figure 4.8: Results pertaining to step change in dc-link voltage (8 kV to 10 kV) at $t = 0.5$ s

are held tightly around their reference value. Figure 4.7 characterizes the above events in various plots.

3. Step change in V_{dc}: Lastly, at $t = 0.5$ s, the dc-link voltage is stepped up from 8 kV to 10 kV. The system response to the preceding event is shown in Figure 4.8. It is evident from the plots that the developed voltage balancing scheme proves to be robust in regulating the capacitor voltages under all possible external perturbations. Besides, except for a small initial deviation, the injected active power is held constant since the value of P_g^* is kept unaltered.

4.4 Comparative study

A qualitative comparison of the proposed 12S-SMC MLI with state of the art topologies; DFCM (Sadigh et al., 2010b), MLDCL (Su, 2005), HMC, (Lezana and Aceiton, 2011), SANPC (Nair et al., 2017), QFCM (Ebrahimi and Karshenas, 2017) is performed. Various figures of merit are considered for the comparison. From Figure 4.9(a) it is evident that the proposed 12S-SMC MLI requires the least number of switches and has an improved reliability. As in any FC-based multilevel converter, the number of FCs plays a vital role in determining the overall cost of the converter. Also, from the reliability point of view capacitors are the second weakest link following the power switches. Hence it is essential to devise converter structure with a lesser number of capacitors. The proposed 12S-SMC MLI and the SANPC topology requires the least number of FCs as indicated in Figure 4.9(b), and thus they need less space and exhibit higher power density. Another major cost factor is the voltage rating of the FCs. In given situation, even though the number of FCs are less, the variety in voltage need to be sustained by them adds on to the cost. Thus, it is crucial to lessen the voltage diversity. With this view, the proposed inverter is compared and Figure 4.9(c) shows the result. Finally, the efficiency curve plot shows the improved performance of the 12S-SMC MLI (refer Figure 4.9(d)).

4.5 12S-SMC MLI modeling

As the number of voltage level increases, the required capacitors increases as well. This escalation adds on to the cost of the 12S-SMC MLI due to additional sensors

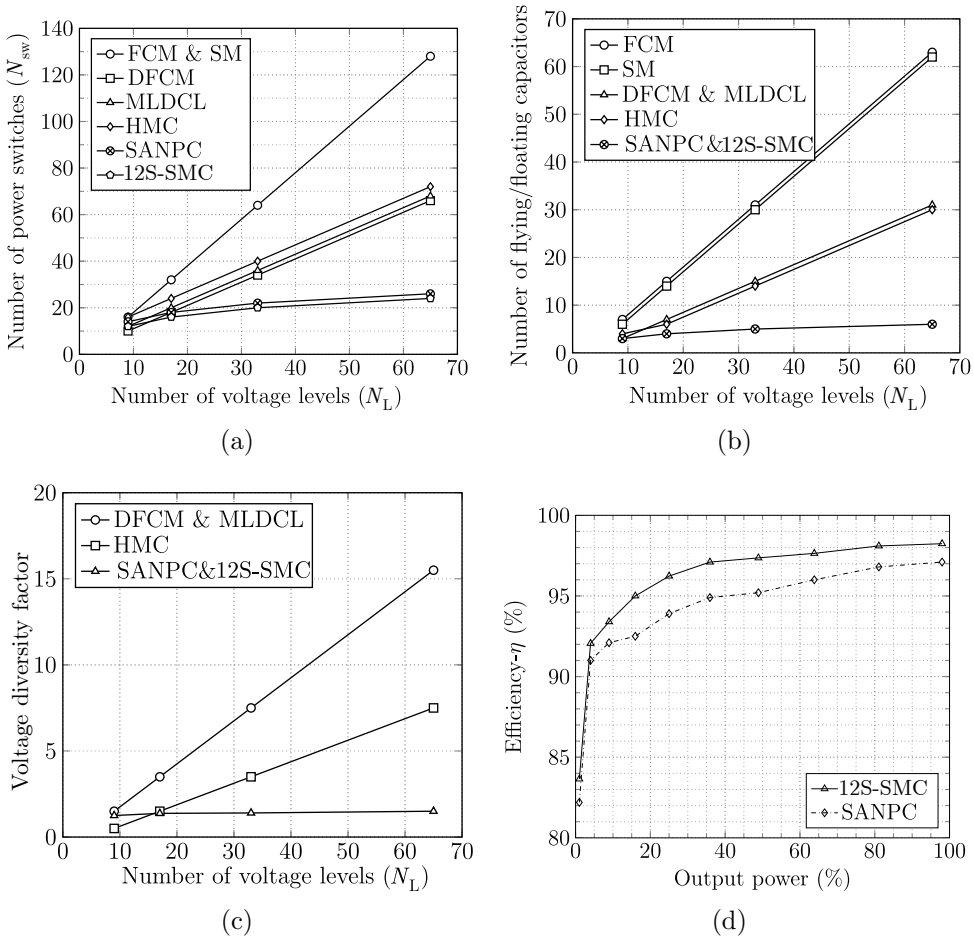


Figure 4.9: Comparison of number of switches, FCs, voltage diversity factor of FCs and efficiency of various MLIs

that are necessary for the capacitors voltage control. One of the ways to confront this issue is to estimate the capacitor voltage using the state-space modeling of the converter thereby eliminating the sensor(s) (Gateau et al., 2002). Development of the instantaneous model of the converter is imperative in the process of voltage estimation and control method. An effort in this regard is made, and the corresponding state-space model of 9L 12S-SMC MLI obtained is as follows:

$$\begin{cases} \dot{\underline{X}} & = A(\underline{S}(t))X(t) + B(\underline{S}(t))V_{\mathrm{dc}}, \\ Y(t) & = C(\underline{X}), \end{cases} \tag{4.18}$$

$$X(t) = \left[V_{\mathrm{C1}}(t)\ V_{\mathrm{C2}}(t)\ V_{\mathrm{C3}}(t)\ i_{\mathrm{L}}(t)\right]^T. \tag{4.19}$$

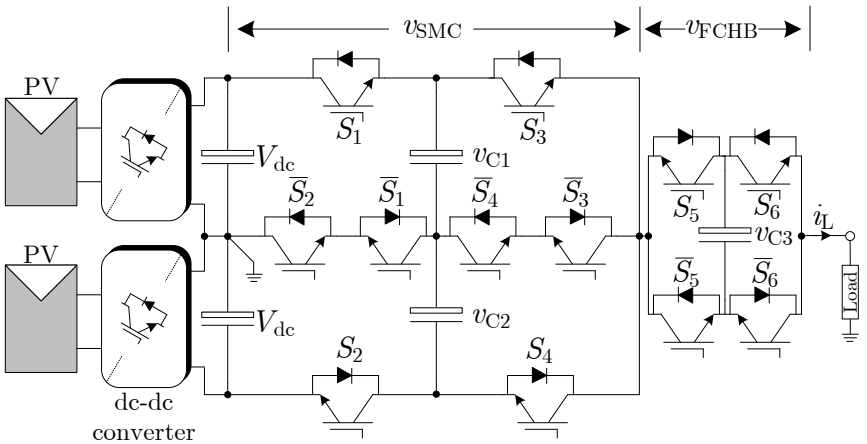


Figure 4.10: Simplified 12S-SMC MLI for one phase leg

where $\underline{S} = \begin{bmatrix} S_1 & S_2 & S_3 & S_4 & S_5 & S_6 \end{bmatrix}$ is the states of the switches. Applying Kirchhoffs voltage/current law to Figure 4.10 yields,

$$\frac{dV_{\text{C1}}}{dt} = \frac{(S_1 - S_3)}{C_1} \times i_{\text{L}}, \tag{4.20}$$

$$\frac{dV_{\text{C2}}}{dt} = \frac{(S_4 - S_2)}{C_2} \times i_{\text{L}}, \tag{4.21}$$

$$\frac{dV_{\text{C3}}}{dt} = \frac{(S_5 - S_6)}{C_3} \times i_{\text{L}}. \tag{4.22}$$

For the simplified model shown in Figure 4.10, the 5L SMC and 3L FCHB output voltages are expressed as a function of states of the switches and is given by

$$v_{\text{SMC}} = (S_1 + S_3)V_{\text{C1}} + (-S_2 - S_4)V_{\text{C2}} + (S_1 - S_2 + S_3 + S_4)V_{\text{dc}}, \tag{4.23}$$

$$v_{\text{FCHB}} = (S_6 - S_5)V_{\text{C3}}. \tag{4.24}$$

From (4.23) and (4.24), the output voltage is expressed as

$$v_{\text{SMC}} + v_{\text{FCHB}} = R_{\text{L}} i_{\text{L}} + L\frac{di_{\text{L}}}{dt}. \tag{4.25}$$

Substituting (4.23) and (4.24) in (4.25), the state-space model is obtained as

follows:

$$A(S(t)) = \begin{bmatrix} 0 & 0 & 0 & \frac{S_1 - S_3}{C_1} \\ 0 & 0 & 0 & \frac{S_4 - S_2}{C_2} \\ 0 & 0 & 0 & \frac{S_5 - S_6}{C_3} \\ \frac{S_1 + S_3}{L} & \frac{-S_2 - S_4}{L} & \frac{S_6 + S_5}{L} & \frac{R_L}{L} \end{bmatrix} \tag{4.26}$$

$$B(S(t)) = \begin{bmatrix} 0 & 0 & 0 & \left(\frac{S_1 - S_2 + S_3 - S_4}{L}\right) \end{bmatrix}^T \tag{4.27}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}^T \tag{4.28}$$

Chapter 5

MLIs RELIABILITY EVALUATION

5.1 Introduction

This chapter introduces the basic concepts of reliability and demonstrates the application of Markov chain-based evaluation method for the same. On the one hand, the reliability of the developed topologies is evaluated using part count method. On the other hand, the reliability of the developed topologies without and with FTC is computed using part stress method and are compared then after. The evaluation is carried out based on the simulated power losses obtained by keeping the system parameters unaltered and uniform among the topologies.

5.2 Fundamentals of reliability

One of the prime requisite features of MLIs or any power-electronic converter is the longer lifespan in addition to high efficiency, high-quality output waveform, smaller size and high power density. Converter with a higher lifespan is often considered to have a higher reliability which in general is defined as "the probability that a device fulfills its intended function (on state, off state and transitions) for a specific period of time within its safe operating area" (Defense, 1991). It is essential to determine the reliability of each part of the system as its reliability, in turn, depends on different factors and needs individual assessment. To assess the converter reliability,

the necessary definitions are revived first as below (Misra, 2012, Allan et al., 2013).

- Failure: It is when the system stops functioning in the desired fashion for any reason. It is categorized as sudden and gradual. In general, the failure-free operation is a random variable.

- Failure rate: It has a vital role in determining the system reliability and is defined as the ratio of the number of failures of a component for a given period of time to the total time of operation. It is commonly expressed as FIT, where one FIT refers to one failure in 10^9 operation hours. According to MIL-HDBK-217F standard (Defense, 1991), the probability distribution of failure of electronic devices (failure density function) is given as,

$$f(t) = \lambda e^{-\lambda t} \, (t > 0), \tag{5.1}$$

  where λ is the failure rate. Then the reliability function denoted by $R(t)$, is given as,

$$R(t) = 1 - \int_0^t f(t) \, dt = e^{-\lambda t}. \tag{5.2}$$

- MTTF: It is the average time before the occurrence of the first failure of a component following the system start. MTTF is obtained by integrating the reliability function for the interval [0, ∞] (Richardeau and Pham, 2013). It is usually estimated in hours and is one of the key specifications of a device or component. It is expressed mathematically as,

$$\text{MTTF} = \int_0^\infty R(t) \, dt = e^{-\lambda t} = \frac{1}{\lambda}. \tag{5.3}$$

5.3 Methodology

Several methods to evaluate the reliability of the system comprising of number of components have been proposed depending on the system's complexity and redundancy (Zhou and Smedley, 2009, Ding et al., 2010, Abdi et al., 2009). These methods can be broadly divided into:

1. Approximate or part count method: This is a straightforward way to estimate the system reliability. It requires less information, part quantities, quality level,

and the application environment. Assuming a typical operating condition referred to as reference condition of the system, the failure rates are predicted, thus the evaluation process leads to a more conservative estimate. The quantity of the component is of main focus while neglecting the actual operating conditions. As an example, for a simple power-electronic converter in the absence of redundancy or FTC, any failure in a single component leads to the failure of the converter itself which implies that the converter components can be viewed as a series connected system. It is customary to express the failure rate (λ_{system}) of such a system as,

$$\lambda_{\text{system}} = \sum_{i=1}^{\text{N}_\text{p}} \lambda_{\text{ref}(i)} \times \text{k}, \tag{5.4}$$

where "k" is the number of elements with the reference failure rate $\lambda_{\text{ref}(i)}$, and "N_p" is the number of parts.

2. Exact or part stress method: This method is based on measurements of the converter parameters. In contrast to the part count method, the operating condition of the system is not neglected and thus requires the knowledge of each specific part stress levels under various operating points. The total failure rate of the system using part stress method is given as,

$$\lambda_{\text{system}} = \sum_{i=1}^{\text{N}_\text{p}} \lambda_{\text{part}_i} \tag{5.5}$$

The failure rate of switch, diode and capacitor are calculated as,

$$\lambda_{\text{P}}^{\text{S}} = \lambda_{\text{B}}^{\text{S}} \times \pi_{\text{Q}} \times \pi_{\text{A}} \times \pi_{\text{E}} \times \pi_{\text{T}}, \tag{5.6}$$

$$\lambda_{\text{P}}^{\text{D}} = \lambda_{\text{B}}^{\text{D}} \times \pi_{\text{Q}} \times \pi_{\text{E}} \times \pi_{\text{C}} \times \pi_{\text{S}} \times \pi_{\text{T}}, \tag{5.7}$$

$$\lambda_{\text{P}}^{\text{C}} = \lambda_{\text{B}}^{\text{C}} \times \pi_{\text{CV}} \times \pi_{\text{Q}} \times \pi_{\text{E}}, \tag{5.8}$$

where the superscripts "S", "D", and "C" respectively corresponds to switch, diode and capacitor. The full set of equations required for calculating the failure rates of each of the above components is given in Appendix B.

Firstly, the reliability of the developed topologies is evaluated using part count method as described further. As per MIL-HDBK-217F the failure rate of the various components of the MLI is as follows: diode: 100; high voltage IGBT: 400 ; low voltage

Table 5.1: The MTTF for the proposed topologies using part count method

Components \ MLI	10S-TNPC	8S-TNPC	12S-ANPC	10S-ANPC	12S-SMC
IGBT	2 × 400+8 × 100	2 × 400+6 × 100	2 × 400+10 × 100	2 × 400+8 × 100	12 × 100
Capacitors	1 × 100	1 × 100	1 × 100	1 × 100	3 × 100
Diodes	12 × 100	8 × 100	12 × 100	10 × 100	12 × 100
Total FITs	2900	2300	3100	2700	2700
Failure rate (failure/10^6 Hours)	2.9	2.3	3.1	2.7	2.7
MTTF (Hours)	344,827	434,782	322,580	370,370	370,370

IGBT: 100; capacitors: 300. Further, the system failure rate is computed by multiplying each component's failure rate and the number of such components used, and summing all obtained values as per (5.4). Besides, to consider the worst condition, it is assumed to have an extra anti-parallel diode connected to each IGBT (Jahan et al., 2017). It is considered that power switches connected across the dc-link as HV switches and remaining all as LV. The corresponding number of components, failure rates, and computed approximate MTTF are listed in Table 5.1. It is evident from Table 5.1 that 8S-TNPC MLI has a better performance and highest MTTF value. This fact is apparent as 8S-TNPC MLI requires the least number of components among all. Upon further inspection, it is inferred that though 10S-ANPC MLI require lesser components than 12S-SMC MLI, the MTTF of both the topologies is same. Thus the computation of MTTF based on part count proves to be conservative and approximate, which calls for a detailed analysis to be performed using part stress method before making a concluding remark on the reliability of the topologies.

5.3.1 Markov reliability calculation approach

Markov reliability evaluation is one of the extensively used methods to determine the reliability of the system which can be discrete or continuous. It is in particular applicable to systems which are characterized by lack of memory, i.e., failure states are independent of past states of a system. It is well known that power electronic-converter is discrete, thereby support the seamless application of Markov method to evaluate its reliability. Markov evaluation method employs Markov chain to establish the relationships among the various operating states of a system right from full operation to its failure. The operating states of the system are related to each other through Markov chain transition (λ_{ij}); the frequency at which system goes to state j

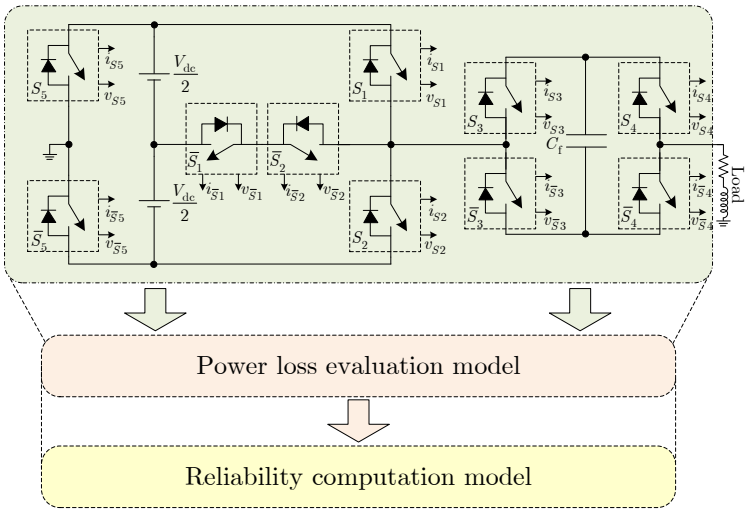


Figure 5.1: Power circuit of 10S-TNPC MLI without FTC and pictorial description of the steps involved in reliability evaluation

from i. The generalized steps involved in Markov reliability method is as follows:

- Obtain the power losses of all the switches (IGBT and anti-parallel diode). The method to compute the power losses is adopted from (Amer, 2014).
- Compute the junction temperature of each of the devices.
- Evaluate the factors ($\pi_{\mathrm{T}}, \pi_{\mathrm{S}}, \pi_{\mathrm{CV}}$, and $\lambda_{\mathrm{B}}^{\mathrm{C}}$) for all the components.
- Compute the aggregate failure rates ($\lambda_{\mathrm{P}}^{\mathrm{S}}, \lambda_{\mathrm{P}}^{\mathrm{D}}$, and $\lambda_{\mathrm{P}}^{\mathrm{C}}$) and the overall reliability henceforth.

5.4 Markov chain-based reliability evaluation of the proposed topologies without and with FTC

In this Section, all the proposed topologies with and without FTC are considered in detail and are assessed.

5.4.1 Reliability evaluation of 10S-TNPC MLI

The power circuit diagram of 10S-TNPC MLI along with the reliability evaluation methodology is shown in Figure 5.1. In the power circuit, failure of an element brings

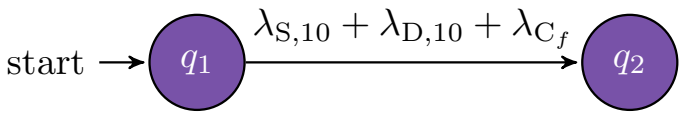


Figure 5.2: Markov chain diagram of the 10S-TNPC MLI without FTC

the complete MLI to standstill. Thus, two states can be identified as,

- q_1: The state where all the components are healthy ($P_1(t)$)
- q_2: The state where MLI fails ($P_2(t)$) owing to failure of one or more components

where $P_1(t)$, $P_2(t)$ are the occupational probability of state q_1 and q_2 respectively. The Markov chain transition rate is given by $\lambda_{S,10} + \lambda_{D,10} + \lambda_{C_f}$ (see Figure 5.2): where $\lambda_{S,10}$, $\lambda_{D,10}$, and λ_{C_f} represent the summation of failure rates of all switches, anti-parallel diodes, and one FC respectively. According to Figure 5.2, the probability of being in state q_1 at some time $t + \Delta t$ is equal to the probability of being in state q_1 at time t and not transitioning out during Δt, and is expressed mathematically as,

$$P_1(t + \Delta t) = P_1(t)[1 - \lambda \Delta t]. \tag{5.9}$$

Similarly, the probability of being in state q_2 at some time $t + \Delta t$ is equal to the probability of being in state q_1 at time t and transitioning to state q_2 in Δt plus the probability of being in state q_2 at time t and not transitioning out during Δt, and is given as,

$$P_2(t + \Delta t) = P_1(t)\lambda \Delta t + P_2(t)[1 - \lambda \Delta t], \tag{5.10}$$

Rearranging (5.9) and (5.10) yields,

$$\begin{aligned} \frac{P_1(t + \Delta t) - P_1(t)}{\Delta t} &= -\lambda P_1(t), \\ \frac{P_2(t + \Delta t) - P_2(t)}{\Delta t} &= \lambda P_1(t). \end{aligned} \tag{5.11}$$

The matrix representation of (5.11) is given as,

$$\frac{d}{dt}[P_1(t)\ P_2(t)] = [P(t)] \times [A] = [P_1(t)\ P_2(t)] \begin{bmatrix} -\lambda & \lambda \\ 0 & 0 \end{bmatrix}$$

Table 5.2: Parameters employed for the simulation

V_{dc}	$R-L$	C_{f}	f_{sw}
500 V	10 Ω - 10 mH	3.3 mF	2.5 kHz

Table 5.3: Power loss (W) of components

S_1	$\bar{S}_1$	S_2	$\bar{S}_2$	S_3	$\bar{S}_3$	S_4	$\bar{S}_4$	S_5	$\bar{S}_5$
21.4494	10.8164	17.9250	5.7657	21.2710	13.7331	4.3728	12.4620	22.4678	22.3018
D_1	$\bar{D}_1$	D_2	$\bar{D}_2$	D_3	$\bar{D}_3$	D_4	$\bar{D}_4$	D_5	$\bar{D}_5$
1.9940	4.6061	1.2369	11.0913	11.7743	3.5376	12.6860	20.7463	0.0825	0.0825

Table 5.4: Failure rate of components

S_1	$\bar{S}_1$	S_2	$\bar{S}_2$	S_3	$\bar{S}_3$	S_4	$\bar{S}_4$	S_5	$\bar{S}_5$
7.2514	6.8869	7.1292	6.7181	7.2452	6.9857	6.6721	6.9425	7.2870	7.2812
D_1	$\bar{D}_1$	D_2	$\bar{D}_2$	D_3	$\bar{D}_3$	D_4	$\bar{D}_4$	D_5	$\bar{D}_5$
0.4715	0.0895	0.4683	0.0947	0.0177	0.0165	0.0178	0.0191	0.4636	0.4636

,

where the system is assumed to start intially from state q_1 i.e., $P(0) = [1\ 0]$.

Once the TM is obtained, the reliability of the system can be obtained as,

$$R(t) = P_1(t) = e^{-\lambda t} = e^{-(\lambda_{\mathrm{S},10}+\lambda_{\mathrm{D},10}+\lambda_{\mathrm{C}_f})}. \tag{5.12}$$

The parameters of the system employed in the simulation are listed in Table 5.2. With the considered parameters, the obtained power losses are indicated in Table 5.3. The so computed failure rate of each of the components using the formulations as given in Appendix B are shown in Table 5.4. Thus, the reliability function and MTTF are:

$$R(t) = P_1(t) = e^{-72.94t} \text{ and}$$
$$\text{MTTF} = \frac{1}{\lambda} = 0.0137 \times 10^6 \text{ Hours}.$$

Further, the reliability of 10S-TNPC MLI is evaluated by imparting the FTC into it. As a part of fault tolerance, two relays namely R_1 and R_2 are added as shown

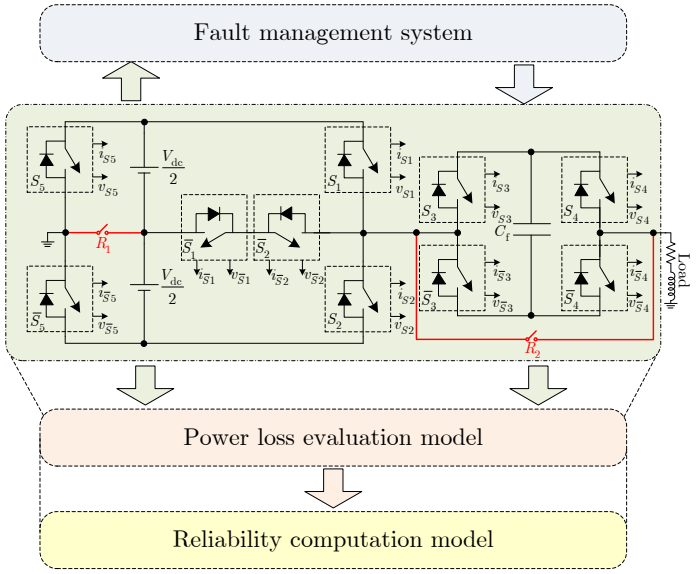


Figure 5.3: Power circuit of the 10S-TNPC MLI with FTC

in Figure 5.3. The whole MLI is considered to be made of three parts: 3L-TNPC unit, 3L-FCHB unit, and 2L-LFS unit. The 3L-TNPC is the fundamental unit that needs to be in continuous operation and a fault in it brings the whole system to rest (Gautam et al., 2017). The appended relays are a normally open type, and they are connected in a way that facilitates the isolation of faulty section from the whole system and ensures normal operation of the MLI with the remaining. To successfully enable the system to operate in various states post-fault, a fault management system is imperative. The primary function of which is to detect and manage the suitable relay leading to the fault isolation. There are many fault diagnosis methods available in the literature (Keswani et al., 2015, Gan et al., 2016), however, owing to the present context, their analysis is out of the scope of this study. Figure 5.4 shows a simple logic circuit developed to alter and adjust the operation of MLI depending upon the occurrence of the fault. The comparator and the level generator is responsible for the generation of reference steeped voltage to be produced at the output of MLI. The gating signals are generated by the switching pulse decoder depending upon the voltage levels and the FC voltage balancing controller input. With respect to Figure 5.3, there are four states of operation as mentioned below and the corresponding Markov chain diagram is illustrated in Figure 5.5.

- q_1: The state where all the components are healthy $(P_1(t))$

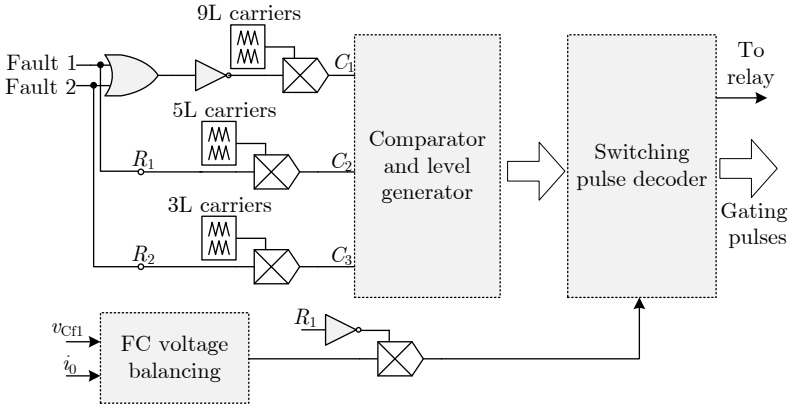


Figure 5.4: Simplified logic diagram of the developed FMS

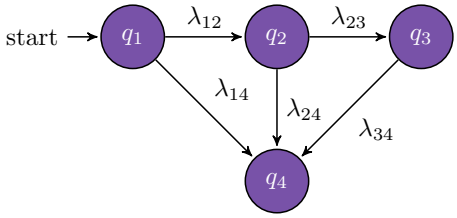


Figure 5.5: Markov chain diagram of the 10S-TNPC MLI with FTC

- q_2: The state where FCHB fails and is bypassed ($P_2(t)$)

- q_3: The state where LFS fails and is bypassed post failure of FCHB ($P_3(t)$)

- q_4: The state where TNPC unit fails leading to the failure of whole MLI ($P_4(t)$)

According to Figure 5.5, the system equation, TM and the failure rates are given as,

$$\frac{d}{dt}[P_1(t)\ P_2(t)\ P_3(t)\ P_4(t)] = [P_1(t)\ P_2(t)\ P_3(t)\ P_4(t)] \times [\mathrm{A}]\,,$$

$$[\mathrm{A}] = \begin{bmatrix} -(\lambda_{12}+\lambda_{14}) & \lambda_{12} & 0 & \lambda_{14} \\ 0 & -(\lambda_{23}+\lambda_{24}) & \lambda_{23} & \lambda_{24} \\ 0 & 0 & -\lambda_{34} & \lambda_{34} \\ 0 & 0 & 0 & 0 \end{bmatrix},$$

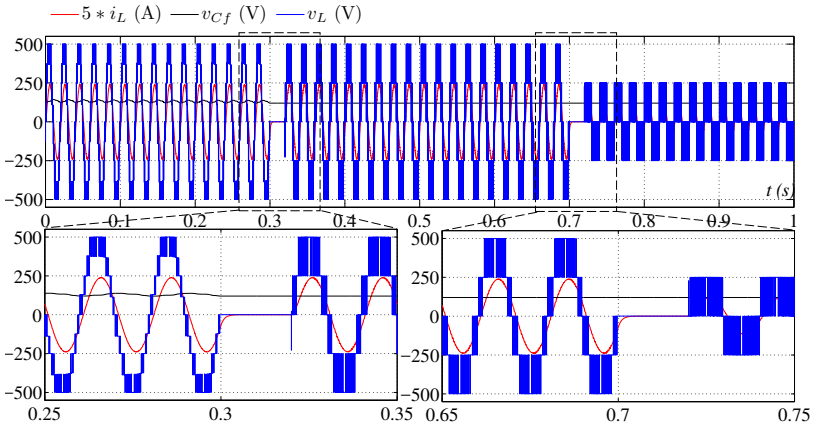


Figure 5.6: Ouput voltage, load current and FC voltage of the proposed 10S-TNPC MLI with FTC

$$
\begin{aligned}
\lambda_{12} &= (\lambda_{\mathrm{S},10} + \lambda_{\mathrm{D},10} + \lambda_{\mathrm{C}_f}) \times P_{\mathrm{R}}, \\
\lambda_{14} &= (\lambda_{\mathrm{S},10} + \lambda_{\mathrm{D},10} + \lambda_{\mathrm{C}_f}) \times (1 - P_{\mathrm{R}}), \\
\lambda_{23} &= (\lambda^{'}_{\mathrm{S},6} + \lambda^{'}_{\mathrm{D},6}) \times P_{\mathrm{R}}, \\
\lambda_{23} &= (\lambda^{'}_{\mathrm{S},6} + \lambda^{'}_{\mathrm{D},6}) \times (1 - P_{\mathrm{R}}), \\
\lambda_{34} &= (\lambda^{''}_{\mathrm{S},4} + \lambda^{''}_{\mathrm{D},4}).
\end{aligned}
\tag{5.13}
$$

where λ_{12} is the rate at which Markov chain transits from state q_1 to state q_2, λ_{23} is the rate at which Markov chain transits from state q_2 to state q_3, λ_{34} is the rate at which Markov chain transits from state q_{13} to state q_4. λ_{14} and λ_{24} respectively are the rate at which Markov chain transits from state q_1 to state q_4 and state q_2 to state q_4. The probability that FMS can manage the fault (P_{R}) is assumed to be 0.9 (Haji-Esmaeili et al., 2017a). The corresponding parts of failure rates of each Markov transitions is given in (5.13). $\lambda_{\mathrm{S},10}, \lambda^{'}_{\mathrm{S},6}$, and $\lambda^{''}_{\mathrm{S},4}$ respectively are the summation of failure rates of switches when the MLI is in healthy condition, post-fault in FCHB, and post-fault in LFS unit. Same holds good for diodes and FC in (5.13). Figure 5.6 shows the output voltage, voltage across FC and load current of the proposed 10S-TNPC MLI with FTC employing the parameters listed in Table 5.2. It is evident from the simulation results that initially, the circuit is in a healthy state, generating a 9L output voltage with a well regulated FC voltage. At $t = 0.3$ s, fault-1 (fault in FCHB unit) occurs. After the occurrence of a fault, the FCHB unit is bypassed, and the gating signals

to the power switches $S_3, \bar{S}_3, S_4$ and $\bar{S}_4$ are blocked. After accomplishing the first fault-tolerant operation, the MLI generates a 5L output voltage with the remaining power circuit. At $t = 0.7$ s, fault 2 (fault in LFS unit) occurs. As a response, the FMS operates the relay R_2 and bypasses the LFS unit and the gating signal to the power switches S_5 and $\bar{S}_5$ are blocked. The MLI continues to operate as a 3L inverter. It is to be mentioned that the FMS is assumed to require one cycle (20 ms) to diagnose and establish the further operating mode (Haji-Esmaeili et al., 2017b). Besides, the reliability of the 10S-TNPC MLI with FTC is evaluated by using the failure rate of each component in different states. The corresponding TM obtained is given as,

$$[\mathrm{A}] = \begin{bmatrix} -72.94 & 65.65 & 0 & 7.29 \\ 0 & -45.14 & 40.63 & 4.52 \\ 0 & 0 & -28.65 & 28.65 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

Once the TM is computed, the probabilities are calculated using the initial condition $P(0) = [1\,0\,0\,0]$ is as follows:

$$P(t) = L^{-1}(\,[SI - A]^{-1}\,) \times P(0). \tag{5.14}$$

The calculated probabilities using (5.14) are given as,

$$\begin{aligned} P_1(t) &= e^{-72.94t}, \\ P_2(t) &= 2.36(e^{-45.15t} - e^{-72.94t}), \\ P_3(t) &= 2.17e^{-72.95t} - 5.819e^{-45.15t} + 3.65e^{-28.657t}, \\ R(t) &= P_1(t) + P_2(t) + P_3(t) \\ &= 0.805e^{-72.94t} - 3.46e^{-45.15t} + 3.65e^{-28.65t}. \end{aligned}$$

The reliability curve of the 10S-TNPC MLI without and with FTC are shown in Figure 5.7. It is apparent that MLI with FTC has a better reliability.

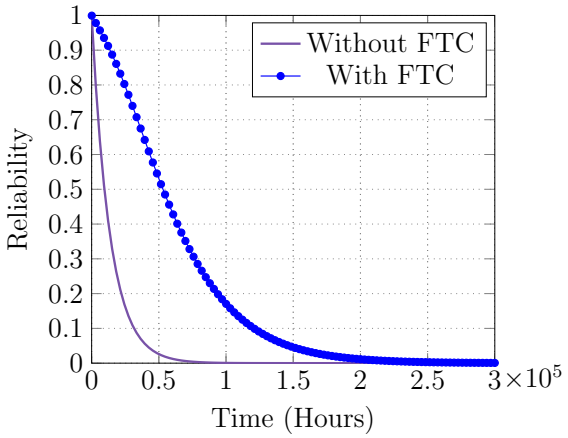


Figure 5.7: Reliability curve of 10S-TNPC without and with FTC

5.4.2 Reliability evaluation of 8S-TNPC MLI

The power circuit diagram of 8S-TNPC MLI along with the reliability evaluation methodology is shown in Figure 5.8. The corresponding Markov chain diagram for the 8S-TNPC MLI is similar to that of 10S-TNPC MLI (refer Figure 5.5). The related failure rate transitions are defined as,

$$\begin{aligned}
\lambda_{12} &= (\lambda_{\mathrm{S},8} + \lambda_{\mathrm{D},8} + \lambda_{\mathrm{C}_f}) \times P_R, \\
\lambda_{14} &= (\lambda_{\mathrm{S},8} + \lambda_{\mathrm{D},8} + \lambda_{\mathrm{C}_f}) \times (1 - P_{\mathrm{R}}), \\
\lambda_{23} &= (\lambda'_{\mathrm{S},6} + \lambda'_{\mathrm{D},6}) \times P_{\mathrm{R}}, \\
\lambda_{23} &= (\lambda'_{\mathrm{S},6} + \lambda'_{\mathrm{D},6}) \times (1 - P_{\mathrm{R}}), \text{ and} \\
\lambda_{34} &= (\lambda''_{\mathrm{S},4} + \lambda''_{\mathrm{D},6}).
\end{aligned}$$

The corresponding TM is given as,

$$[\mathrm{A}] = \begin{bmatrix} -59.12 & 53.21 & 0 & 5.91 \\ 0 & -45.14 & 40.63 & 4.52 \\ 0 & 0 & -28.65 & 28.65 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

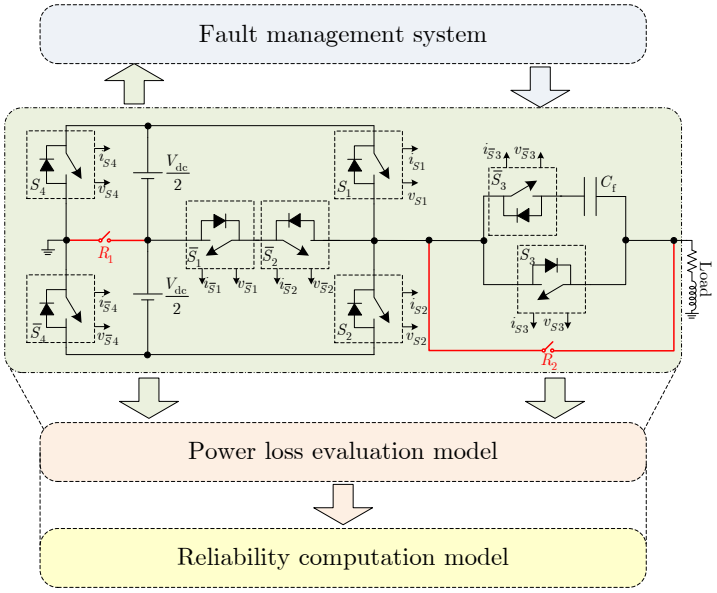


Figure 5.8: 8S-TNPC with FTC

The calculated probabilities are given as,

$$
\begin{aligned}
P_1(t) &= e^{-59.13t}, \\
P_2(t) &= 3.8(e^{-45.15t} - e^{-59.13t}), \\
P_3(t) &= 4.3e^{-28.66t} - 9.37e^{-45.15t} + 5.07e^{-59.13t}, \\
R(t) &= P_1(t) + P_2(t) + P_3(t) \\
&= 2.26e^{-59.13t} - 5.56e^{-45.15t} + 4.3e^{-28.65t}
\end{aligned}
$$

From the above equations, the reliability of 8S-TNPC MLI without FTC is $e^{-59.13t}$. The pictorial representation of the reliability curves of the 8S-TNPC MLI without and with FTC are compared in Figure 5.9. The comparison of results in Figure 5.7 and Figure 5.9 confirms the improved reliability of 8S-TNPC MLI, owing to its reduced number of switches.

5.4.3 Reliability evaluation of 12S-ANPC MLI

The power circuit diagram of 12S-ANPC MLI along with the reliability evaluation methodology is shown in Figure 5.10. The corresponding Markov chain diagram for the 12S-ANPC MLI is similar to that of 10S-TNPC MLI (see Figure 5.5) with the

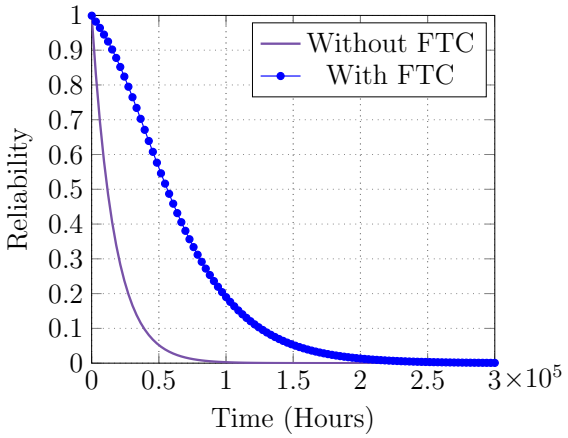


Figure 5.9: Reliability curve of 8S-TNPC without and with FTC

following states identified:

- q_1: The state where all the components are healthy ($P_1(t)$)
- q_2: Fault in FCHB cell and the relay R_2 operates ($P_2(t)$)
- q_3: Fault in LFS unit and the relay R_1 operates ($P_3(t)$)
- q_4: Fault in ANPC and whole system fails

The failure rate transitions are given as,

$$\begin{aligned}
\lambda_{12} &= (\lambda_{\mathrm{S},12} + \lambda_{\mathrm{D},12} + \lambda_{\mathrm{C}_f}) \times P_{\mathrm{R}}, \\
\lambda_{14} &= (\lambda_{\mathrm{S},12} + \lambda_{\mathrm{D},12} + \lambda_{\mathrm{C}_f}) \times (1 - P_{\mathrm{R}}), \\
\lambda_{23} &= (\lambda^{'}_{\mathrm{S},8} + \lambda^{'}_{\mathrm{D},8}) \times P_{\mathrm{R}}, \\
\lambda_{23} &= (\lambda^{'}_{\mathrm{S},8} + \lambda^{'}_{\mathrm{D},8}) \times (1 - P_{\mathrm{R}}), \text{ and} \\
\lambda_{34} &= (\lambda^{''}_{\mathrm{S},6} + \lambda^{''}_{\mathrm{D},6}).
\end{aligned}$$

The computed TM is given as,

$$[\mathrm{A}] = \begin{bmatrix} -86.753 & 78.078 & 0 & 8.67 \\ 0 & -58.71 & 52.84 & 5.87 \\ 0 & 0 & -43.01 & 43.01 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

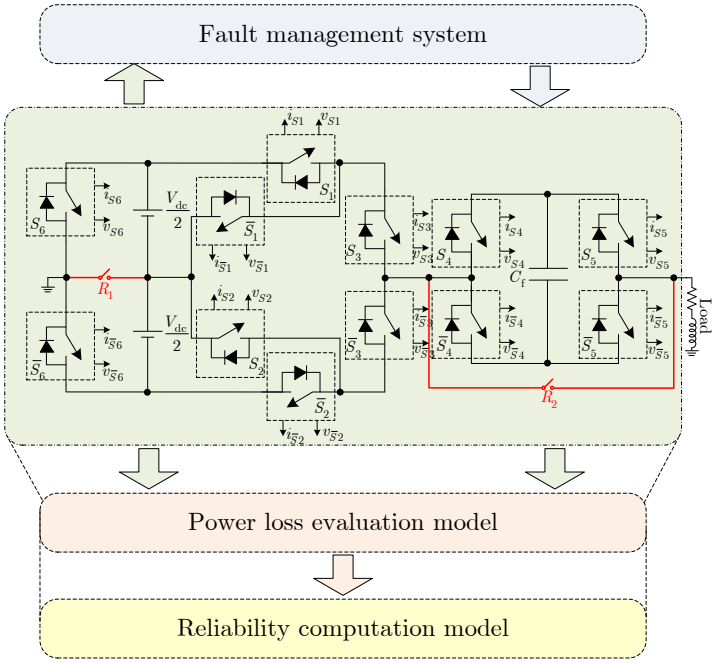


Figure 5.10: 12S-ANPC with FTC

Two different sequence of operating modes is considered to demonstrate the satisfactory performance of the FMS and the developed FC voltage balancing controller. Firstly, the fault is assumed to emerge in FCHB and then in LFS unit, referred to as sequence-1. Secondly, the fault is assumed to emerge in LFS unit and then in FCHB unit, referred to as sequence-2. The corresponding results are shown in Figure 5.11(a) and Figure 5.11(b) respectively. As evident from Figure 5.11(b), post-fault in LFS unit, the MLI generates 5L voltage while the FC voltage is well regulated around the reference value within a cycle time confirms the successful operation of FMS and FC voltage regulator. The reliability so obtained considering the computed TM is as follows:

$$
\begin{aligned}
P_1(t) &= e^{-86.75t}, \\
P_2(t) &= 2.78(e^{-58.71t} - e^{-86.75t}), \\
P_3(t) &= 6.06e^{-43.01t} - 9.369e^{-58.71t} + 3.36e^{-86.75t}, \text{ and} \\
R(t) &= P_1(t) + P_2(t) + P_3(t) \\
&= 1.58e^{-86.75t} - 6.58e^{-58.71t} + 6.06e^{-43.01t}.
\end{aligned} \tag{5.15}
$$

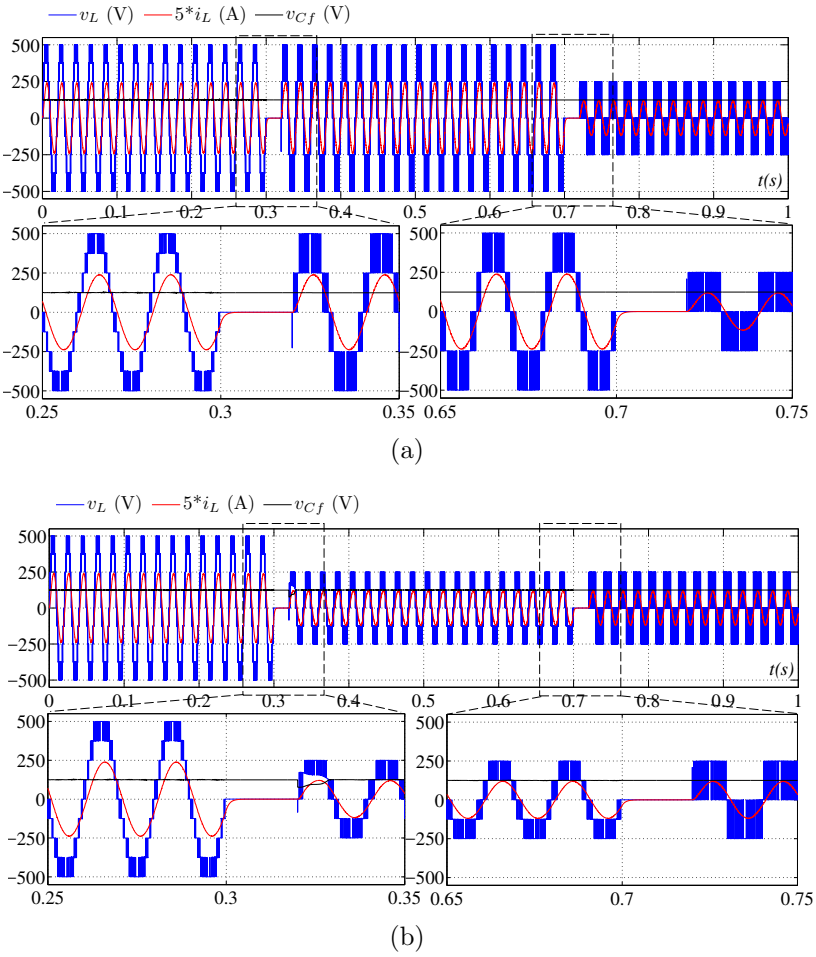


Figure 5.11: Ouput voltage, load current and FC voltage of the proposed 12S-ANPC MLI with FTC for (a) sequence-1 mode operation and (b) sequence-2 mode operation

From (5.15) the reliability of 12S-ANPC MLI without FTC is $e^{-86.75t}$. The reliability curves without and with FTC are compared in Figure 5.12.

5.4.4 Reliability evaluation of 10S-ANPC MLI

The power circuit of 10S-ANPC MLI with reliability evaluation scheme is shown in Figure 5.13. As apparent from the circuit, it mainly comprises of only two sections, 5L-ANPC unit and LFS unit. Therefore, a single relay R_1 is employed for imparting the FTC. The following are the valid state of operation:

- q_1: The state where all the components are healthy $(P_1(t))$
- q_2: Fault in LFS unit and the relay R_1 operates $(P_2(t))$

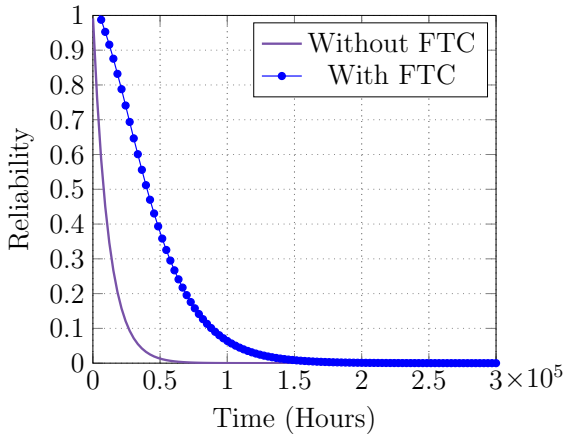


Figure 5.12: Reliability curve of 12S-ANPC with and without FTC

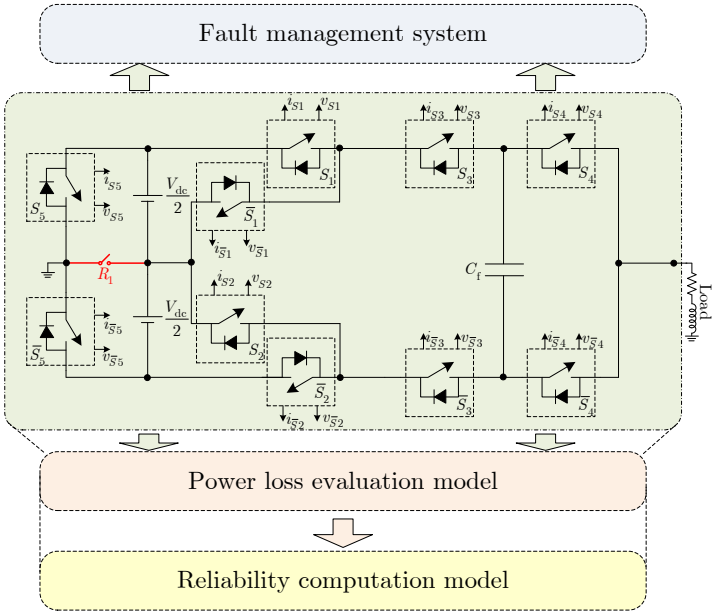


Figure 5.13: 10S-ANPC with FTC

- q_3: Fault in ANPC and whole system fails

The corresponding Markov chain diagram is shown in Figure 5.14 and the failure rate transitions and TM are given as,

$$\lambda_{12} = (\lambda_{\mathrm{S},10} + \lambda_{\mathrm{D},10} + \lambda_{\mathrm{C}_f}) \times P_{\mathrm{R}},$$
$$\lambda_{13} = (\lambda_{\mathrm{S},10} + \lambda_{\mathrm{D},10} + \lambda_{\mathrm{C}_f}) \times (1 - P_{\mathrm{R}}), \text{ and}$$
$$\lambda_{23} = (\lambda^{'}_{\mathrm{S},8} + \lambda^{'}_{\mathrm{D},8}).$$

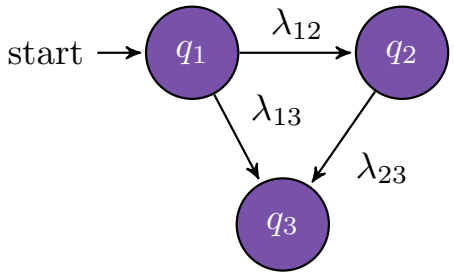


Figure 5.14: Markov chain diagram of the 10S-ANPC MLI with FTC

$$[A] = \begin{bmatrix} -(\lambda_{12}+\lambda_{13}) & \lambda_{12} & \lambda_{13} \\ 0 & -\lambda_{23} & \lambda_{23} \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} -72.94 & 65.642 & 7.29 \\ 0 & -55.47 & 55.47 \\ 0 & 0 & 0 \end{bmatrix}.$$

Using the TM, the reliability of 10S-ANPC MLI without and with FTC respectively is $e^{-72.94t}$ and given as,

$$\begin{aligned} P_1(t) &= e^{-72.94t}, \\ P_2(t) &= 3.756(e^{-55.47t} - e^{-72.94t}), \text{ and} \\ R(t) &= P_1(t) + P_2(t) + P_3(t) \\ &= 3.76e^{-55.47t} - 2.75e^{-72.94t}. \end{aligned}$$

5.4.5 Reliability evaluation of 12S-SMC MLI

The circuit topology of the 12S-SMC MLI with reliability evaluation scheme is shown in Figure 5.15. The Markov chain diagram is same as that of Figure 5.14. The following are the valid state of operation:

- q_1: The state where all the components are healthy ($P_1(t)$)
- q_2: Fault in LFS unit and the relay R_1 operates ($P_2(t)$)
- q_3: Fault in SMC and whole system fails

The system performance during pre-fault and post-fault condition is demonstrated in Figure 5.16. After the occurrence of a fault at $t = 0.1$ s, the FCHB is bypassed, and

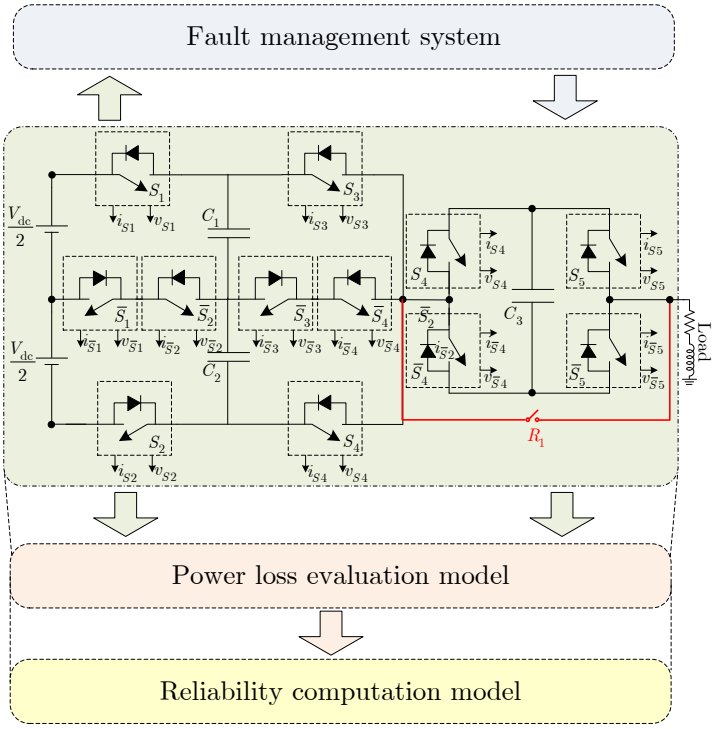


Figure 5.15: 12S-SMC with FTC

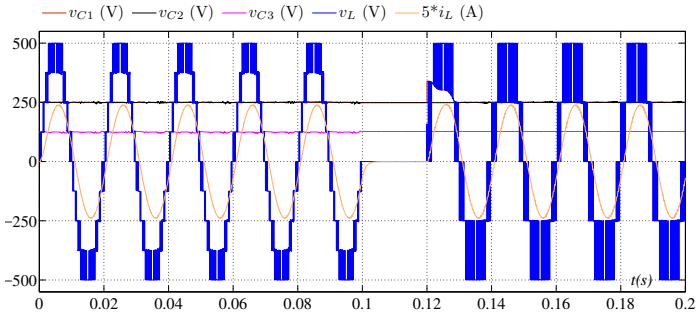


Figure 5.16: Ouput voltage, load current and FC voltage of the proposed 12S-SMC MLI with FTC

the voltage across FC remains intact. Further, the voltage across flying capacitors C_1 and C_2 are regulated and held tightly at their reference value. The Markov chain transitions and the corresponding TM are given as follows:

$$\lambda_{12} = (\lambda_{\mathrm{S},12} + \lambda_{\mathrm{D},12} + \lambda_{C_1} + \lambda_{C_2} + \lambda_{C_3}) \times P_{\mathrm{R}},$$
$$\lambda_{13} = (\lambda_{\mathrm{S},12} + \lambda_{\mathrm{D},12} + \lambda_{C_1} + \lambda_{C_2} + \lambda_{C_3}) \times (1 - P_{\mathrm{R}}), \text{ and}$$
$$\lambda_{23} = (\lambda^{'}_{\mathrm{S},8} + \lambda^{'}_{\mathrm{D},8} + \lambda_{C_1} + \lambda_{C_2}).$$

$$[A] = \begin{bmatrix} -87.37 & 78.63 & 8.73 \\ 0 & -59.61 & 59.61 \\ 0 & 0 & 0 \end{bmatrix}$$

The reliability of the 12S-SMC MLI computed using the above TM is given as,

$$\begin{aligned} P_1(t) &= e^{-87.38t}, \\ P_2(t) &= 2.83(e^{-59.61t} - e^{-87.37t}), \text{ and} \\ R(t) &= P_1(t) + P_2(t) + P_3(t) \\ &= 2.83e^{-59.61t} - 1.83e^{-87.37t}. \end{aligned}$$

5.4.6 Comparison of reliability of the proposed topologies

Based on the reliability function obtained for all the proposed topologies, the distinction in their reliability characteristics is plotted and compared. In general, it becomes advantageous to compare the topologies based on the MTTF value and thus, the MTTF of the MLIs with FTC is calculated as follows: As an example consider the following case of TM given as,

$$[A] = \begin{bmatrix} -86.753 & 78.078 & 0 & 8.67 \\ 0 & -58.71 & 52.84 & 5.87 \\ 0 & 0 & -43.01 & 43.01 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

The truncated matrix excluding the absorbing state q_4 from $[A]$ is obtained as,

$$[Q] = \begin{bmatrix} -86.753 & 78.078 & 0 \\ 0 & -58.71 & 52.84 \\ 0 & 0 & -43.01 \end{bmatrix}$$

Finally, MTTF can be calculated by summing all entries of first row of $[I - Q]^{-1}$ where $[I]$ is an identity matrix of order same as $[Q]$ (Allan et al., 2013). Figure 5.17 shows the reliability curves of the proposed topologies with and without FTC. The following observations are made:

- Without FTC, the MLI topologies 10S-TNPC and 10S-ANPC are found to exhibit similar reliability characteristics. The same holds good for the MLI

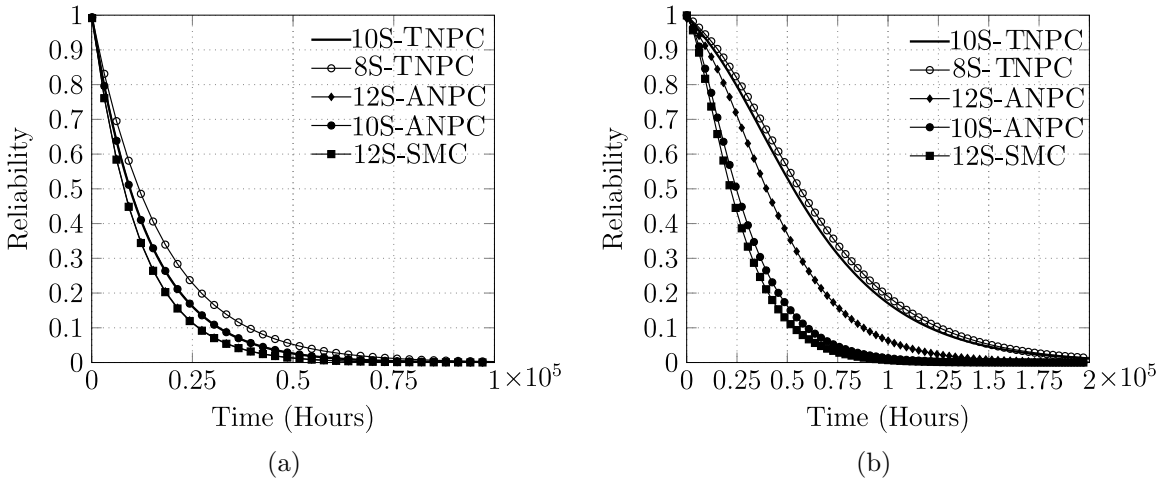


Figure 5.17: Comparison of reliability curves of the proposed topologies (a) without FTC (b) with FTC

Table 5.5: Comparison of MTTF of the proposed topologies with FTC

MLI	10S-TNPC	8S-TNPC	12S-ANPC	10S-ANPC	12S-SMC
MTTF (Hours)	0.0591×10^6	0.0621×10^6	0.0442×10^6	0.0292×10^6	0.026×10^6

topologies 12S-ANPC and 12S-SMC. Owing to the least part count the 8S-TNPC MLI has better reliability condition in comparison to all.

- Equipped with FTC, the 10S-TNPC and 8S-TNPC MLIs exhibit near same reliability characteristics. Followed by the 12S-ANPC MLI. However, though the 10S-ANPC MLI require lesser part count in comparison to that of 12S-ANPC, its reliability is lesser as it lacks redundancy. The 12S-SMC is found to demonstrate the least reliability among all. Thus, it worth noting that in addition to the lesser number of components it is vital to preserve the modularity of the MLI in order to have a higher reliability performance.

Further, the MTTF of the proposed topologies evaluated using the mthod above discussed is tabulated in the Table 5.5. By comparing the MTTF values enlisted, the 8S-TNPC MLI is found to have the highest MTTF as expected from the reliability curves.

Chapter 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

Recently, as a result of enormous research and development in the field of MLIs, their presence in industries over a wide-ranging application is noticeable. Many topological and control issues of MLIs have been studied and described. Though significant efforts are made in reducing the complexity of MLIs, there exists a way to develop alternate solutions which further lessens the operational and control challenges. Among the existing topologies, there is a need to investigate, understand the properties and propose suitable modifications making them more adaptable depending on the applications. For low and medium-power applications, especially in grid-connected renewable systems, the power quality standard are very stringent, and one of the ways to comply is by employing bulky passive filters. In such cases, use of an MLI with a higher number of output voltage levels is more logical. However, it would be a more challenging task since it escalates the structural and control complexity. With this thought, the main contributions of this thesis were the proposal and verification of three variety of modifications for three different converters catering to low- and medium-power level with suitable uncomplicated control strategies. The general conclusion of each chapter has been collected as the following:

In Chapter 1, a review of MLIs including the classic, not-so-classic, emerging and hybrid topologies has been performed. As an outcome, it was learned that despite

many solutions capable of generating more number of voltage levels, an opportunity for developing an alternative way of achieving the same endures. From the literature three potential converter topologies, TNPC MLI suitable for low-power, ANPC and SMC MLIs suitable for high-power applications were chosen for hybridization.

In Chapter 2, firstly a method to extend the 3L-TNPC MLI to output 9L voltage waveform is demonstrated by appending a 3L-FCHB and using a 2L converter leg units referred to as 10S-TNPC MLI. The structural details of the devised topology and operating principles are detailed. Further, a sensorless voltage balancing technique to regulate the FC voltage at the desired value is implemented which enables the system to be devoid of both voltage and current sensor(s). A detailed case study considering the single-phase grid-connected operation is investigated. Following which the developed topology is simulated and experimentally verified feeding a passive $R-L$ load. The adapted sensorless control allows the MLI to generate the multilevel waveform and has proven advantageous in comparison to complex cost function-based control strategies. Further, an upgraded i.e., a further reduced component count topology is derived from the previously developed topology. The operating principle, simulation and experimental results match with that of the previous topology while requiring two lesser number of switches. Finally, both the topologies were compared against the state-of-the-art MLIs proving their potential merits.

Modified ANPC topologies have been proposed in Chapter 3. On the one hand, a 3L-ANPC MLI was hybridized by combining it with a 3L-FCHB and 2L converter units referred to as 12S-ANPC MLI. With the aid of sufficient redundant switching states, a sensor-based control scheme to regulate the voltage across FC for which LFE were developed. Simulation and experimental results confirmed the theory of operation and control strategy. The methods to extend the topology for higher voltage levels is studied. On the other hand, the developed second variant referred to as 10S-ANPC MLI is the first ever topology with the reduced part count requiring least structural disruption of a 5L-ANPC MLI. Following the three-phase grid-connected operation, the obtained results confirmed the satisfactory performance. Further, a detailed comparison of the proposed topologies pertaining to the medium-power level application is performed. The comparative study distinguished the developed topologies among other popular ones highlighting their ability in overcoming some of the shortcomings in the available solutions.

Chapter 4 illustrated the hybrid 9L-SMC MLI devised as an amalgamation of

the 3L-FCHB unit and the undervalued 5L-SMC owing to its higher components requirement for higher voltage levels. This newly developed solution enables the classic 5L-SMC to generate a large number of output voltage levels with a reduced number of components, compared to many traditional solutions and in that sense, it can be regarded as an unprecedented solution. A detailed three-phase grid-connected case study with the hybrid SMC MLI and the LFE-based voltage balancing controller have shown encouraging results for the performance of the control strategy. Finally, the comparison of results have demonstrated some of the promising features of the hybrid SMC MLI against others.

In chapter 5, a systematic and detailed evaluation of the reliability is done as well. Both the part count and part stress method of reliability evaluation of the proposed topologies is accomplished. Furthermore, the operation of each of the topologies is considered under failure conditions of one or more of its subsystem is investigated. A simple method of reconfiguration is applied to sustain the continuous operation of the circuit. Simulation results validate the fault-tolerant operation. Besides, the reliability evaluated for each of the developed topologies with and without FTC is compared. The result shows that reliability of the topologies with FTC is higher than that of without FTC. The reason behind the exclusion of classic topologies in the reliability study is that they require higher part count and are apparent to exhibit lesser reliability than the developed ones.

6.2 Future scope

Based on the research carried out in this thesis, the recommendations for future research are as follows:

- To investigate the application of the presented hybridization technique to other MLIs thereby, resulting in many other interesting topologies.
- To integrate the proposed PWM methods with dc-link ripple voltage minimization techniques for additional improvement in output voltage quality by eliminating the low-frequency voltage ripples, and thereby, reducing the capacitance of the FCs.
- To investigate and employ FC voltage estimation-based methods, and then,

based on the estimated value, the voltage across the FC can be regulated instantaneously leading to a reduced sensing efforts and cost.

- To further study the device level fault-tolerant capabilities pertaining to the proposed topologies. Besides, inclusion of additional reliability constraints and other reliability functions helps in a more precisive quantification of the developed topologies.
- Performance and cost comparison of the developed topologies by considering hybrid semiconductor devices against uniform devices can be further studied and can be extended to other hybrid MLIs as well.

Appendix A

PROOF OF SELF VOLTAGE BALANCING

As mentioned in chapter 2, except for the levels $\pm V_{\mathrm{dc}}/2$, 0, and $\pm V_{\mathrm{dc}}$, the FC is connected in series with the load and source. Thus is either charged or discharged depending on the direction of load current. Figure A.1 depicts one cycle of typical output voltage and current waveform of a MLI.

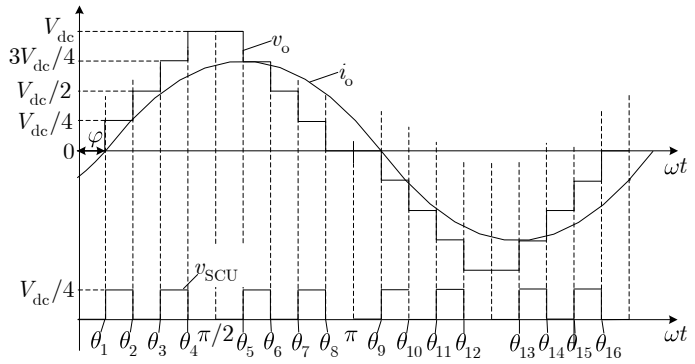


Figure A.1: Generic output voltage of a multilevel inverter controlled using fundamental switching method.

Assuming the output voltage and load current as,

$$v_{\mathrm{o}}(t) = V_{\mathrm{m}} \sin(\omega t) \tag{A.1}$$

$$i_{\mathrm{o}}(t) = I_{\mathrm{m}} \sin(\omega t - \phi) \tag{A.2}$$

where V_{m} and I_{m} are the peak values of the output voltage and load current respec-

tively, ϕ is the phase angle difference between them. The energy absorbed or delivered to the load by the FC is expressed as,

$$E = \int V I \, dt \tag{A.3}$$

where V, I and E are voltage, current, and energy of the FC respectively. The energy associated with the FC during positive and negative half cycle of the output voltage can be derived as follows,

$$\begin{aligned}
E^{+} &= \int_{0}^{\pi} V_{\mathrm{SCU}} \, I_{\mathrm{m}} \, \sin(\omega t - \phi) \\
&= I_{\mathrm{m}} \int_{0}^{\pi} V_{\mathrm{SCU}} \, \sin(\omega t - \phi) \\
&= I_{\mathrm{m}} \times V_{\mathrm{dc}}/4 \left[\int_{\theta_1}^{\theta_2} \sin(\omega t - \phi) + \int_{\theta_3}^{\theta_4} \sin(\omega t - \phi) + \int_{\theta_5}^{\theta_6} \sin(\omega t - \phi) + \int_{\theta_7}^{\theta_8} \sin(\omega t - \phi) \right] \\
&= I_{\mathrm{m}} \times V_{\mathrm{dc}}/4 \, [\cos(\theta_1 - \phi) - \cos(\theta_2 - \phi) + \cos(\theta_3 - \phi) - \cos(\theta_4 - \phi) \\
&\qquad + \cos(\theta_5 - \phi) - \cos(\theta_6 - \phi) + \cos(\theta_7 - \phi) - \cos(\theta_8 - \phi)] \qquad \text{(A.4)} \\
&= I_{\mathrm{m}} \times V_{\mathrm{dc}}/4 \, [\cos(\theta_1 - \phi) - \cos(\theta_2 - \phi) + \cos(\theta_3 - \phi) - \cos(\theta_4 - \phi) \\
&\qquad + \sin(\theta_1 - \phi) - \sin(\theta_2 - \phi) + \sin(\theta_3 - \phi) - \sin(\theta_4 - \phi)] \, . \qquad \text{(A.5)}
\end{aligned}$$

The final expression for E^{+} in (5) is obtained by substituting $\theta_5 = \theta_1 + \pi/2$, $\theta_6 = \theta_2 + \pi/2$, $\theta_7 = \theta_3 + \pi/2$ and $\theta_8 = \theta_4 + \pi/2$ in (4).

Performing a set of similar steps as for E^{+}, the energy associated with FC during negative half cycle is obtained as,

$$\begin{aligned}
E^{-} &= \int_{\pi}^{2\pi} V_{\mathrm{SCU}} \, I_{\mathrm{m}} \, \sin(\omega t - \phi) \\
&= I_{\mathrm{m}} \int_{\pi}^{2\pi} V_{\mathrm{SCU}} \, \sin(\omega t - \phi) \\
&= I_{\mathrm{m}} \times V_{\mathrm{dc}}/4 \left[\int_{\theta_9}^{\theta_{10}} \sin(\omega t - \phi) + \int_{\theta_{11}}^{\theta_{12}} \sin(\omega t - \phi) + \int_{\theta_{13}}^{\theta_{14}} \sin(\omega t - \phi) + \int_{\theta_{15}}^{\theta_{16}} \sin(\omega t - \phi) \right] \\
&= I_{\mathrm{m}} \times V_{\mathrm{dc}}/4 \, [\cos(\theta_9 - \phi) - \cos(\theta_{10} - \phi) + \cos(\theta_{11} - \phi) - \cos(\theta_{12} - \phi) \\
&\qquad + \sin(\theta_9 - \phi) - \sin(\theta_{10} - \phi) + \sin(\theta_{11} - \phi) - \sin(\theta_{12} - \phi)] \, . \qquad \text{(A.6)}
\end{aligned}$$

Owing to the symmetrical nature of the output voltage, it is evident that $\theta_9 =$

$\theta_1 + \pi$, $\theta_{10} = \theta_2 + \pi$, $\theta_{11} = \theta_3 + \pi$ and $\theta_{12} = \theta_4 + \pi$. Thus, the energy flowing into and from the FC is equal to the full cycle of fundamental voltage. In other words, it results in keeping the voltage across FC at desired level in all condition. This principle of energy balance stabilizes and regulates the voltage across FC naturally without any voltage and/or current sensor(s) thereby facilitate in the reduction of proposed inverter's overall design cost.

Appendix B

FORMULAS TO EVALUATE FAILURE RATES

The base failure rate ($\lambda_{\mathrm{B}}^{\mathrm{S}}$ and $\lambda_{\mathrm{B}}^{\mathrm{D}}$) are constants and equal to 0.012 and 0.064 respectively (Defense, 1991). The capacitor failure rate is computed as,

$$\lambda_{\mathrm{B}}^{\mathrm{C}} = 0.00254 \times \left[\left(\frac{S}{0.5}\right)^{3} + 1\right] \times \exp\left[5.09 \times \left(\frac{T_A + 273}{378}\right)^{5}\right], \tag{B.1}$$

where S is equal to the ratio of operating voltage to rated voltage. The temperature factor (π_{T}) in (5.8) is calculated as follows:

$$\pi_{\mathrm{T}}^{\mathrm{S}} = \exp\left(-1925 \times \left(\frac{1}{T_{\mathrm{J}} + 273} - \frac{1}{298}\right)\right), \tag{B.2}$$

$$\pi_{\mathrm{T}}^{\mathrm{D}} = \exp\left(-1925 \times \left(\frac{1}{T_{\mathrm{J}} + 273} - \frac{1}{293}\right)\right), \tag{B.3}$$

where T_{J} is the device junction temperature and is determined using

$$T_{\mathrm{J}} = T_{\mathrm{C}} + \theta_{\mathrm{JC}} \times P_{\mathrm{Loss}}, \tag{B.4}$$

where T_{C} is the heat sink temperature, θ_{JC} is the thermal impedance of the switch or diode, and P_{Loss} is the total power loss in the switch or diode. Further, the stress factor (π_{S}) and capacitance factor (π_{CV}) are calculated as follows:

$$\pi_{\mathrm{S}} = V_{\mathrm{S}}^{2.43}, \tag{B.5}$$

where, V_S is equal to the ratio of operating voltage to rated voltage and

$$\pi_{CV} = 0.34 \times C^{0.12}, \tag{B.6}$$

where C is the capacitance in microfarad. The values of quality factor (π_Q), environment factor (π_E), application factor (π_A), and construction factor (π_C) respectively are equal to 5.5, 6, 10 and 1 (Abdi et al., 2009).

Appendix C

DESCRIPTION OF EXPERIMENTAL PLATFORM

This chapter describes the experimental setup and software used to implement the developed control strategies and a detailed description of the laboratory prototype.

C.1 Overview of the experimental platform

The generalized block diagram representation of the developed low-power experimental prototype is shown in Figure C.1. The dSPACE 1104 board is employed which performs voltage, current sensing, and all the control computations programmed through Matlab/Simulink. The experimental setup comprises of the following main units:

- A PC for rapid-prototyping and real-time control
- A dSPACE 1104 board with inbuilt compiler to run the program developed, signal feedback, control signal generation and communicating with the PC
- Interface cards (Isolations, dead band circuit, etc.)
- Power circuit board (MOSFETs and gate drivers)
- The current sensors and voltage sensors
- The load box

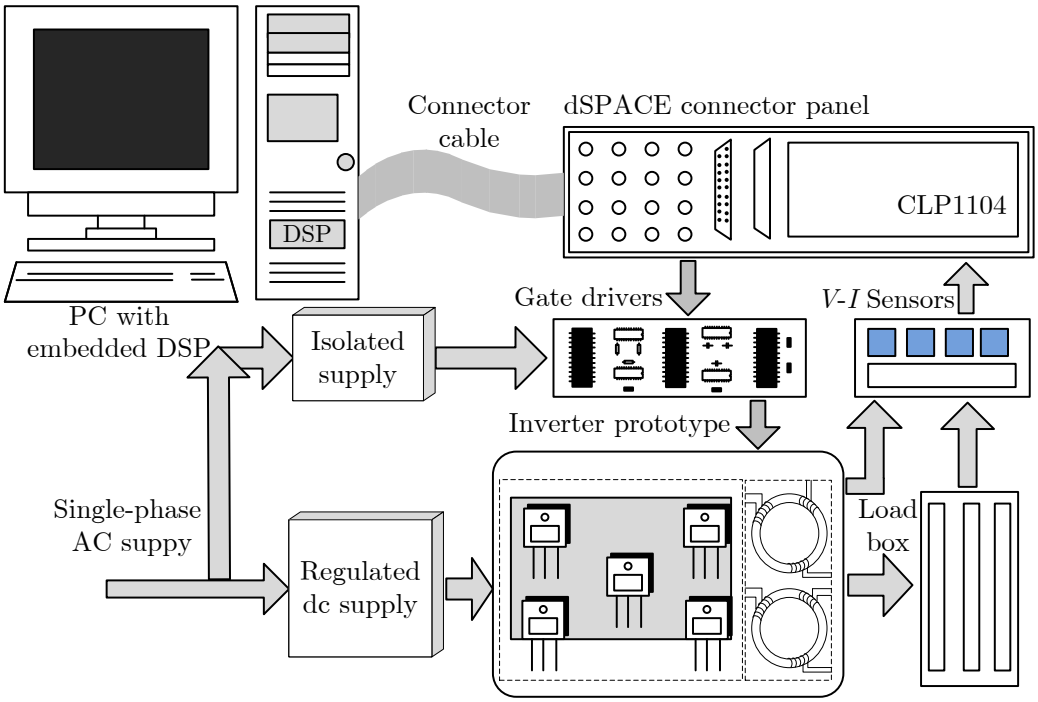


Figure C.1: Platform of the experimental setup

C.2 dSPACE DS1104 control board

dSPACE R&D controller is designed to enable a rapid prototyping and real-time simulation of various engineering applications. It provides a real-time interface for connecting the external devices to the processor inbuilt. It is a full-fledged control system based on a Motorola Power PC MPC8240 processor with PPC 603e core, 64-bit floating point processor, and on-chip peripherals clocked at 250 MHz. It also comprises of a slave DSP 16-bit fixed point processor from Texas Instruments TMS320F240 clocked at 20 MHz. The picture of the DS1104 controller and its additional I/O pins is shown in Figure C.2. The user has the flexibility to develop the desired model using Simulink which is further compiled for generating the appropriate C-code. The C-code so generated is dumped into the DSP controller. In addition to I/O pins, it consists of A/D and D/A converters for sensing the external feedback signals measured from the system under control. A graphical user interface termed Control Desk enables the user to implement/modify the reference values in real time while the system is in running condition. The following are the key specifications of the DS1104 control board:

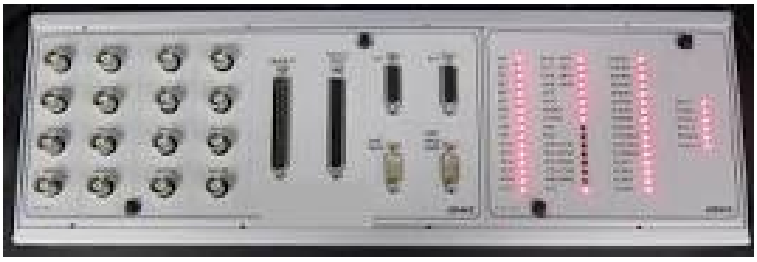


Figure C.2: The $19''$ racking system with DS1104 controller with digital I/O pins, analogue and control PWM cards

Processor

- MPC8240 with PPC 603e core and on-chip peropherals
- 64-bit floating-point processor
- CPU closk: 250 MHz
- 2 × 16 KB cache, on-chip

Memory

- 32 MB SDRAM
- 8 MB Flash Memory

Timers

- 4 General purpose-timers
- 1 time base counter

A/D converter

- 5 A/D converter channels (1 × 16-bit and 4 × 12-bit)
- Input voltage range: ±10 V
- Conversion time:2 μs for 16-bit; 800 ns for 12-bit

D/A converter

- 8 channels, 16-bit resolution
- Output range: ±10 V
- I_{max}: ±5 mA

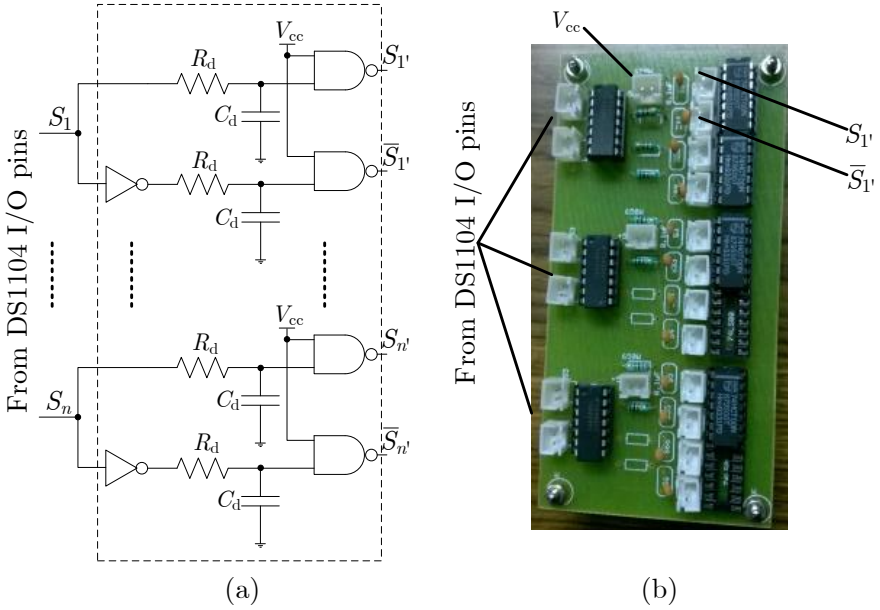


Figure C.3: (a) Schematic (b) PCB of the developed dead band circuit

Slave DSP

- TI TMS320F240, 16-bit fixed point processor
- CPU closk: 20 MHz
- I/O channels: 10 PWM outputs, 4 capture inputs, 1 serial peripheral interface

C.3 The pheripheral interface circuit board

Practically, the power switch exhibits a finite delay time during switching ON and OFF. Thus, it is essential to introduce a small dead time termed as dead band among the switching of power switches constituting a leg or the switches whose simultaneous switching ON leads to the shoot-through condition. The required dead band can be generated in many ways like an analog-based circuit, dedicated digital circuits or using the internal dead band modules of DSPs. In this work, a digital circuit with passive components based dead band generator is developed. The schematic and the printed circuit board (PCB) of the developed dead band circuitry is shown in Figure C.3(a) and Figure C.3(b) respectively. The minimum dead band required for the

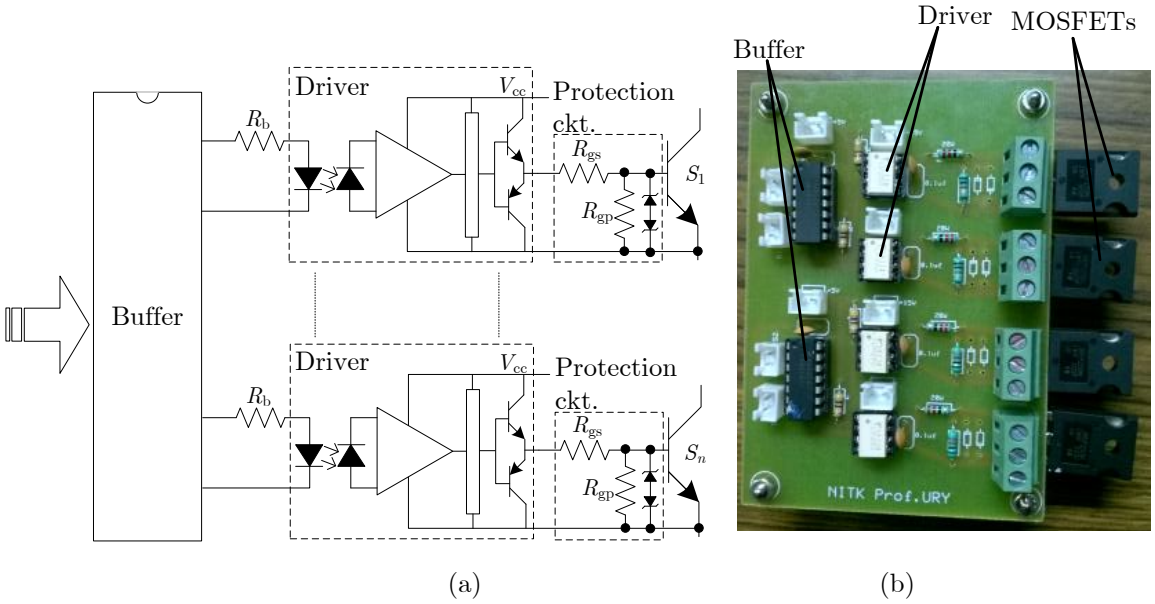


Figure C.4: (a) Schematic (b) PCB of the developed driver circuit and inverter power board

selected MOSFET (IRF250N) with a rating of 200 V and 20 A is given as (Xi, 2007)

$$t_{\mathrm{db,min}} = [(t_{\mathrm{d,off}} - t_{\mathrm{d,on}}) + (t_{\mathrm{pd,max}} - t_{\mathrm{pd,min}})] \times 1.2, \tag{C.1}$$

where, $t_{\mathrm{d,off}}$, and $t_{\mathrm{d,on}}$ respectively are the turn-off and turn-on delay time of the switch, $t_{\mathrm{pd,max}}$ and $t_{\mathrm{pd,min}}$ respectively are the maximum and minimum driver propogation delay. Referring to (Toshibha, 2007) and (Siliconix, 2011) the value of $t_{\mathrm{db,min}}$ is computed to be

$$t_{\mathrm{db,min}} = [(70 - 16) + (500 - 150)] \times 1.2 = 485\,\mathrm{ns}. \tag{C.2}$$

Further, the value of R_{d} and C_{d} is computed using (C.2) as $t_{\mathrm{db,min}} = R_{\mathrm{d}} \times C_{\mathrm{d}}$. Taking the nearest values as 100 Ω and 10 nF results in a dead band of 1 μs. The schematic and the printed circuit board (PCB) of the developed gate drive as well as power circuit is shown in Figure C.4(a) and Figure C.4(b) respectively. The value of the input resistance or buffer resistance (R_{b}) is computed using the forward current (I_{F}), input forward voltage (V_{F}) and "H" level pulse (V_{H}) as $R_{\mathrm{b}} = \frac{V_{\mathrm{F}} - V_{\mathrm{H}}}{I_{\mathrm{F}}} \approx 1$ kΩ.

Gate driver is an essential part of the power circuit that is responsible for providing

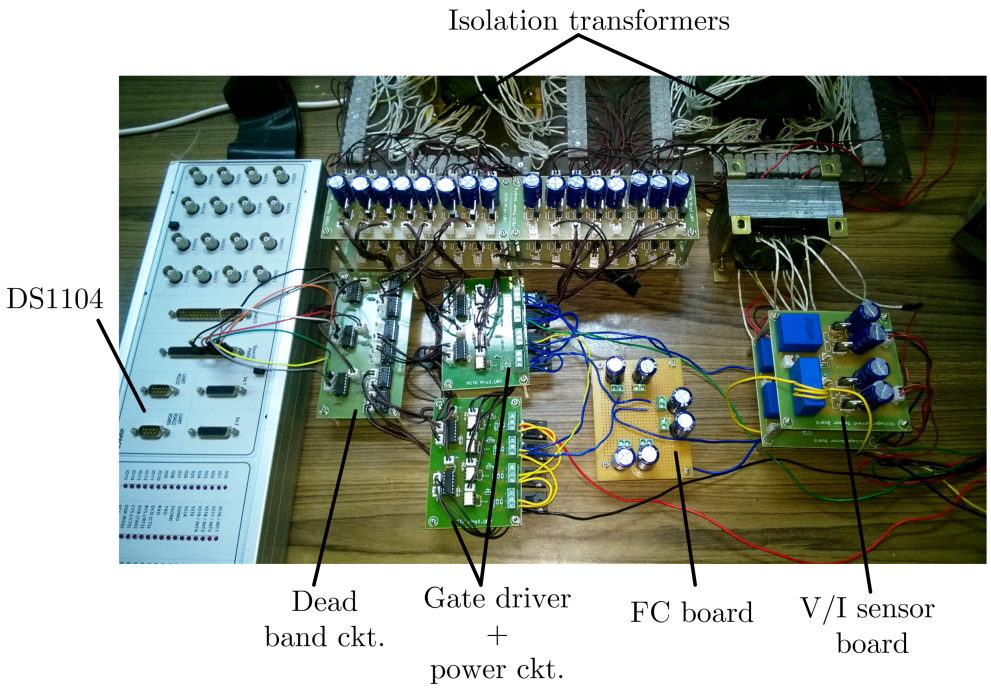


Figure C.5: Experimental setup

the required source and sinking current of the gate to source capacitance of the power switch. The value of R_{gs} is calculated so as to limit the maximum output current of the driver IC to a safe value i.e., 1.5 A for TLP250. Hence, the computed value of $R_{\text{gs}} = \frac{15}{1.5} = 10\,\Omega$. As evident from Figure C.3(b), each of the power circuit houses four MOSFETs placed at the bottom side of the board and associated gate drives. The rationale behind such a generalized board is to facilitate the realization of any MLI topology (motto of this work) smoothly with a minimum effort of only requiring to make suitable external connections using connecting wires.

The voltage sensors LV25p and current sensor LA55-p are employed for sening the FC voltages and load current. The procedure for design of the sensors is adopted from (Mishra et al., 2010). The overall hardware setup with other associated units is shown in Figure C.5.

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Bio-data

Name : Sandeep N
Date of birth: 11-04-1991
Marital status: Unmarried
E-mail: sandeep.n@ieee.org
Mobile: +91-8951879158

Education

- **M.Tech.**, Power Electronics & Drives, Visvesvaraya National Institute of Technology (VNIT), Nagpur, CGPA-9.03, 2014.
- **B.E.**, Electrical & Electronics Engineering, B. M. S. College of Engineering, Bengaluru, CGPA-9.33, 2012.
- **Diploma**, Electrical & Electronics Engineering, Sri Jayachamarajendra Government Polytechnic (SJP), Bengaluru, Aggregate-82.1%, 2009.

Address
Type-1 quarters
Foremen training institute
Outer ring road
Bangalore, Karnataka-575025, India.