

# Performance of cascode Class-EF<sup>-1</sup> PA with built-in techniques for UWB radar toward monitoring of patient actions

ISSN 1751-858X  
 Received on 5th June 2019  
 Revised 26th October 2019  
 Accepted on 7th November 2019  
 E-First on 31st January 2020  
 doi: 10.1049/iet-cds.2019.0241  
 www.ietdl.org

Rajesh Kumar<sup>1</sup>, Santanu Dwari<sup>1</sup>, Binod Kumar Kanaujia<sup>2</sup>, Sandeep Kumar<sup>3</sup> ✉, Hanjung Song<sup>4</sup>

<sup>1</sup>Department of Electronics Engineering, IIT, Dhanbad, India

<sup>2</sup>School of Computational and Integrative Sciences, JNU, New Delhi, India

<sup>3</sup>Department of E&C Engineering, National Institute of Technology Karnataka, Surathkal, Mangaluru, India

<sup>4</sup>Department of Nano Science and Engineering, Centre for Nano Manufacturing, Inje University, Gimhae 621-749, Republic of Korea

✉ E-mail: fedrer.engg@gmail.com

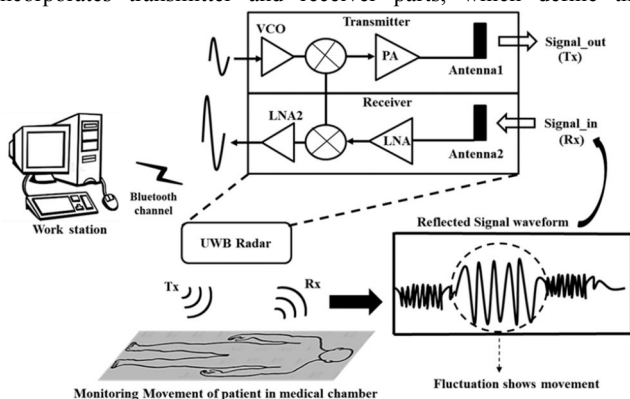
**Abstract:** This work proposes a performance of the cascode Class-EF<sup>-1</sup> power amplifier (PA) for UWB radar transmitter. The cascode Class-E PA with built-in techniques overcomes the traditional mismatch and provides good performance of PA. Incurs the resonance and switching effect is observed in cascode Class-E PA that compensates for the parasitic effects and provides a wide-impedance range. While design-II includes negative capacitance and inverse Class-F, which achieves a redundant performance of wide bandwidth and power-added efficiency (PAE). Design-II achieves the redundant performance compared with design-I. Both design-I and design-II are implemented and analysed through simulation and experimental results using RF 65 nm Samsung Magnachip Hynix CMOS process. Design-I achieves a wide-impedance bandwidth ranging from 3 to 11.7 GHz with drain efficiency (DE) and maximum PAE of 80 and 73% at the output power of 26.4 dBm. The global efficiency (GE) and error vector magnitude (EVM) of 70 and 5.2% are also achieving for design-I. The redundant performance in design-II achieves wide bandwidth with operating frequency range of 2–13 GHz with maximum DE and PAE of 85 and 76%. For design-II, GE and EVM are investigated as 68 and 4.9% that could validate the accuracy and robustness of the UWB radar.

## 1 Introduction

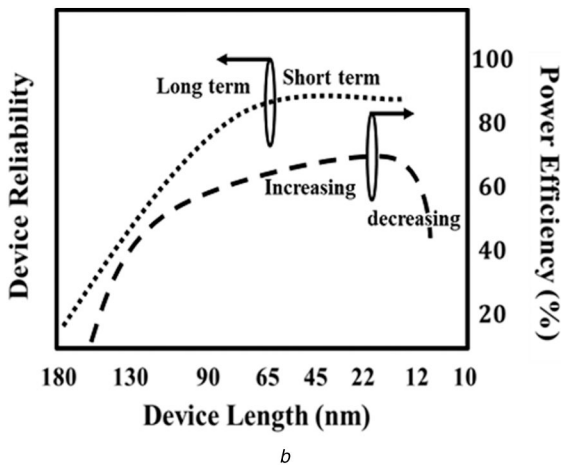
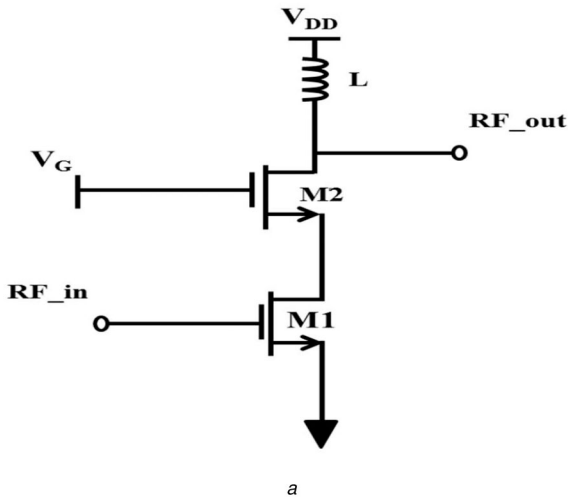
In medical applications, the radar system is demanding and very challenging for detection of the small organ movements with discontinuities inside the human body. However, such radar systems are optimised for various range of applications with developed topologies and radiating structures. Those range of applications included detection of the pathological conditions such as remote monitoring of vital signs, tumours etc. Remotely monitored physiologic functions in humans have been observed as the first time in the 1970s using medical radars, though development was limited due to bulky and expensive apparatus in those years [1, 2]. Afterwards, development of the inexpensive and compact radar system came due to advancement in device and technology, which was based on ultra-wideband (UWB) [3], continuous-wave [4] or frequency-modulated continuous-wave techniques [5, 6]. Fig. 1 shows conceptual pictorial view of the monitor of patient movement through UWB radar. The UWB radar incorporates transmitter and receiver parts, which define the

functioning of the UWB radar. In the extreme right of this figure, waveform indicates non-movement and movement of the patient in the room. The UWB radar emits signals toward the ceiling of the patient, therefore, that signal will then come in contact with the human body. The reflected signals will be fluctuating when the patient moves. The fluctuation of the signal represents the movement of the patient while non-fluctuation of the signal shows non-movement. These data could be recorded and analysed under the control centre of the surveillant. As per discussed concept in Fig. 1, UWB radar plays an important role in monitoring the movement of the patient. Although, various medical doctors and clinically facing the diagnosis problems to properly monitor the movement of the patient via UWB radar in recent years. Moreover, this is due to conventional transceiver integration technologies in the UWB radar.

The major challenges in the transmitter section of UWB radar toward monitoring the movement of patient need to take care of: (i) power consumption of devices should be low; therefore, it would be suitable for sensing in a longer time; (ii) signal bandwidth should be higher, therefore, signal properly reaches the patient; and (iii) it requires advancement in device and technology that enable UWB radar toward accuracy and robustness. The complementary metal–oxide–semiconductor (CMOS) advancement in recent years could offer solutions for improving the transmitter functioning of the UWB radar. The main component in the transmitter UWB radar is the power amplifier (PA) before the antenna. Still, various researchers investigated receiver architectures of UWB radar front-end with CMOS technology have been greatly improved challenges and issues in medical application. However, still, the main challenges lie in the transmitter section. The continuous and accurate monitoring of human movement is important in intensive care units, emergency rooms, home health care, paediatric clinics and rescue operations. We have considered here investigated performances of CMOS-based PA while they were not suitable for UWB radar in the monitoring of patient movement. In the past few years, mostly proposed Class-E PAs achieved maximum power efficiency lower than 40% at around 5 GHz [7–15], except in [10] where higher than 40% is achieved but output power is only 15.4



**Fig. 1** Typical block diagrams of UWB radar, which monitors the movement of the patient in the medical chamber. The monitoring movement of body using UWB radar has shown fluctuations in the waveform



**Fig. 2** Conventional cascode Class-E PA with its (a) Basic structure, (b) Design trade-off

dBm. These proposed PAs cannot be considered and suitable for UWB transmitter toward patient monitoring because of lower-power efficiency and of low-output power. A W-band-based Class-E PA using cascode topology, low upper base resistance and minimally overlapping current-voltage technique achieved peak power-added efficiency (PAE) and saturated output power is measured to be 40.4% and 17.7 dBm, respectively [16]. An inverse Class-F gallium nitride high electron mobility transistor (HEMT) PA was designed using novel parasitic-element compensation method and achieved maximum PAE of 70% at 1.8 GHz while cascode Class-E PAs achieved the best trade-off between reliability and power efficiency with 67% of PAE over the range of 1.4 GHz but they are not suitable for UWB radar because of lower bandwidth [17, 18]. Several papers have been reported [19–21], on inverse Class-F amplifier, which demonstrated many advantages, but they had not reported better explanation and experimental results of power efficiency; therefore, in practical point of view, they were useless. In [22], the recently investigated survey of UWB radar in medical applications, where the author considered various design blocks aspects and issues. In this work, cascode Class- $EF^{-1}$  PA with built-in techniques is proposed for UWB radar toward monitoring of patient movement. The proposed topology achieved enough bandwidth for sensing signal by UWB radar with maximum PAE of 75%. The highest power and drain efficiency (DE) of cascode Class- $EF^{-1}$  PA could provide better accuracy and robustness for UWB radar. This paper is organized as follows: Section 2 illustrates the cascode Class-E PA and Class- $EF^{-1}$  PA with incorporated techniques, whereas Section 3 discusses the measured results of Class- $EF^{-1}$  PA with redundant performance, and finally the conclusion is given in Section 4.

## 2 Cascode Class- $EF^{-1}$ PA

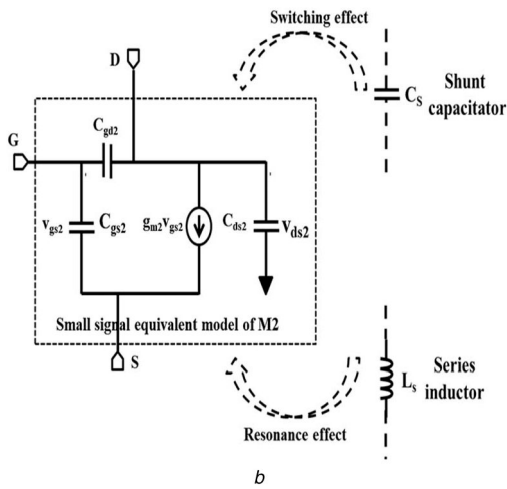
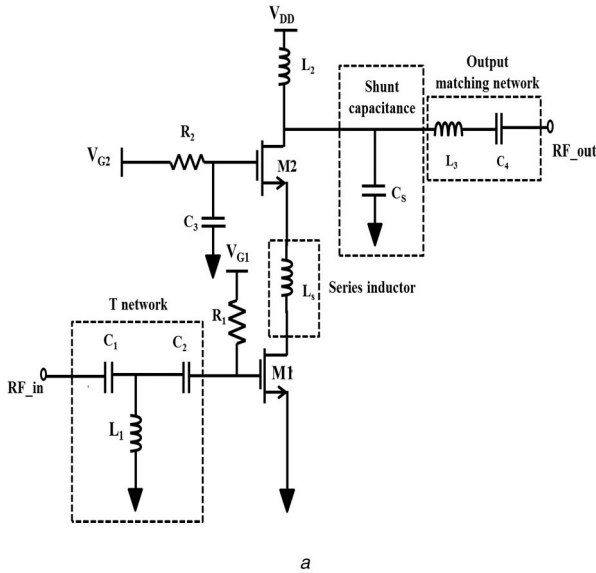
This section describes the design and consideration of cascode Class- $EF^{-1}$  PA with built-in techniques. The incorporation of the proposed integrated circuit design improves the performance of the UWB radar for patient monitoring in the medical applications. Section 2.1 illustrates the following proposed cascode Class-E PA with T-network, series inductor and shunt capacitor effect, whereas Section 2.2 elaborates the excess improved performance of cascode PA by replacing the shunt capacitance by inverse Class-F with negative capacitance.

### 2.1 Design-I with built-in techniques

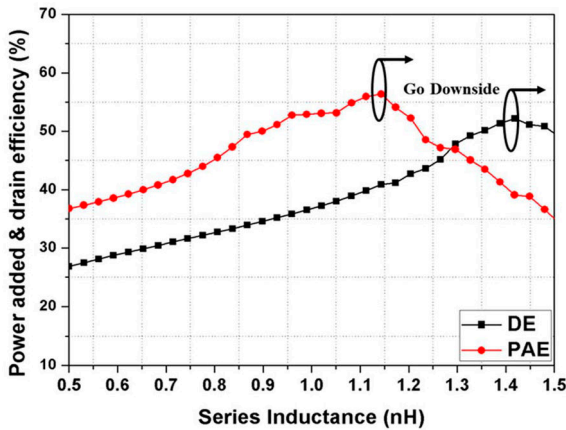
A cascode solution of Class-E PA with a CMOS process has been depicted in [18], where the best trade-off between the device reliability and power efficiency are achieved. However, over the couple of years of the decade, due to continuous scaling down of semiconductor device length to the nanometre regime has increased device stress and resulting in various power losses and mismatch the traditional trade-offs. Fig. 2a shows conventional cascode Class-E PA, where metal-oxide-semiconductor field-effect transistors (MOSFETs) M1 and M2 get shared peak drain-to-source voltage and reduced maximum oxide voltage drop while constant voltage is applied to the gate of M2. Moreover, Fig. 2b shows trade-off mismatch of conventional design between the device reliability and power efficiency with respect to device length. The conventional Class-E PA maintained long-term device reliability that degrades and became a short term with scaling down of the device length. Such kinds of devices stress impact directly on the power efficiency with increased dissipation, which has been showed as best the trade-off with reliability in the traditional design. Fig. 3a shows a proposed schematic representation with built-in techniques and improves the circuit stability and the accuracy of UWB radar toward patient movement in medical application. The proposed design incorporates T-network, single-ended cascode Class-E, series inductor, shunt capacitor and output-matching network. A T-network provides impedance tuner dynamic range for wideband Class-E operation, whereas series inductor and shunt capacitor provides resonance and switching effect for achieving high-power efficiency. Moreover, these effects suppress the undesired harmonics in the desired frequency of operation and obtain wide-impedance bandwidth. The design consideration of the proposed Class-E PA commences with T-network, where the impedance of inductor can be determined as a function of radio-frequency (RF) input frequency. The impedance tuner dynamic range provided by T-network can be determined by using the equation below:

$$Z_{\text{input}}(\omega) = \left( \left( \left( Z_{\text{PA}}(\omega) - \frac{j}{\omega C_2} \right)^{-1} - \frac{j}{\omega L_1} \right) - \frac{j}{\omega C_1} \right) \quad (1)$$

where  $Z_{\text{input}}(\omega)$  is the input impedance of T-network;  $Z_{\text{PA}}(\omega)$  is the input impedance of PA; and  $\omega$  is the frequency of operation. The values of inductor  $L_1$  and capacitances  $C_1$ ,  $C_2$  are chosen appropriately, therefore, network can provide dynamic tuner range to the Class-E operation and also reduce the possibility of power losses. As depicted in [18], the drain-to-source voltage gets shared between cascode devices; therefore, M2 has to be the considering main targeting component in the proposed topology. A series inductor  $L_s$  and shunt capacitance  $C_s$  are the important key factors, which reduce the effects of parasitic in the transistor and could improve the performance of cascode Class-E PA. A series inductor provides resonance mode while shunt capacitance gives switching effect on MOSFET M2 and both of suggested operations could be maintaining the best trade-off between the device reliability and power efficiency. The resonance mode is defined as ‘creation of flux lines around the bond wire (inductor), which opposes the vibration of parasitic’ while switching mode offers ‘creation of charging value for turn-on condition for M2’. When cascode PA is operated under Class-E operation, the switching mode of shunt capacitance keeps M2 turn-on condition until signal amplification. At the same time, parasitics of M2 dominant and influences on that

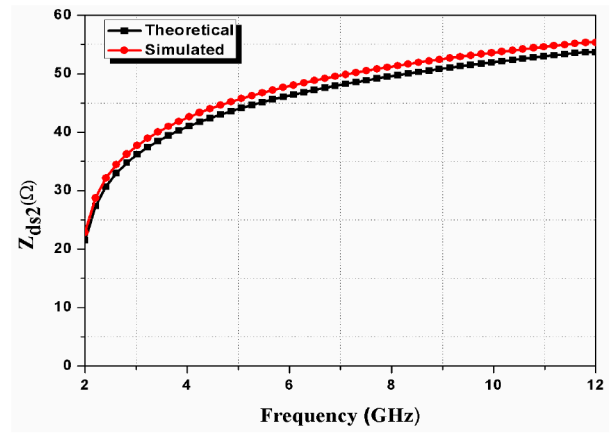


**Fig. 3** Proposed Class-E PA with its (a) Structure and consideration, (b) Small-signal model of MOS M2

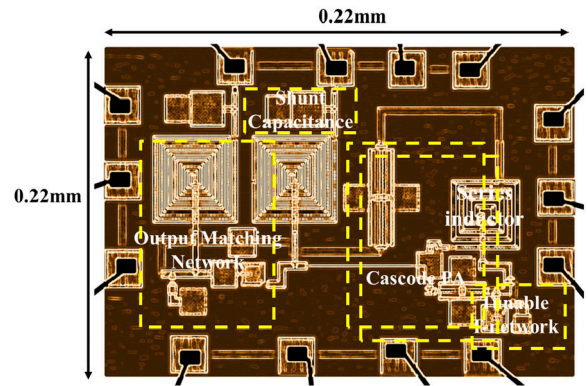


**Fig. 4** Simulated PAE and DE versus inductance

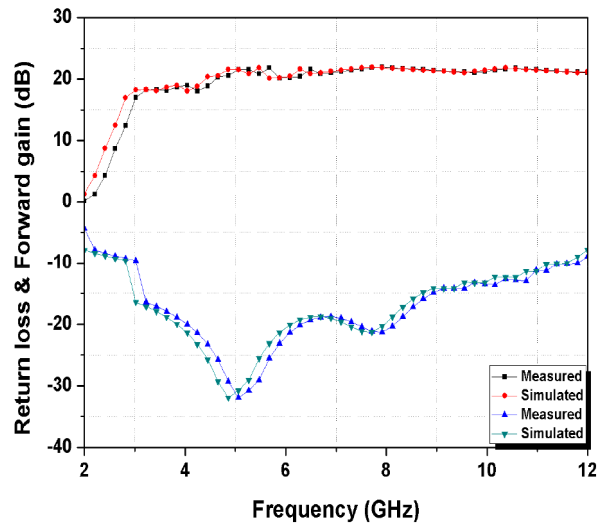
switching mode; hence, M2 goes on turn-off and that degrades the performance of PA. The initiation of switching mode is caused by a maximum voltage drop across M2 from the power supply. It is observed that to keep M2 in turn-on for long period duration, the series inductor is essential to the employee in-between M1 and M2 which is contributing the resonance effect and reduce the parasitics as well as the transconductance of M2 during the switching period. Therefore, the output impedance of M2 enhances due to reduced parasitics, and that impedance will resonate with the inductor-capacitor (LC) output-matching network and resulting in higher-power efficiency over the wider range of impedance bandwidth.



**Fig. 5** Theoretical and simulated output impedance versus frequency



**Fig. 6** Microchip photograph of design-I with built-in techniques



**Fig. 7** Return loss and forward gain versus frequency

The effects of series inductance on PAE and DE are also observed during the simulation, which is illustrated in Fig. 4. From this figure, it is found that after inductance value of 1.1 and 1.4 nH, the power efficiency and the DE goes downside because parasitic  $C_{gd2}$  of M2 shows more dominating behaviour due to large consideration of inductor values. Therefore, the value of series inductance is taken to be 1.15 nH to avoid more dominating parasitics. An equivalent small-signal model of MOSFET M2 with consideration of effects is shown in Fig. 3b. In the conventional design of cascode Class-E without series inductor and shunt capacitance, the parasitics  $C_{gd2}$ ,  $C_{gs2}$  and  $C_{ds2}$  of MOSFET M2 are effected due to shared drain-to-source voltage and that degrades the power efficiency when Class-E operated at the higher frequency. Therefore, series inductor and shunt capacitance are incorporated in-between M1 and output-matching network and they contributed

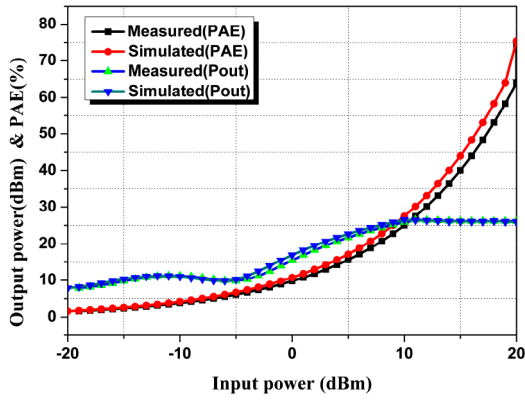


Fig. 8 Measured output power and PAE versus input power for design-I

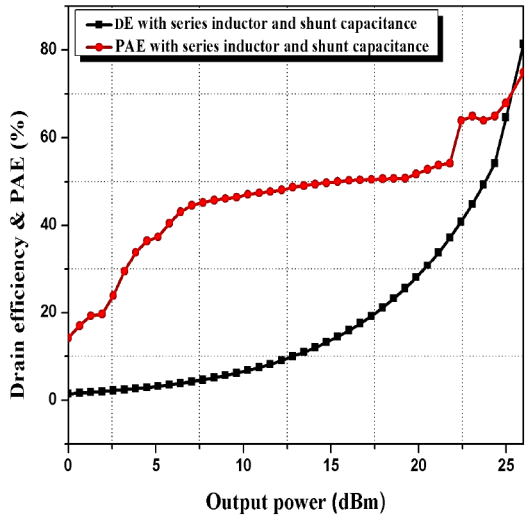


Fig. 9 Measured PAE and DE versus output power

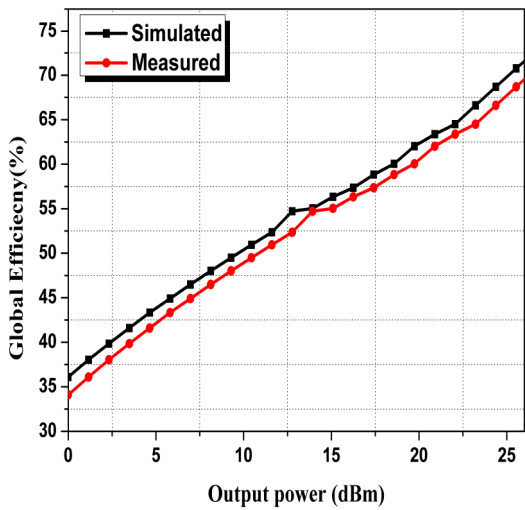


Fig. 10 Simulated and measured global efficiency versus output power

resonance and switching effect toward M2. These effects reduce the driving current of M2 caused by parasitic of M2 when they diminish their influences, and consequently, the output impedance  $Z_{ds2}$  of M2 is increased and try to settle down on  $(50 + j0) \Omega$  condition. The output impedance  $Z_{ds2}$  is calculated using small-signal equivalent model of M2 with consideration of  $L_s$  and  $C_s$  and that can be shown by using the equation below:

$$Z_{ds2} = \left( \frac{V_{ds2}}{(g_{m2} V_{ds2} + \lambda L_s C_s \omega_0 C_{ds2} V_{ds2} + j \lambda \omega_0 C_{gd2} V_{DD})} \right) \quad (2)$$

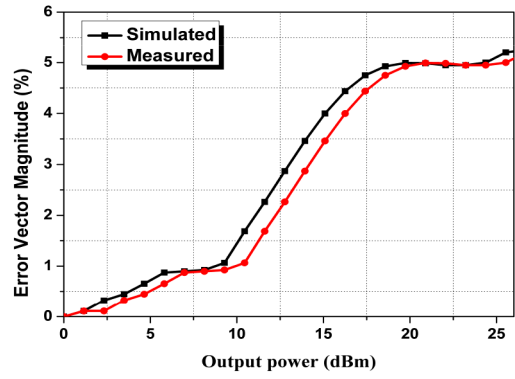


Fig. 11 EVM versus Output power (for design-I)

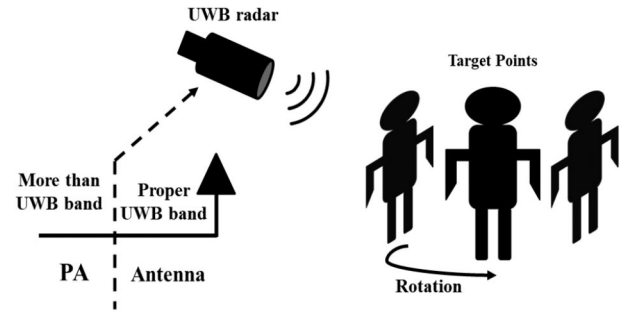


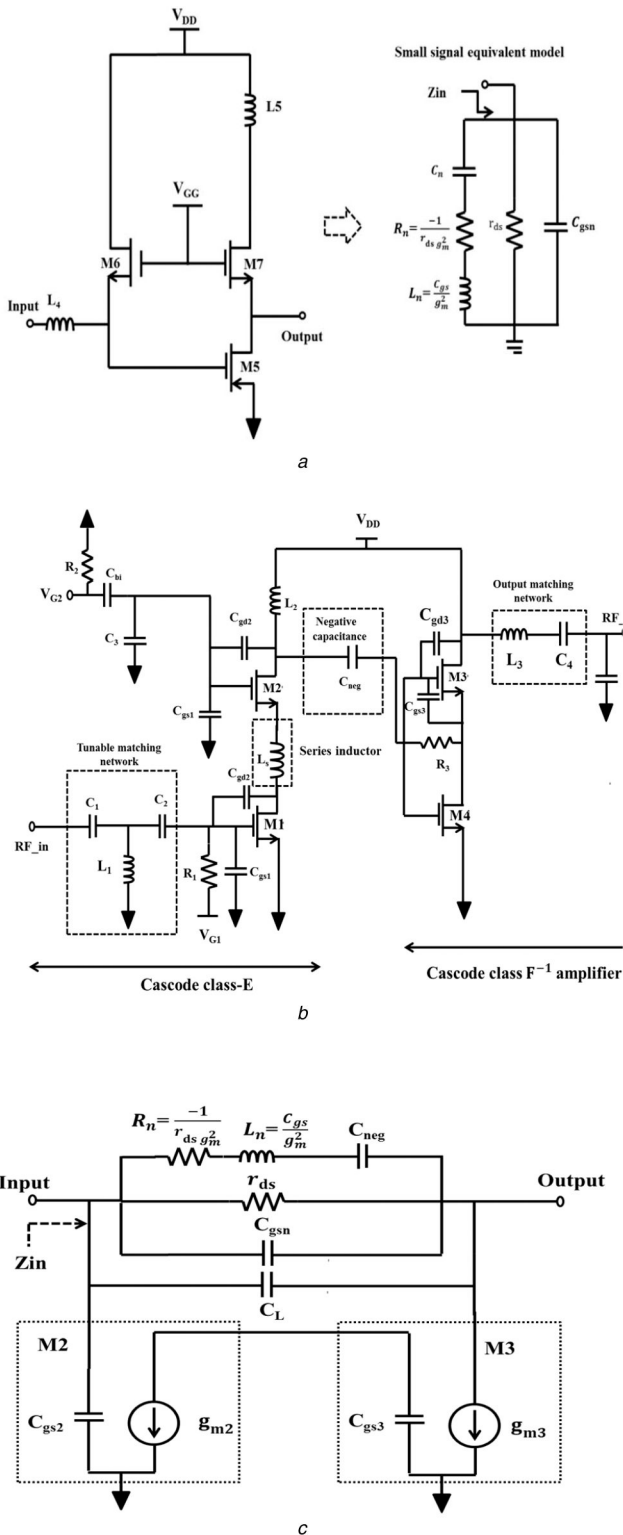
Fig. 12 Pictorial view of the interaction between the radar functioning and patient movement

Table 1 Component values of the proposed design-I with built-in techniques

Components	Values
M1	30/0.065 $\mu\text{m}$
M2	28/0.65 $\mu\text{m}$
R1	3 $\Omega$
R2	4 $\Omega$
C1	1.0 pF
C2	1.12 pF
C3	1.5 pF
C4	1.24 pF
Cs	1.01 pF
L1	1.0 nH
L2	1.5 nH
L3	1.95 nH
Ls	1.15 nH

Here,  $g_{m2}$  is the transconductance of M2;  $C_{ds2}$  is the drain-to-source capacitance,  $C_{gd2}$  is the gate-to-drain capacitance and  $V_{ds2}$  is the drain-to-source voltage across M2, respectively. The variation of output impedance concerning frequency can be seen in Fig. 5, where  $Z_{ds2}$  is settled down to  $(50 + j0) \Omega$  condition and ready to resonate with output-matching network. Owing to fine matching between  $Z_{ds2}$  and LC output-matching network, cascode Class-E with incorporated techniques can achieve the wide-impedance bandwidth of about 9 GHz. The proposed schematic representation of cascode Class-E with incorporate technique is analysed and implemented on the advanced design system (ADS) using RF simulator with Magna-chip Hynix a CMOS process.

A microchip photograph of the proposed design-I is realised in Fig. 6. The fabricated chip is characterised using three layers of the wafer with CMOS 65 nm Magna-chip Hynix process. For RF inductors and capacitances, metal-oxide-metal and metal-insulator-metal capacitance while spiral inductor microfabrication is employed. The die area is calculated as 0.22 mm<sup>2</sup> including all bonds and testing pads. The measured and simulated results of the proposed design include S-parameter analysis, where return loss achieves wide-impedance bandwidth of 9 GHz ranging from 3 to



**Fig. 13** Proposed design-II cascode Class-EF<sup>-1</sup> with its (a) Incorporate negative capacitance and equivalent model, (b) Fully integrated schematic diagram, (c) Small-signal models of M2 and M3 with negative capacitance

**Table 2** Comparison performance of design-I with others

Reference	$f$ , GHz	$P_{out}$ , dBm	DE, %	PAE, %	Gain, dB	global efficiency (GE), %	EVM, %	Technology, $\mu\text{m}$	Chip size, $\text{mm}^2$
[23]	1.8	31.5	51	54	26	N/A	10.8	0.13	1
[24]	1.95	26	58	43.6	26	N/A	N/A	0.18	1.60 × 0.52
[25]	2.45	20	50.7	43.6	N/A	N/A	N/A	0.18	1.4 × 1.6
[25]	5.3	21.6	47.7	42	11	N/A	18	0.18	0.47 × 0.561
this work	3–11.7	26.4	80.03	74.9	20.04	70.1	5.2	0.065	0.22 × 0.22

12 GHz with a fractional amount of 132%. The wide-impedance bandwidth is obtained due to suppression of even harmonics because of reduction in parasitic at the M2. The gain of the proposed design achieves good flatness from 3 to 12 GHz and which is more than 20 dB. Both simulated and measured results of return loss and forward gain made a good correlation with each other, which can be seen in Fig. 7. Although, measured and simulated plotting of the output power and the PAE are illustrated in Fig. 8, where a chip prototype delivers a maximum output power of 26.4 dBm under the supply voltage of 1.2 V. As expected, PAE is exponentially increased up to 74.9% at the input power of 20 dBm and this is due to added less power consumption from output LC network. Fig. 9 shows a measured PAE of 73% and DE of 80% at the maximum output power of 26.4 dBm. Fig. 10 shows the simulated and measured global efficiency versus output power at operation frequency.

Fig. 11 shows the simulated and measured error vector magnitude (EVM) of the fabricated design-I using ADS and N9030A PXA key sight technologies, respectively. The measured EVM of 5.2% and global efficiency of 70%. The experimental setup of the design-I and design-II would be considered in Section 3. The component values of the proposed design-I is shown in Table 1. The performances of design-I with other reported literatures are shown in Table 2.

## 2.2 Design-II with redundant performance

This section approaches design-II with redundant performance using negative capacitance and inverse Class-F techniques. This design-II aims to achieve redundant power efficiency and a wide band of operation for UWB radar, which targets the movement of the patient. Fig. 12 shows a clear pictorial view of transmitter section for UWB radar that targets the subject. It is mandatory to observe this figure for a better understanding of the interaction between the radar functioning and patient movement. By the way, design-I with built-in techniques achieved maximum PAE of 74% over the wide-impedance bandwidth of 3–11.7 GHz.

Although, it is found that power efficiency would degrade when the output of cascode PA is fed to the antenna of UWB radar, and this is due to the loading effect of the antenna. Therefore, we have to maintain power efficiency and wide-impedance bandwidth as per the requirement of UWB transmitting antenna in medical radar. In Fig. 12, the UWB medical radar is considered into two transmitter parts: part-I is the designed PA, which requires redundant frequency band than UWB due to loss of efficiency and bandwidth reduction. While part-II is antenna which requires at least UWB for proper monitoring of the patient. For this reason, design-I with negative capacitance and inverse Class-F technique is employed in design-II and achieve the redundant performance of cascode Class-EF<sup>-1</sup> PA. The redundant achievements of cascode Class-EF<sup>-1</sup> PA enable several features such as better accuracy, high-speed communication and bandwidth freedom for UWB radar toward patient monitoring. In the previous section, design-I achieved wide-impedance bandwidth and that is restricted up to 11.7 GHz. Moreover, this is due to fewer mismatch in impedance between shunt capacitance and output-matching network. Therefore, we replace shunt by negative capacitance network in design-II, which compensates parasitic of shunt itself and provides freedom in the existing wide band of operation. Fig. 13a shows a schematic diagram of negative capacitance with its small equivalent model. A negative capacitance is composed of three MOSFETs naming M5, M6 and M7 and its aspect ratios are (30/0.065), (30/0.065) and (28/0.065)  $\mu\text{m}$ , respectively. An

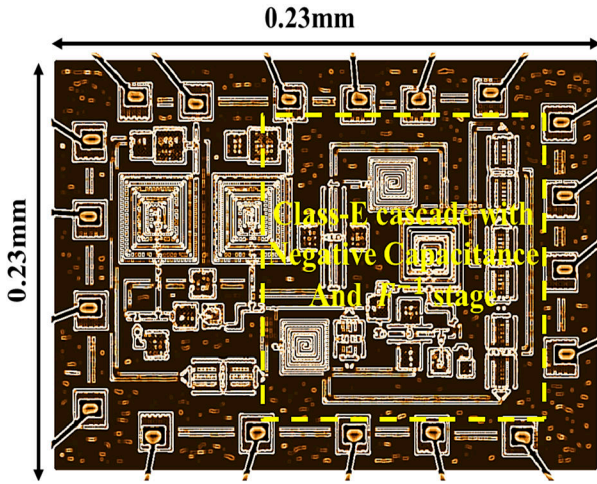


Fig. 14 Microchip photograph of design-II with negative capacitance and Class-F<sup>-1</sup>

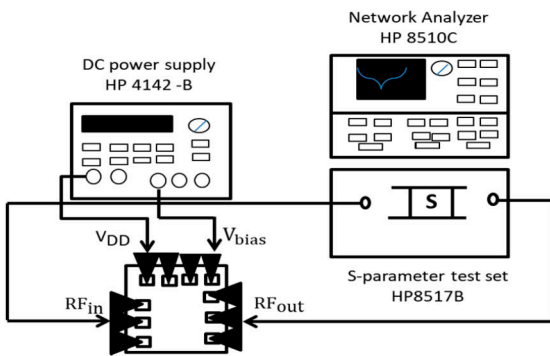


Fig. 15 S-parameter measurement setup 1 for both designs I and II

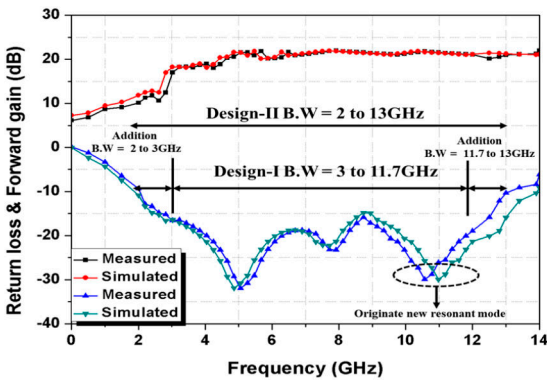


Fig. 16 Return loss and forward gain versus frequency for design-II

equivalent model network can be generated by using negative capacitance in the form of equivalent values of  $R$ ,  $L$  and  $C$ , respectively. To get freedom in wideband of operation, it is essential to provide tuning behaviour in negative capacitance ( $C_{\text{negative}}$ ) approach. From the equivalent model of  $C_{\text{negative}}$ , the input impedance can be calculated as (3). Two common-source transistors  $M5$  and  $M7$  are connected in a way that a positive feedback loop is created to convert the inductor load to a negative capacitor [26]. The generated negative capacitance using this topology is relatively linear in a wide-frequency band comparing with the negative capacitance effect due to positive feedback through in a common gate. For the simple derivation, the additional parasitic capacitances such as the intrinsic capacitances of the device are neglected. The intrinsic capacitances of the transistor in

the cascode Class-E stage and the Class-F<sup>-1</sup> stage are shown in Fig. 13b. The proposed design can be used to compensate for the undesired capacitive loading effect from that negative capacitance. Total input impedance of the circuit is then (see (3)). Here,  $C_{\text{gs}_{\text{total}}} = C_{\text{gs}_1} + C_{\text{gs}_2} + C_{\text{gs}_3} - C_{\text{gs}_n}$  and  $C_{\text{gd}_{\text{total}}} = C_{\text{gd}_1} + C_{\text{gd}_2} + C_{\text{gd}_3} - C_n$  are intrinsic capacitances that can be significantly reduced. Therefore, larger transistors can be used in the gain cells while the desired bandwidth is kept by choosing the proper value for negative capacitors, where while  $g_{m_{\text{total}}} = g_{m_1} + g_{m_2}$  is the total transconductance of cascode Class-E stage and the Class-F<sup>-1</sup>. Fig. 13c demonstrates the small-signal equivalent model of the transistors  $M2$  and  $M3$  with negative capacitance small-signal model of the proposed design-II and it is noting that bandwidth can be derived using calculating relation by

$$\omega = \frac{g_{m_{\text{total}}}}{2\pi \times (1 + (2C_{\text{gd}_{\text{total}}}/C_{\text{gs}_{\text{total}}})) \times C_{\text{gs}_{\text{total}}}}$$

Owing to this bandwidth dependency on the parasitic of  $C_{\text{negative}}$ , it approaches wideband of operation as compared with shunt capacitance employed in design-I. The  $C_{\text{negative}}$  of the proposed network can be evaluated by using the equation below:

$$C_{\text{negative}} = -2C_L \frac{g_{m_{\text{total}}}^2 - \omega^2 C_{\text{gs}_{\text{total}}} (C_{\text{gs}_{\text{total}}} + 2C_{\text{gd}_{\text{total}}})}{g_{m_{\text{total}}}^2 + \omega^2 (C_{\text{gs}_{\text{total}}} + 2C_{\text{gd}_{\text{total}}})^2} + 4C_{\text{gd}_{\text{total}}} \quad (4)$$

where  $C_{\text{gs}_{\text{total}}}$  and  $C_{\text{gd}_{\text{total}}}$  are parasitic capacitances of the whole design-II with incorporate networks, whereas  $C_L$  is the internal load capacitance because of internal circuit of negative capacitance. A  $C_{\text{negative}}$  has become a frequency-dependent parameter due to (4) and that provides tuning behaviour in the desired band of operation [26]. However, the  $C_{\text{negative}}$  further degrades the power efficiency caused by combinational effects of parasitic. Therefore, next stage is followed by cascode inverse Class-F mode [27]. The inverse Class-F mode operation has the ability to overcome the undesired harmonics and the fundamental load; thus, resulting in reducing the device stress and provide freedom in the power efficiency. The  $C_{\text{negative}}$  is connected between the output of cascode Class-E and input of cascode inverse Class-F amplifier which compensates the degradation of stability for design-II. The value of  $C_{\text{negative}}$  has been calculated to be small as 10 pF and observed that it is able to enhance PAE about to be 2%. In the next observation, when we followed cascode Class-F mode where the input signal is found to be changed by harmonic component produced from  $C_{\text{gs}_{\text{total}}}$ . Therefore, the cascode inverse Class-F PA is found to be a good candidate for maintaining current and input of non-linearity. The inverse Class-F PA offers a good efficiency when an infinite second harmonic impedance  $Z_{2L}$  and third harmonic impedance  $Z_{3L}$  at short circuit are kept. The open-circuit condition at load does not permit any non-linearity due to the input signal. So, the effect of second harmonics impedance would be diminished at the input. Therefore, harmonic manipulation is carried out at the load up to third harmonics only. Hence, the incorporation of negative capacitance and inverse Class-F mode with design-I obtained redundant performance in the design-II. The measured and simulation results of design-II would be discussed in Section 3.

### 3 Results and discussion

Fig. 14 depicts the microchip photograph of the fabricated cascode Class-EF<sup>-1</sup> PA. The similar fabrication process has been developed

$$Z_{\text{in}} = - \frac{j\omega(C_{\text{gs}_{\text{total}}} + 2C_{\text{gd}_{\text{total}}}) + g_{m_{\text{total}}}}{(g_{m_{\text{total}}} - j\omega C_{\text{gs}_{\text{total}}})2C_{\text{gd}_{\text{total}}} + 4j\omega C_{\text{gd}_{\text{total}}}(C_{\text{gs}_{\text{total}}} + 2C_{\text{gd}_{\text{total}}}) + g_{m_{\text{total}}}} \quad (3)$$

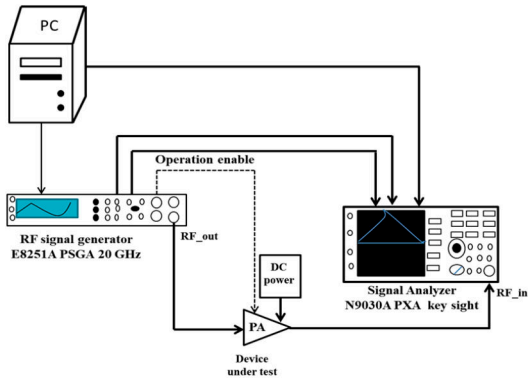


Fig. 17 EVM and power efficiency measurement setup 1 for both design-I and design-II

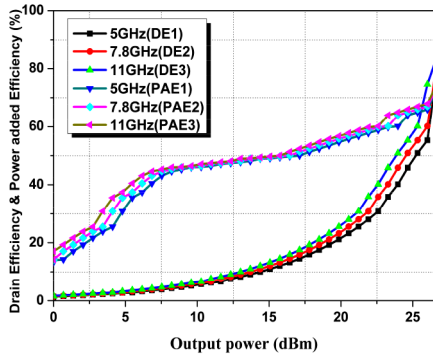


Fig. 18 Measured DE and PAE versus output power for design-II

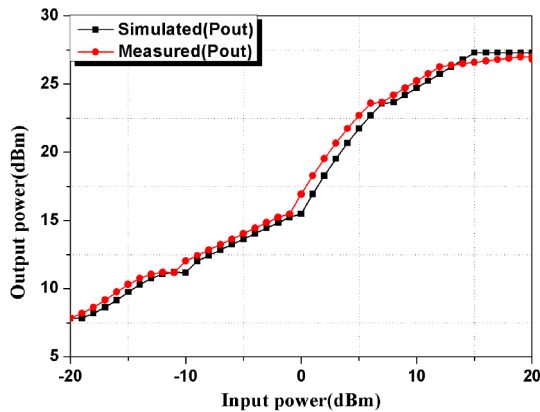


Fig. 19 Measured and simulated output power versus input power

for the design-II with incorporate circuits. The fabricated prototype has grown using three layers of the substrate technology. The chip area is calculated as  $0.23 \times 0.23 \text{ mm}^2$ , which is similar as die photograph of design-I and this is due to considering Murata spiral RF inductors and capacitors. All components are on-chip elements and fabricated using commercial 65 nm Samsung Magna-chip RF CMOS process. To remove the effect of package parasitic and spiral inductance, ground-signal-ground RF probes are landed on the input and output networks. Fig. 15 shows S-parameter experimental setup, where performance is examined using Agilent vector network analyser (HP 8510C). The return loss and forward gain are illustrated in Fig. 16, where an additional 1 GHz in the lower band and more than 1 GHz in the upper band are achieved with design-I impedance bandwidth. The negative capacitance creates new resonating mode at 11 GHz within the desired band of operation. The third resonant mode is basically to support the Class-F inverse to reduce undesired harmonics at the output. Owing to this, matching between negative capacitance with Class-F and output-matching network made a good correlation with each other at which results into wide-impedance bandwidth ranging from 2 to 13 GHz with 157% in fractional amount. The measured

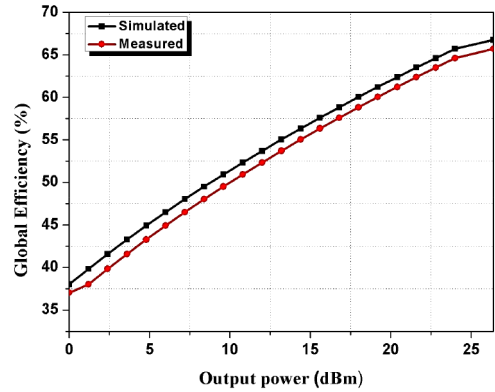


Fig. 20 Measured and simulated global efficiency versus output power

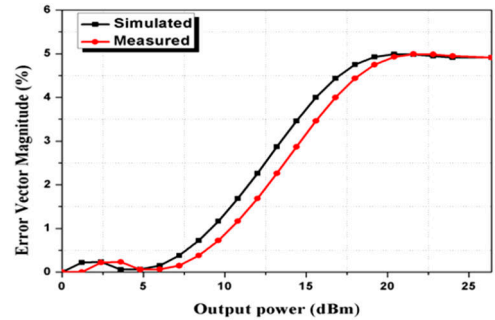


Fig. 21 EVM versus Output power (for design-II)

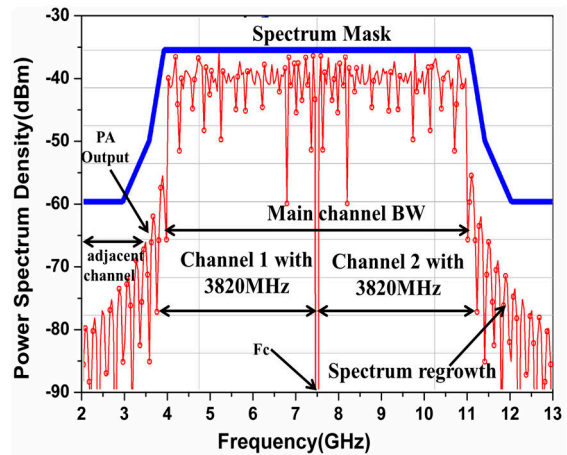


Fig. 22 Spectrum mask test at an output power of 26.4 dBm

and simulated gains around 24 dB is achieved with good flatness in the desired band of operation.

The next observation is to consider EVM and power efficiency experimental setup in Fig. 17, where performance is examined using the Agilent signal analyser (N9030A PXA key sight technologies). The measured DE and PAE with respect to output power are obtained at three resonating modes of 5, 7.8 and 11 GHz and can be seen in Fig. 18. At the output power of 26.4 dBm, the maximum PAE and DE of 75 and 85% are achieved, which is more than design-I performance. The output power versus input power curve is shown in Fig. 19. The Class- $EF^{-1}$  PA with cascode bias has achieved 26.4 dBm of maximum output power in simulation and 26.2 dBm of output power in measurement. It is observed that output power is linearly enhanced from 12.7 to 26.4 dBm for optimal load impedance of the proposed design-II. The output power of design-II is found to be more stable as compared with design-I by using incorporation of negative capacitance and inverse Class-F.

Additionally, simulated and measured global efficiency of 68% at the output power of 26.4 dBm is achieved and which is shown in Fig. 20. The practically global efficiency can be calculated using relation

**Table 3** Comparison performance of design-I with design-II

Proposed	$f$ , GHz	$P_{out}$ , dBm	DE, %	PAE, %	Gain, dB	Class of operation	bandwidth (BW), %	EVM, %	GE, %	Technology, $\mu\text{m}$	Chip area, $\text{mm}^2$	Column heading 2	Column heading 3	Column heading 4
design-I	3–11.7	26.4	80	73	20.04	Class-E	132	5.2	70	0.065	$0.22 \times 0.22$	123	123	123
design-II	2–13	26.4	85	75	24	Class-EF <sup>-1</sup>	157	4.91	68	0.065	$0.23 \times 0.23$	123	123	123

$$GF\% = \frac{P_{RF\_out}}{P_{PA\_DC} + P_{driver\_DC}}$$

where the combined power consumption of actual PA and driver circuit is considered. Moreover, the EVM is measured and simulated with respect to output power, which is shown in Fig. 21. The excellent performance of EVM could provide the best linearity and accuracy to the UWB radar for patient monitoring. A spectrum mast test of design-II is shown in Fig. 22. It is clear at the observation point that Class-EF<sup>-1</sup> PA is showing power spectrum density of around -38 dBm within range of channel 1 and channel 2. Moreover, the corresponding adjacent channel power ratio of ~35.3 dBc is achieved within main channel bandwidth. The comparative performances of both design-I and design-II are shown in Table 3.

## 4 Conclusion

In this paper, a novel performance of the cascode Class-EF<sup>-1</sup> with built-in techniques is presented for UWB radar in the purpose of monitoring patient movement in medical applications. The proposed architectures are included in the design-I and design-II with built-in techniques and achieve the best performance compared with traditional designs. The design-I with T-network, shunt capacitance, series inductor and cascode topology of Class-E PA provided the highest PAE and DE of 73 and 80% over wide-impedance bandwidth ranging from 3 to 11.7 GHz. While design-II with negative capacitance technique and inverse Class-F provided redundant performance. This achieves PAE and DE of 75 and 85% over wide-impedance bandwidth ranging from 2 to 13 GHz with three resonating modes of 5, 7.8 and 11 GHz. This novel performance of cascode Class-EF<sup>-1</sup> PA could be more suitable for that UWB radar which monitored the movement of patients in medical applications.

## 5 Acknowledgments

This work was supported by National Research Foundation of Korea, Grant/Award Number: NRF2019R1F1A1056937.

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