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Real-time implementation of transformerless dynamic voltage restorer based on T-type multilevel inverter with reduced switch count

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Summary

This paper presents T-type multilevel inverter topology-based dynamic voltage restorer (DVR) with reduced switch count. In medium voltage and high-power applications, two-level voltage source inverters are insufficient because of more voltage stress on switches, large dv/dt, size, and cost of the filter. To overcome these problems, multilevel inverter-based DVR is suitable, which can be directly connected to the medium voltage distribution system without injection transformer. In addition, the control of the DVR is implemented by abc to dq controller. The voltage compensation capability of the proposed DVR is enhanced by employing the in-phase compensation technique with reduced carrier pulse width modulation scheme, and also the total harmonic distortion(THD) in the load voltage is reduced. The design and analysis of the proposed system are discussed, and its performance is validated in MATLAB/Simulink and in the OPAL-RT real time processor.

KEYWORDS

dynamic voltage restorer, reduced carrier PWM scheme, T-type multilevel inverter, voltage sag and swell

1 | INTRODUCTION

In present days, power quality (PQ) is being worsened because of an increase of sensitive loads in industry, domestic, and commercial applications, ie, at the end users. So it is important to analyze the electrical power at the end users. There are other natural causes for PQ problems such as flashover, electronic equipment failure, and lighting. In general, PQ problems are voltage sag and swell, flicker, harmonics, and notches.[1,2] Among these PQ problems, voltage related disturbances such as voltage swell and voltage sag are very severe. Causes of voltage sag are faults on the distribution

List of Symbols and Abbreviations: %, percentage; AC, Alternating current; BNC, Bayonet neill concelman; CHB, cascaded H-bridge; CPD, custom power devices; CSI, current source inverter; DC, Direct current; D-STATCOM, distribution static compensator; dv/dt, change in voltage with respect to time; DVR, Dynamic Voltage restorer; FC, flying capacitor; FPGA, field programmable gate array; HIL, hardware in the loop; I/O, input and output; IGBT, Insulated gate bi-polar transistor; LPF, low-pass filter; LSPWM-POD, line shift pulse width modulation-phase opposition dissposition; LV, low voltage; MLI, multilevel inverter; MV, medium voltage; MVA, mega-volt ampere; NPC, neutral point clamped; p.u, per unit; PC, peripheral components; PCC, Point of common coupling; pf, power factor; PLL, phased lock loop; PQ, power quality; PSPWM, Phase shift pulse width modulation; PWM, pulse width modulation; RCP, rapid control prototyping; RCPWM, reduced carrier pulse width modulation; RMS, root mean square; RSC, reduced switch count; RT, real time; SSC, static series compensator; THD, total harmonic distortion; UPQC, unified power quality conditioner; VSI, voltage source inverter; ϕ, phase.

network, start or stop of large loads, badly regulated transformers, and capacitor switching. According to the IEEE 1159 and IEEE 1346 standard,[3] the definition of voltage sag is a reduction in the source voltage from 10% to 90% of the source voltage for a duration of 1/2 cycles to less than 1 minute.[4,5] According to IEEE 1159 standard, the voltage swell is an increase in RMS voltage from 1.1 to 1.8 p.u of nominal voltage for a time period of 1/2 cycles to less than 1 minute. To prevent PQ problems on sensitive loads, different new power electronic devices are available. The most effective and feasible power electronics devices are custom power devices (CPD).[6,7] They can be either connected in series or parallel or series-parallel. The series compensating devices are static series compensator (SSC) and dynamic voltage restorer (DVR), the parallel compensating device is distribution static compensator (D-STATCOM), and the series-parallel compensator is UPQC. In general, DVR is used for voltage related PQ issues, D-STATCOM is used for current-related PQ issues, and UPQC is for both voltage- and current-related issues. This paper is focused on the performance of the DVR to diminish the PQ problems of voltage swell and sag in a distribution network. DVR is a power electronic device, which is connected in series between source and load. It regulates load voltage by controlling the real and reactive power between the DVR and power distribution network.[8,9] The rating of the DVR is based on factors such as a current rating of the distribution line, load power factor, and maximum voltage injection.

The DVR can be located either at low voltage (LV) or medium voltage distribution (MV) level as shown in Figure 1. The MV DVR system integrates numerous sensitive loads in a grid, and thereby, it reduces the cost per MVA.[10] Decentralized compensation by LV DVR targets only critical loads. The LV DVR injects the negative, positive, and zero sequence voltages, whereas MV DVR compensates only negative and positive voltages.

Based on the type of supply, DVR topologies are divided into three phases and single phase. Each categorization of these DVR topologies is further divided based on converter topologies[11] as shown in Figure 2. The AC-AC converters[12,13] are used in DVR system for mitigation of the PQ problems without direct current (dc) link capacitor. The advantage of the AC-AC converter-based DVR is that it eliminates the DC capacitor and energy storage elements. Thus, there is a possible reduction in weight, volume, and cost of the system. However, these converters draw more current from the grid during voltage sag conditions, and hence, they are not feasible for deep voltage sag compensation in weak electrical grids.[14] The *z*-source converters compensate the deep voltage sag with lower dc-link voltage, but it requires more passive elements, and there is a shoot through problem in it.[15]

In the three-phase DVR, the commonly used converter topologies are full-bridge, four-leg, six-switch two-level, and six-switch split capacitor inverter.[16] In general, two-level voltage source inverter-based DVRs are used in medium or high voltage applications. These switches have to block large voltage when it is used for medium or high voltage distribution network. Large dv/dt causes electromagnetic interference. In addition to that to avoid these problems, multilevel inverters (MLIs) are used. The commonly used MLI topologies are flying capacitor (FC) and diode-clamped and cascaded H-bridge (CHB) MLIs. Each topology has certain drawbacks. For instance, in diode-clamped MLI topologies, balancing the capacitor voltages is difficult as the voltage level increases.[17] FC MLIs require more dc capacitors with increasing the number of voltage levels,[18] whereas in CHB, MLI requires more isolated DC sources, and the number of switches increases as the number of voltage level increases.[19,20] The number of switches required in diode-clamped, FC, and CHB MLI for n-level voltages is $N_{sw} = 2(n - 1)$. In all three topologies, the number of switches required for a

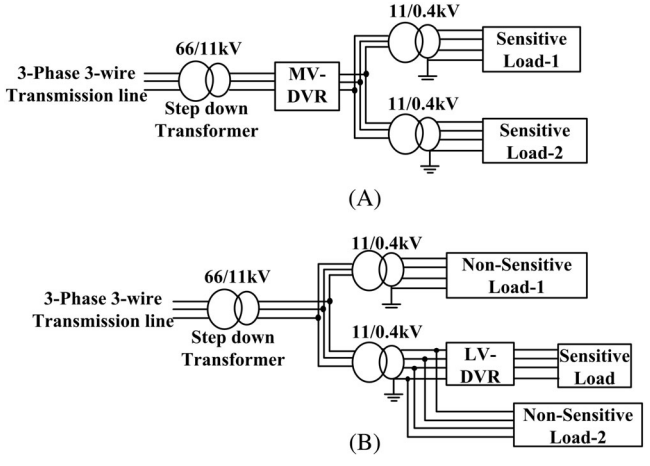

FIGURE 1 Dynamic voltage restorer (DVR) located in (A) medium voltage distribution and (B) low voltage distribution system

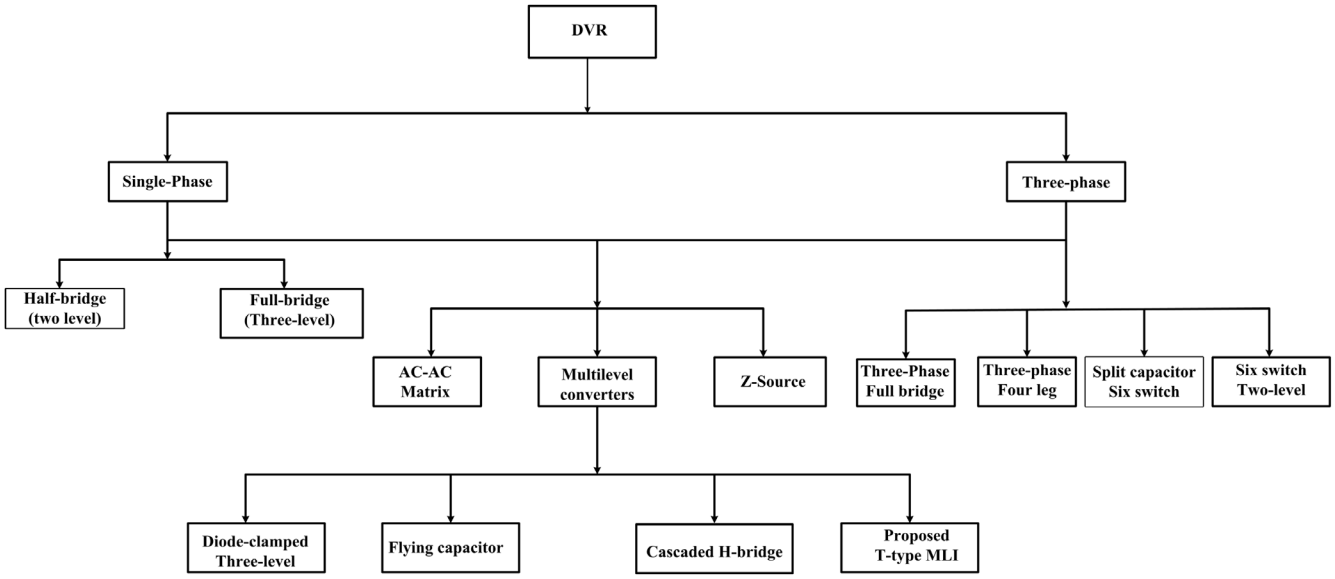

FIGURE 2 Classification of dynamic voltage restorer (DVR) topologies based on inverter structures

TABLE 1 Comparison between the inverter topologies in dynamic voltage restorer (DVR) structure

Sl.No	Inverter	Advantages	Disadvantages
1	1-ϕ Half bridge inverter[22]	Less cost and less switch count	Harmonic content is high in the output voltage
2	1-ϕ Full bridge inverter[23]	Used in a high voltage distribution system	Presence of harmonic content is high
3	3-ϕ full-bridge inverter[24]	Simple control and less cost	Large dv/dt and Presence of electromagnetic interference
4	3-ϕ six-switch inverter[25]	Less power semiconductor devices, simple topology	unable to compensate unbalanced voltages
5	3-ϕ split-capacitor six-switch four wire inverter[26]	Able to compensate unbalanced voltages	input/output voltage ratio issues related to the capacitor voltage balancing
6	3-ϕ four leg inverter[27]	No dc-link capacitor balancing problem	Required two extra switches
7	AC-AC converter[28]	Elimination of energy storage elements and DC-link capacitor	not feasible for deep voltage sag condition in the week grid
8	Z-source inverter[29]	Ability to inject Deep voltage sag with lower dc-link voltage	It requires more LC elements and shoot through problem
9	Diode-clamped MLI[30]	Multilevel output and industrial approved	The requirement of clamping diodes are high for high-level inverters
10	Flying-capacitor MLI[31]	Can be used for any number of levels	An excessive number of storage capacitors are required for more than three level
11	Cascaded H-bridge inverter[32]	Used in medium voltage and high power applications	The number of switching devices increases, complex control structure and requires isolated dc supplies
12	Proposed T-type MLI	Isolated dc supplies are not required and reduced number of switching devices	Requires high power rating switches

certain voltage level is high, which, in turn, increases the number of gate drivers, cost, and size. In order to avoid these problems, a reduced switch count (RSC) MLI topology is required for the DVR system in MV and high-power applications.[21] Table 1 shows the comparison between the inverters used in the DVR structure.

In this paper, a real-time implementation of transformerless DVR using RSC T-type MLI topology is proposed. Transformerless DVR leads to elimination of the injection transformer, and as a result size, weight and cost of DVR will be reduced. Transformerless DVR performs the work without compromising efficiency and reliability. The proposed three-phase DVR is implemented by abc to dq control technique. Simulation results of proposed T-type topology are carried out in MATLAB/Simulation software and compared with results taken from OPAL-RT, OP4510, and real-time prototype setup.

This paper contains six sections, wherein Section 2 presents the working principle and operation of T-type MLI, Section 3 presents DVR control and reduced carrier pulse width modulation (PWM) technique, Section 4 presents simulation results and discussion, Section 5 presents real-time results and discussion, and Section 6 presents conclusion.

2 | WORKING PRINCIPLE AND OPERATION OF PROPOSED SYSTEM

2.1 | Proposed five-level T-type topology configuration

The proposed T-type MLI is one of the RSC topologies. The T-type inverter contains four unidirectional switches and one bidirectional switch. The bidirectional switch is shown inside the dotted square box in Figure 3. The bidirectional switch blocks both positive and negative polarity voltages, in addition to the bidirectional current flow through it.[33] The midpoint dc voltage source is connected to any one of the poles of the H-bridge network across the bidirectional switch. The necessity of bidirectional switches and dc voltage sources is increased as the voltage level increase, but the full bridge or H-bridge remains unchanged. The proposed MLI contains combinations of bidirectional and unidirectional switches. The number of switches needs to be in each phase for this topology is $(n - 3) + 4$, where $(n - 3)$ indicates the additional unidirectional switches and 4 indicates the number of switches in full-bridge or H-bridge network. The three-phase connection of T-type multilevelinverter DVR is shown in Figure 3.

2.1.1 | Advantages of T-type MLI topology

- The proposed topology reduces the switch count by 37.5% compared with other topologies,[34]
- Requires just 60% of diodes required in a diode-clamped MLI,[34]
- Output and input currents are sinusoidal with less harmonic content,
- Less cost, weight, and size compared with conventional topologies,
- Switching redundancy is reduced compared with other conventional topologies,
- It does not require isolated dc sources.

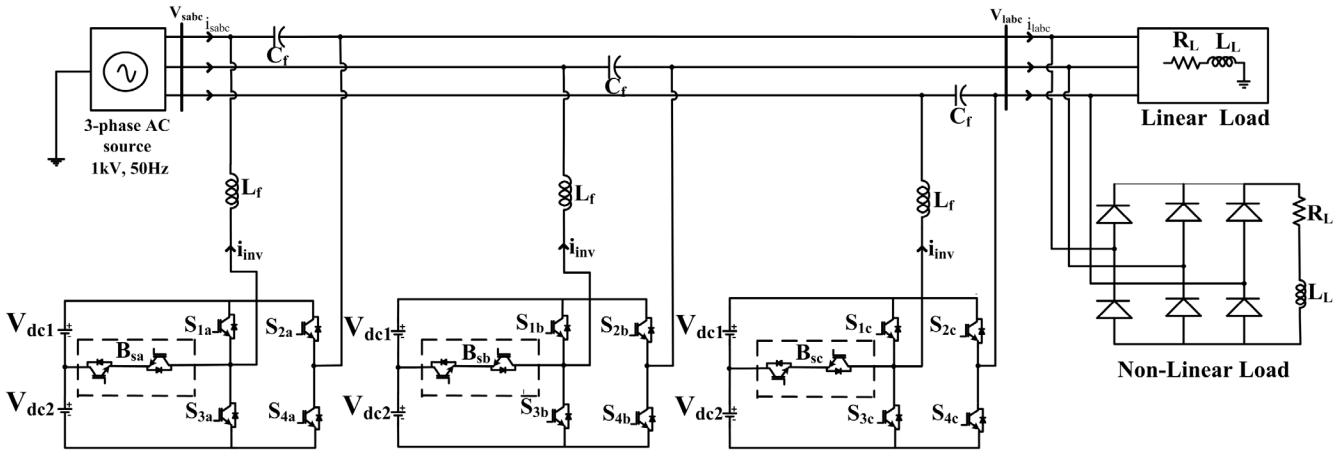

FIGURE 3 Proposed five-level T-type topology dynamic voltage restorer (DVR)

2.2 | Switching configuration of five-level proposed inverter

Five-level T-type MLI requires midpoint dc source to obtain five levels per phase, ie, 2 V, V, 0, −V, and −2 V. Switching states of the proposed T-type MLI for different voltage levels are shown in Table 2. State "1" represent ON, and "0" represent OFF of the corresponding switch. The five-level output voltage of T-type topology can be produced by considering the two voltage sources with equal magnitude, ie, $V_{dc1} = V_{dc2} = V_{dc}$. The comparison of proposed T-type MLI with well-known conventional topologies is summarized in Table 3. The proposed T-type topology has less switching losses compared with other conventional MLI topologies, and approximate losses are shown in Figure 4. Here for a 100-kW system, the power losses are calculated for the IGBTFD300R06KE3 with the help of Equations (1) and (2).[35] Figure 5 shows the current direction and conduction of switches for each switching state. It is to be noted that only two switches are switched on to generate the output voltage. Power losses are mainly two types during the operation of power semiconductor switching devices. These are switching losses (P_{sw}) and conduction losses (P_c). Conduction losses occur while the power semiconductor switches are carrying current during on state and conduction current.[36] As the number of switching devices increases, the conduction losses increases proportionally[37]; the conduction losses are calculated from Equation (1):

TABLE 2 Switching scheme of T-type multilevel inverter

Sl.No	S_1	S_2	S_3	S_4	B_s	V_0
1	1	0	0	1	0	2 V
2	0	0	0	1	1	V
3	1	1	0	0	0	0
4	0	0	1	1	0	0
5	0	1	0	0	1	-V
6	0	1	1	0	0	-2 V

TABLE 3 Comparison of proposed T-type MLI with conventional MLI topologies

Sl.No	Multilevel inverter	Diode-Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed T-type
1	Main switches	8	8	8	6
2	Flying capacitors	0	6	0	0
3	Diodes	6	0	0	0
4	DC Source	1	1	2	2
4	DC Bus capacitors	4	4	2	0

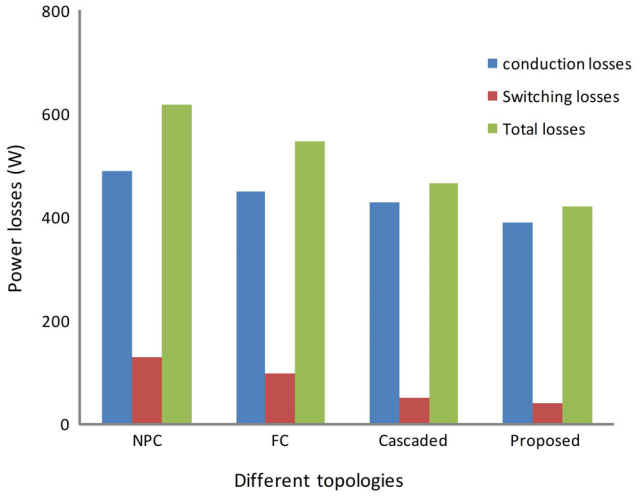

FIGURE 4 Comparison of power losses between conventional and proposed T-type multilevel inverter (MLI)

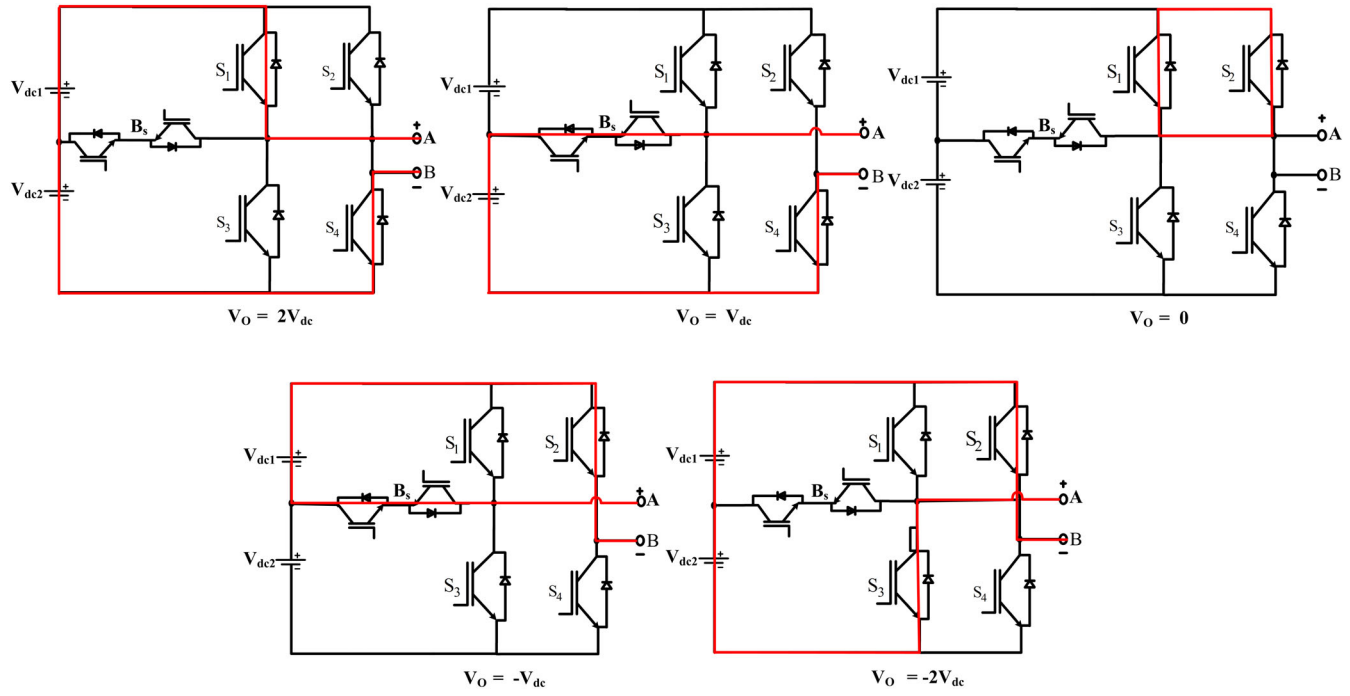

FIGURE 5 Switching states of proposed T-type topology for corresponding phase voltages

$$P_c = u_{ceo} * I_{av} + r_c * I_{rms}^2, \tag{1}$$

where P_c is conduction losses of the switches, u_{ceo} is collector-emitter voltage of on state zero current, I_{av} is average current, I_{rms} is RMS current of the switch, and r_c is collector emitter resistance. Switching losses occur during turn-on and turn-off of the power semiconductor switching devices. These losses are on both the switch and antiparallel diode.[38] Switching losses are proportional to the carrier frequency f_c. Switching losses (P_{sw}) are calculated from Equation (2):

$$P_{sw} = \frac{E_{dc}}{n-1}\left(e_{on} + e_{off}\right) * f_c * \frac{1}{2pi}\int_a^b i_{out} d\theta, \tag{2}$$

where P_{sw} is switching losses, e_{on} is turn-on energy per switching, and e_{off} is turn-off energy per switching. e_{on} and e_{off} values are obtained from datasheet of the switch, E_{dc} is the input voltage, f_c is carrier frequency, "a" and "b" are the phase angles while current is passed, and "n" is phase voltage level.

3 | DVR CONTROLLER AND PWM TECHNIQUE

3.1 | DVR controller using abc to dq rotating frame

Two controllers are well-known in a linear control system, open loop (feedforward), and closed loop (feedback).[39] Feedforward controller is faster than feedback controller for the required voltage compensation. The feedback controllers are best in minimizing the steady-state error.[40]

Block diagram of abc to dq control technique is shown in Figure 6 in which the measured three-phase grid voltages are transformed from abc to dq rotating frame using abc/dq transform with support of PLL. The reference value of DVR in dq frame is obtained by subtracting grid voltage $V_{G,\,d}$ and $V_{G,\,q}$ from their respective reference values. These reference values generated based on in-phase compensation technique. The obtained DVR reference voltages transformed back to abc components using dq/abc transformation.[41] The reference voltages can be considered as reference signals for PWM modulation.

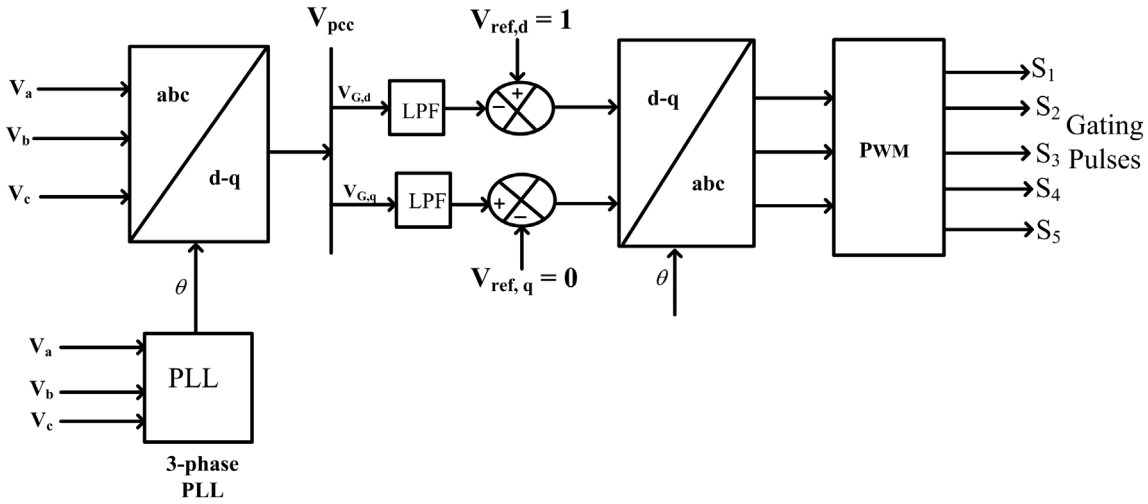

FIGURE 6 abc to dq control technique for three-phase dynamic voltage restorer (DVR)

3.2 | Mathematical analysis of abc-dq rotating frame

In d-q transformation, the 3-ϕ system is transformed to the 2-ϕ stationary reference frame, and then these variables stationary frame to a rotary reference frame with an angular velocity of "ω". Deduce the dq0 components from abc signals by performing an abc to dq0 transformation in a rotating reference frame by using Equation (3).

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & cos\left(\theta-\frac{2pi}{3}\right) & cos\left(\theta+\frac{2pi}{3}\right) \\ -sin\theta & -sin\left(\theta-\frac{2pi}{3}\right) & -sin\left(\theta+\frac{2pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}. \tag{3}$$

The reference voltages of the DVR in the dq0 frame can be expressed in (4) and (5).

$$V^*_{Dd} = V^*_d - V_d. \tag{4}$$

$$V^*_{Dq} = V^*_q - V_q. \tag{5}$$

DVR reference voltages are obtained by using inverse parks transformation from Equation (6).

$$\begin{bmatrix} V^*_{dvra} \\ V^*_{dvrb} \\ V^*_{dvrc} \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta & 1 \\ cos\left(\theta-\frac{2pi}{3}\right) & -sin\left(\theta-\frac{2pi}{3}\right) & 1 \\ cos\left(\theta+\frac{2pi}{3}\right) & -sin\left(\theta+\frac{2pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V^*_{Dd} \\ V^*_{Dq} \\ V^*_{D0} \end{bmatrix}. \tag{6}$$

3.3 | Reduced carrier pulse width modulation scheme

In literature, phase shift pulse width modulation (PSPWM) and line shift pulse width modulation-phase opposite disposition (LSPWM-POD) techniques are not suitable to three-phase MLIs because of its poor THD performance inline voltages.[42] Some modifications are required in carrier arrangements of conventional schemes[43,44] to improve

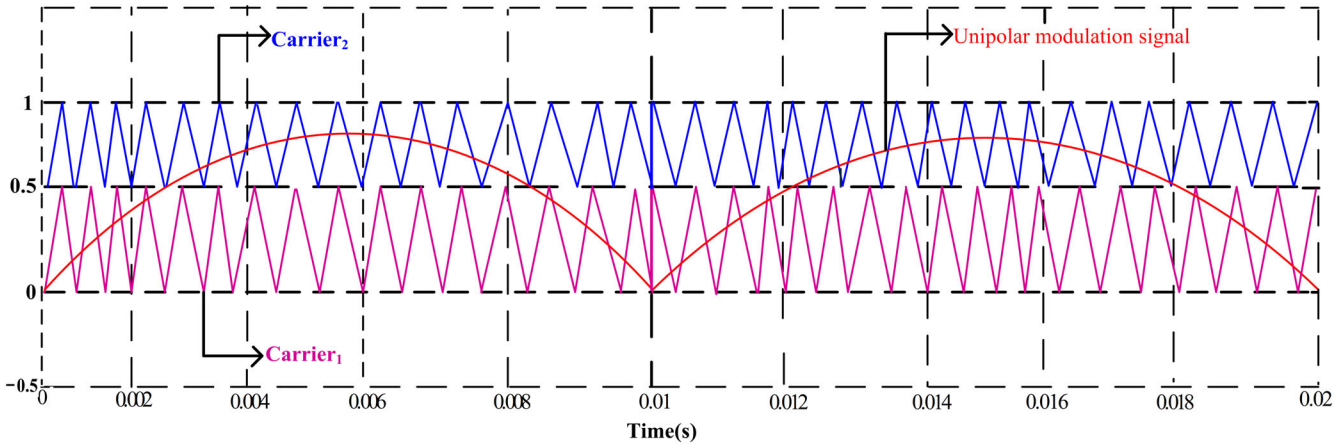

FIGURE 7 Reduced carrier pulse width modulation scheme

MLI harmonic performance. Therefore, reduced carrier modulation scheme is proposed; it gives better performance compared with other conventional modulation schemes. Reduced carrier pulse width modulation scheme requires $(n-1)/2$ carrier signals and single unipolar modulation signal to acquire "n" level voltages. Carrier signals and single unipolar modulation signal arrangement for proposed T-type MLI are depicted in Figure 7. The peak of the carrier signal (V_c) is obtained from Equation(7), and amplitude modulation index is obtained from Equation (8).

$$V_{\mathrm{c}} = \frac{2}{(n-1)} \tag{7}$$

$$m_{\mathrm{a}} = \frac{2V_{\mathrm{m}}}{(n-1)V_{\mathrm{c}}} \tag{8}$$

where V_c is the peak of the carrier signal and V_m is the peak of the modulation signal; "n" is the phase voltage levels. Minimum and maximum values of each carrier obtained from (9) and (10) and frequency modulation signal m_f are calculated from Equation (11).

$$carrier_{\mathrm{imax}} = \frac{2i}{(n-1)} \tag{9}$$

$$carrier_{\mathrm{imin}} = \frac{2(i-1)}{(n-1)} \tag{10}$$

where "n" is the levels in phase voltages and "i" is the carrier number.

$$m_{\mathrm{f}} = \frac{f_{\mathrm{c}}}{f_{\mathrm{m}}} \tag{11}$$

where f_c is the frequency of the carrier signal and f_m is the frequency of the modulation signal. If the magnitude of the unipolar modulation signal is less than the peak of the carrier$_1$, then a phase voltage of 0 to V is obtained. Further, if the magnitude of the unipolar modulation signal is greater than the carrier$_1$, then V to 2 V voltages are obtained. The polarity of the output voltage is determined by the unipolar modulation signal in phase voltages. Figure 8 shows the switching pulses obtained by using a reduced carrier PWM scheme for a proposed inverter. Switching pulses of S_1 and S_2 drive the S_1 and S_2 switches, and switching pulses of S_3 and S_4 drive the S_3 and S_4 switches. S_1, S_3 and S_2, S_4 are complementary switches. Switching pulses of B_s drive the bidirectional switch, and bidirectional switch B_s should be

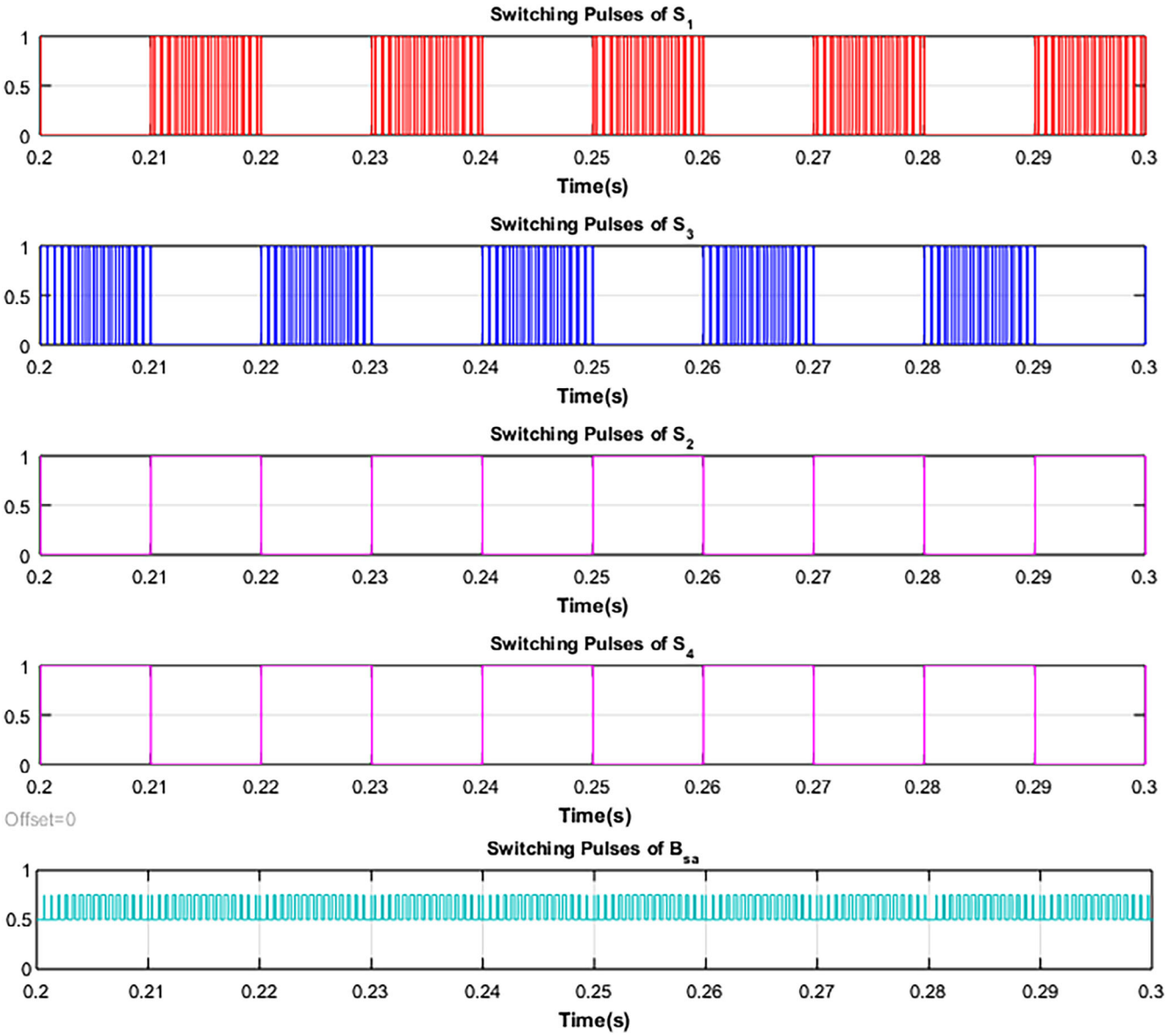

FIGURE 8 switching pulses of T-type multilevel inverter (MLI)

TABLE 4 Simulation system parameters

Sl.No	System Parameters	Simulation Values
1	Source voltage (V_{rms} Line-to-Line)	1 kV
2	Resistance/phase	0.005 Ω
3	Inductance/phase	0.1 mH
4	Filter resistance(R_f)	1.5 Ω
5	Filter inductance(L_f)	2 mH
6	Filter capacitance(C_f)	1100 μF
7	Switching frequency	2 kHz
8	DC-link voltage	$V_{dc1} = V_{dc2} = 350$ V
9	Load	100 kVA, 0.9 p.f

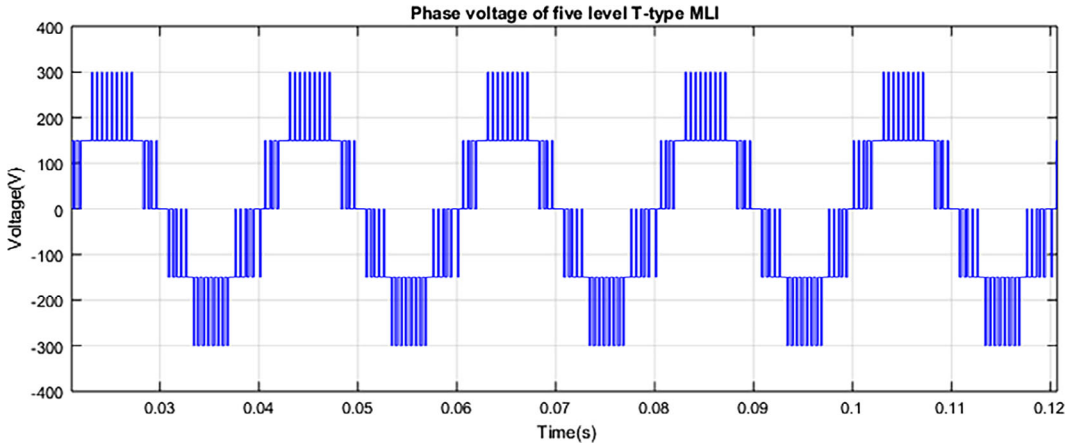

FIGURE 9 Phase voltage of five-level T-type multilevel inverter (MLI)

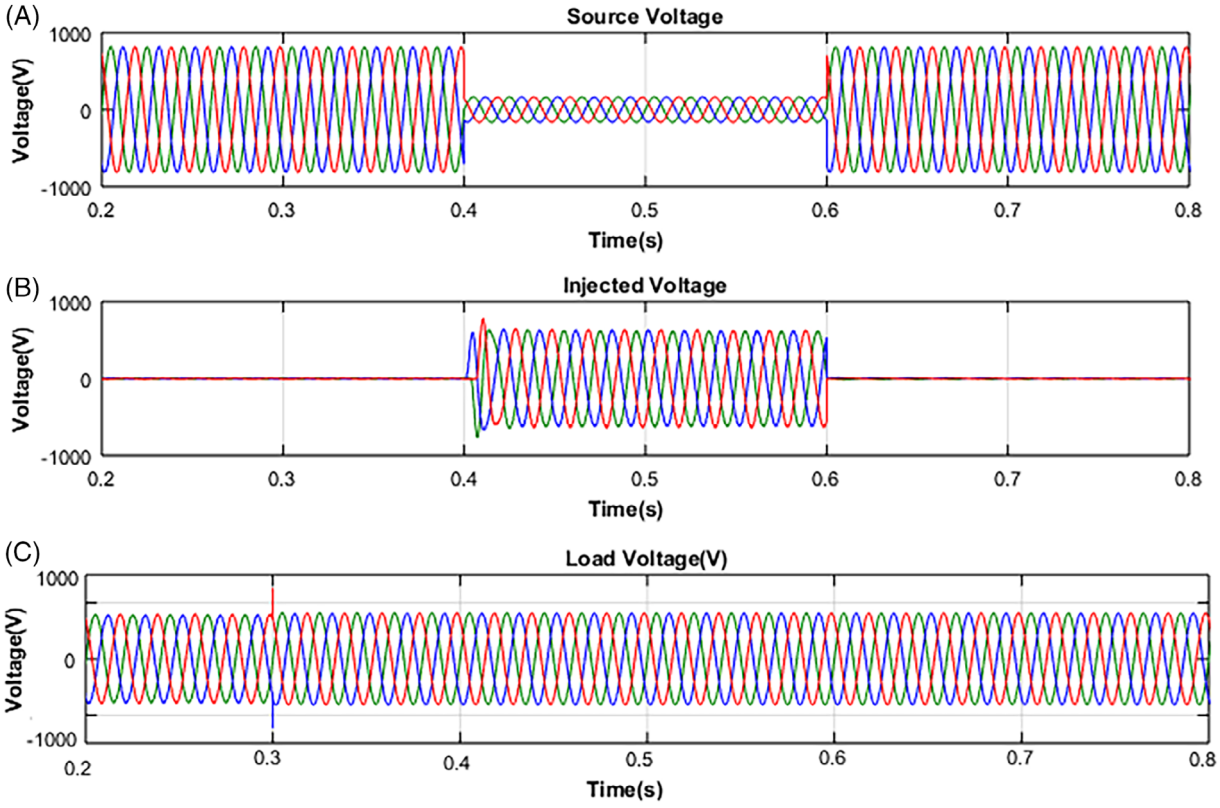

FIGURE 10 Simulation results of 80% voltage sag (A) source voltage, (B) injected voltage by dynamic voltage restorer (DVR), (C) load voltage

conducting with S_4 and S_2 switches, respectively, to obtain positive +V and −V voltages. The switching pulses obtained at 2-kHz carrier frequency and $m_a = 0.9$.

4 | SIMULATION RESULTS

The performance of Transformerless T-type MLI-based DVR is verified in the MATLAB/Simulink software. The performance of the DVR tested for voltage sag and swell scenarios. Table 4 shows the simulation system parameters.

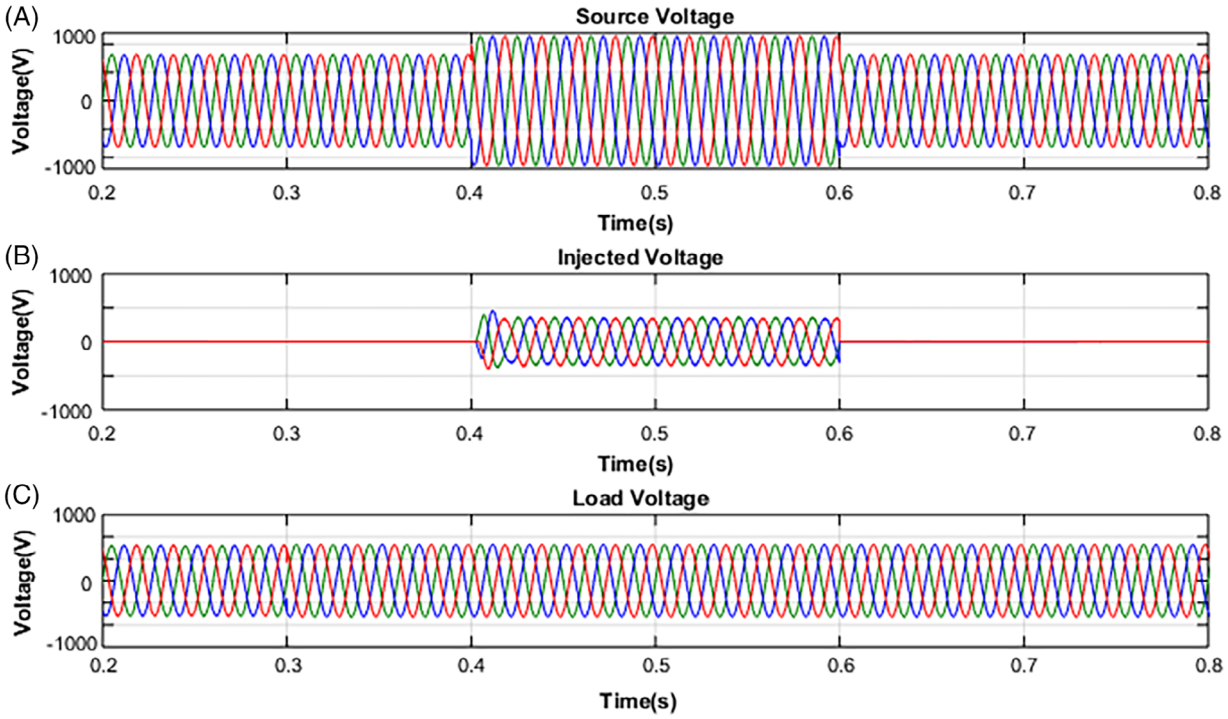

FIGURE 11 Simulation results of 50% voltage swell (A) source voltage, (B) injected voltage by dynamic voltage restorer (DVR), (C) load voltage

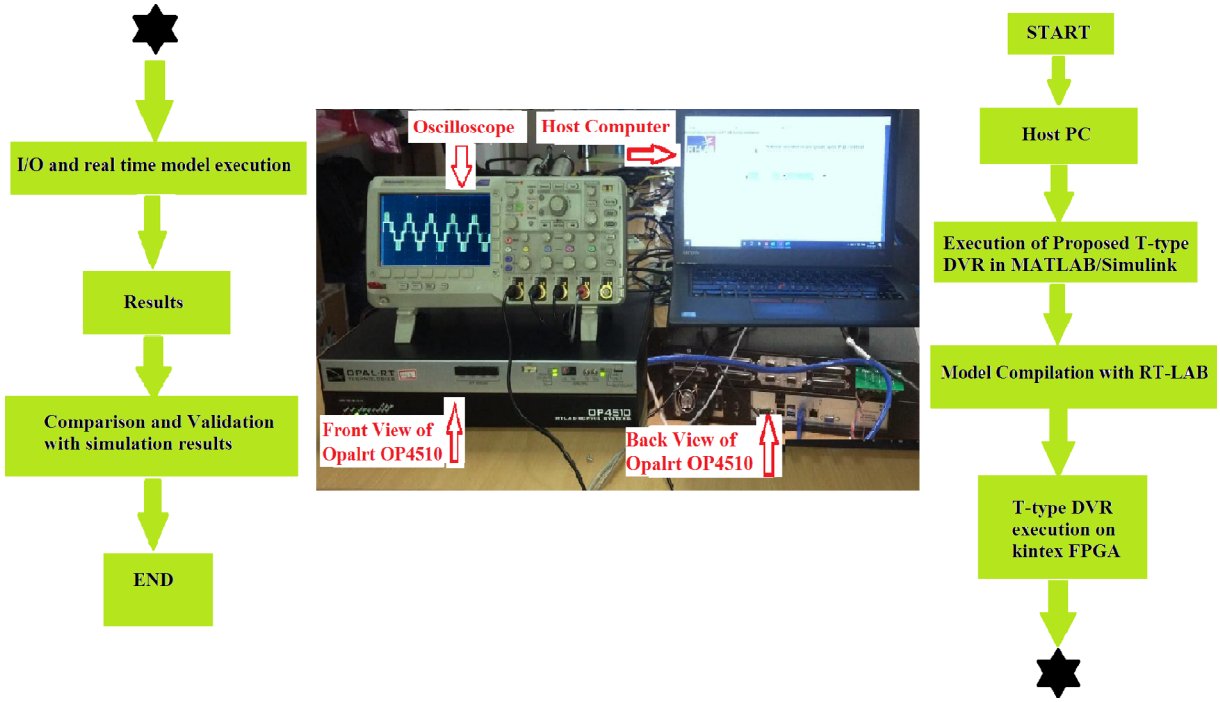

FIGURE 12 Real-time prototype setup with OPAL-RT

Figure 9 shows the phase voltage of five-level T-type MLI, before the output filter. Figure 10 shows the simulated results of the DVR for voltage sag compensation. The source voltage is in normal position until 0.4 seconds. From 0.4 to 0.6 seconds, 80% voltage sag occurred in source voltage, then the DVR will compensate the required voltage in series between the source and load to keep load voltage at the desired value. Simulated results of the DVR for voltage swell

compensation are shown in Figure 11. The source voltage is stable until 0.4 seconds. From 0.4 to 0.6 seconds, 50% voltage swell occurred in source voltage then the DVR will compensate for the necessary voltage. Despite voltage swell in the source voltage, the sensitive loads are protected by DVR with an injection of phase opposed voltage to the source voltage.

5 | REAL-TIME RESULTS

RT-LAB allows the users to simulate the readily available simulink model in the real-time simulation platform through RT-laboratory setup and then conduct the real-time simulation work on a targeted computer equipped with multicore peripheral component processors.[45] This RT-LAB setup is particularly used in HIL and RCP applications.[46] It handles transparently synchronization and user interaction with input/output boards and data exchanges for seamless distributed execution. Real-time (RT) simulation hardware technology is important for the design and test procedure of different types of electrical systems like adjustable speed drives, power converters, CPD, and the power grid. RT-LAB reduces the risks for plant operations and saves time. Hardware In Loop (HIL)-based real-time simulator is used to test the prototypes in real-time domain.[47-49] However, in this paper, Software In Loop (SIL)-based real-time simulator, OPAL-RT OP4510, is used to test the performance of the proposed T-type topology-based DVR. The proposed T-type MLI-based DVR modeling and simulation is synchronized to the OPAL-RT using real-time software, which interface with the sensing boards, host computer, OP4510 configurable board, Kintex-7 field programmable gate array (FPGA) synchronization to a real-time lab by using OP4510.[50] It is a fast processor up to 3.5-GHz frequency. The results are verified in

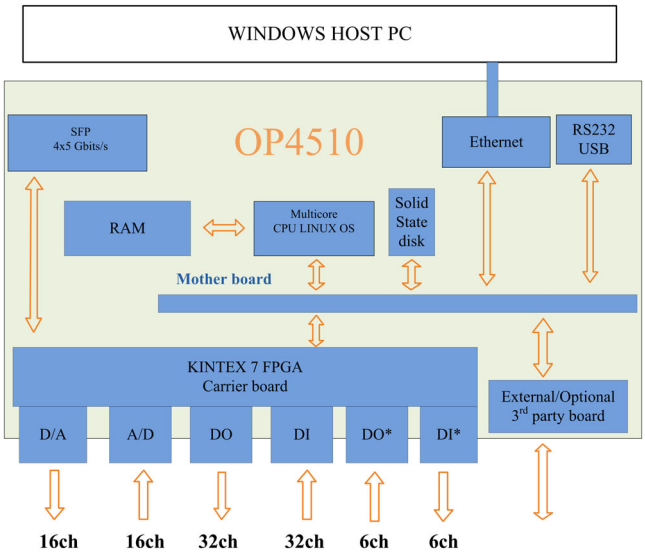

FIGURE 13 OPAL-RT architecture

TABLE 5 Real-time system parameters

Sl.No	Parameters	Values
1	Power supply voltage range	185-260 V
2	Sampling time (T_s)	20 μs
3	Gain factor	0.01
4	Performance time on FPGA chip	250 ns
5	Model of FPGA processor	Kintex-7 FPGA
6	Digital channel input voltage	5 V to 50 V
7	Digital channel output voltage	5 V to 30 V
8	Analog channel input voltage	±20 V
9	Analog channel output voltage	±16 V

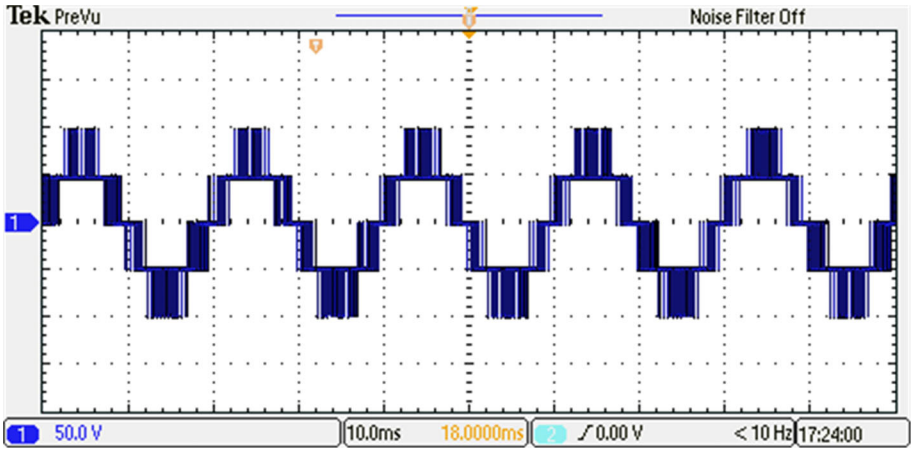

FIGURE 14 Phase voltage of five-level T-type multilevel inverter (MLI) (scale: volts/div = 50 V,time/ div = 10 ms)

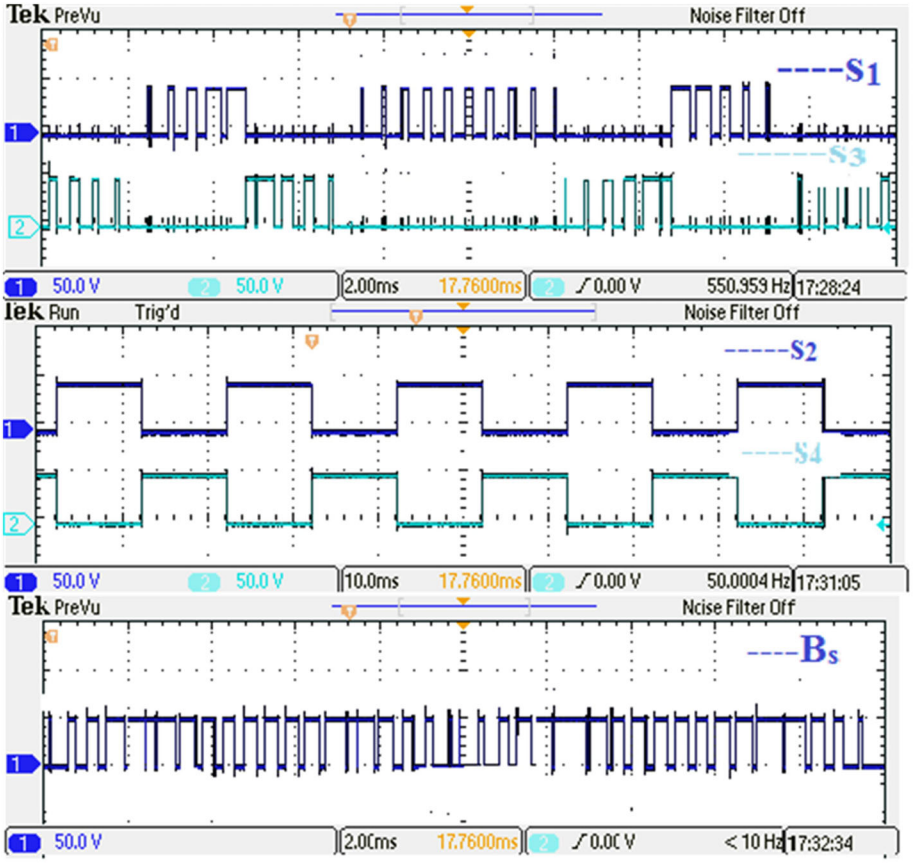

FIGURE 15 Real-time driving signals for the switching devices S_1, S_3, S_2, S_4 and B_s

oscilloscope connecting through mini BNC probes to OPAL-RT OP4510. The real-time prototype setup with OPAL-RT is shown in Figure 12.

It has 16 analog input and output channels and 32 digital input and output channels as shown in Figure 13. Table 5 shows the real-time system parameters. Five-level T-type MLI output phase voltage is shown in Figure 14. Figure 15 shows the switching pulses of T-type MLI; these digital pulses are obtained by real-time OPAL-RT, OP4510. T-type MLI DVR model synchronizes to OPAL-RT real-time software. To get these digital signals externally, ±5 V are given to the 18 and 37 digital output pins, and to get output voltages, the scale was decreased by a factor of 100 in voltage measurements. S_1 and S_3 are complementary pulses and also S_2 and S_4. B_s signal drives with S_4 and S_2 switches to obtain +V and −V voltages. Real-time results of T-type MLI DVR with voltage sag as shown in Figure 16. These analog signals are obtained by real-time laboratory software OP4510. Figure 16 shows the 80% voltage sag in source voltage during 0.4 to 0.6 seconds. During this time, interval load voltage will be distorted, and the DVR will compensate the required voltage

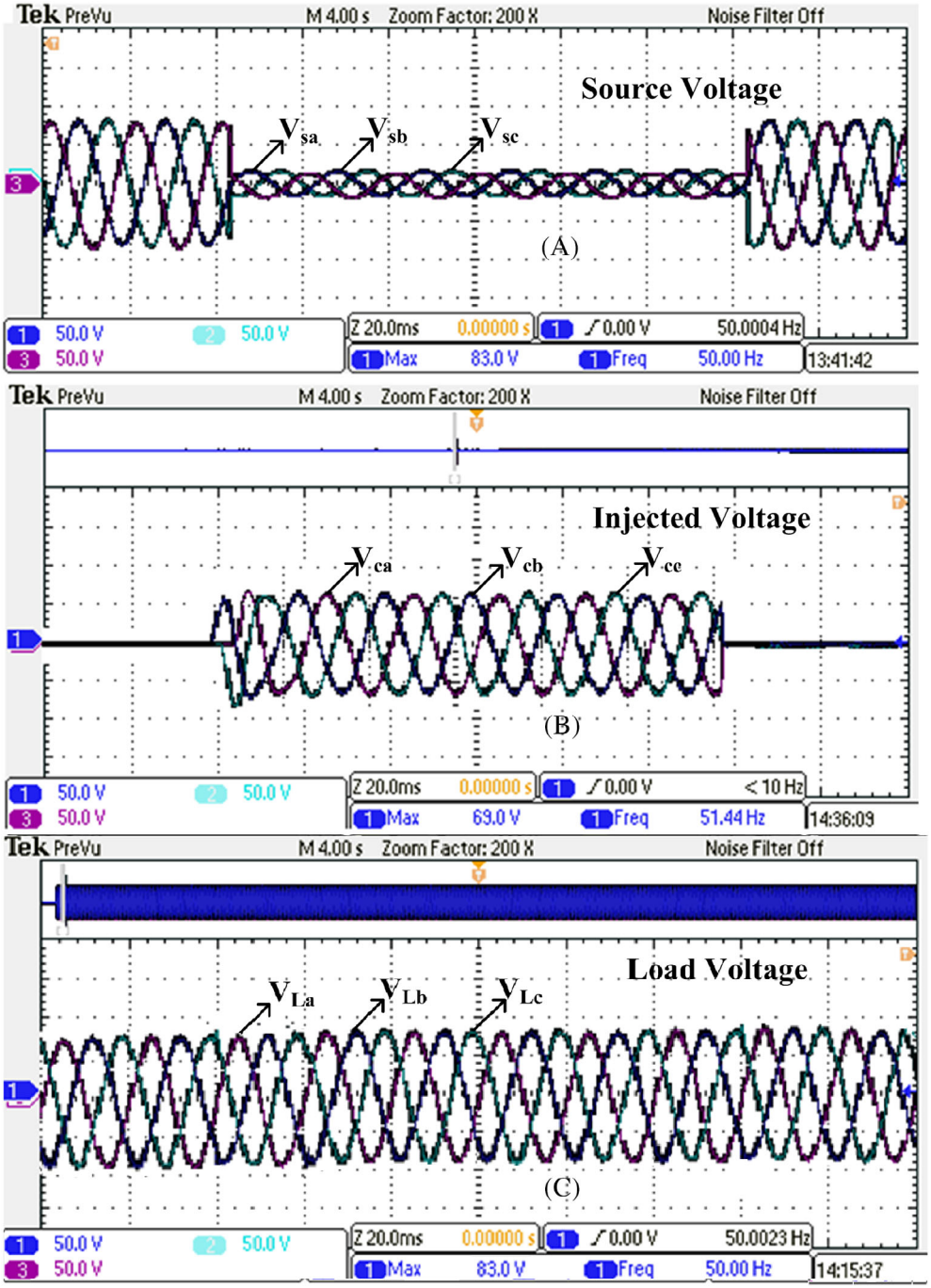

FIGURE 16 Real-time results of 80% voltage sag (A) source voltage, (B) injected voltage by dynamic voltage restorer (DVR), (C) load voltage (scale: volts/div = 50 V, time/div = 20 ms)

to restore the desired voltage at load terminals, and Figure 17 shows the real-time results for a 50% voltage swell in the source voltage during 0.4 to 0.6-second time interval; DVR will get activated to compensate the equivalent voltage at load terminals without affecting grid voltage fluctuations.

5.1 | Analysis of total harmonic distortion

The harmonic spectrum of the load current and voltage are shown in Figure 18–21 for the proposed configuration using LSPWM-POD and RCPWM techniques. Total harmonic distortion (THD) values of both PWM techniques are shown in Table 6. Reduced carrier PWM technique gives less THD in line current and voltage for T-type MLI DVR compared with LSPWM-POD technique.

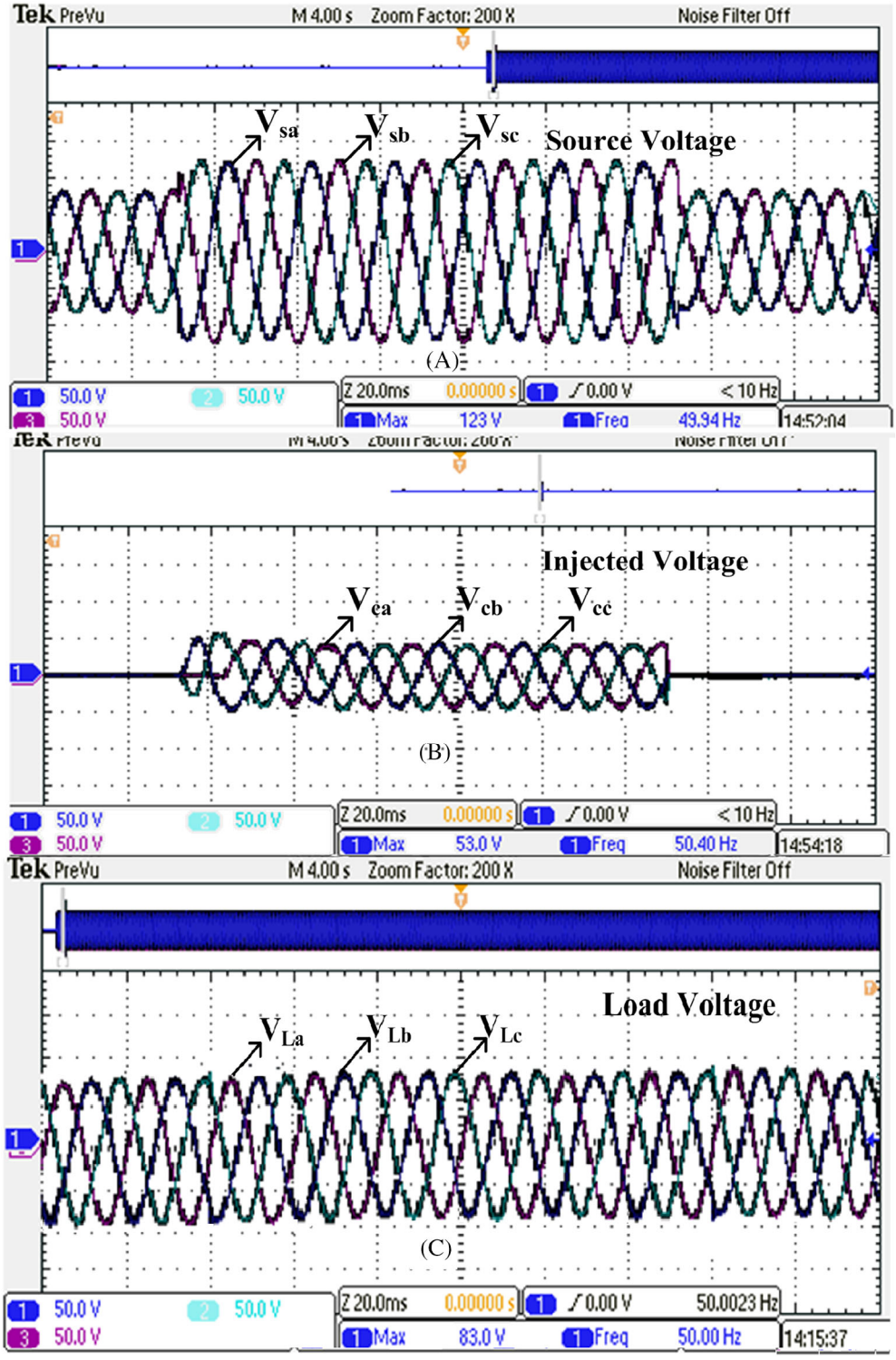

FIGURE 17 Real-time results of 50% voltage swell (A) source voltage, (B) injected voltage by dynamic voltage restorer (DVR), (C) load voltage (scale: volts/div = 50 V, time/div = 20 ms)

6 | CONCLUSION

In this paper, the design and development of a T-type MLI topology for the application of transformerless DVR to alleviate the voltage swell and voltage sag are explained. The advantage of this topology is to reduce the number of switches compared with other conventional topologies. Transformerless DVR leads to reduced cost and difficulty of the DVR. The performance and the efficiency of the proposed DVR are verified by simulation results as well as real-time prototype setup with OPAL-RT results. In addition, the DVR is controlled by abc to dq controller. The capability of the five-level T-type MLI-based DVR is tested using in-phase compensation technique with reduced carrier PWM scheme to

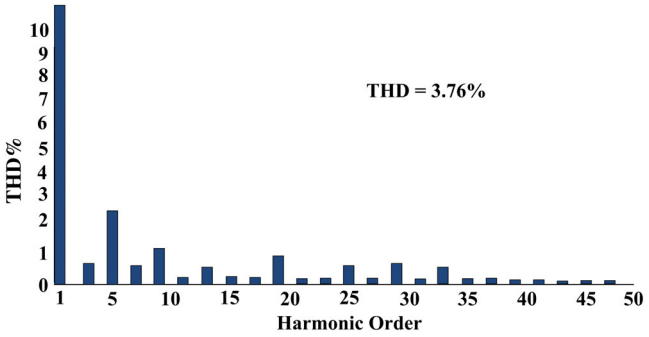

FIGURE 18 FFT spectrum of load current for T-type MLI DVR with LSPWM-POD

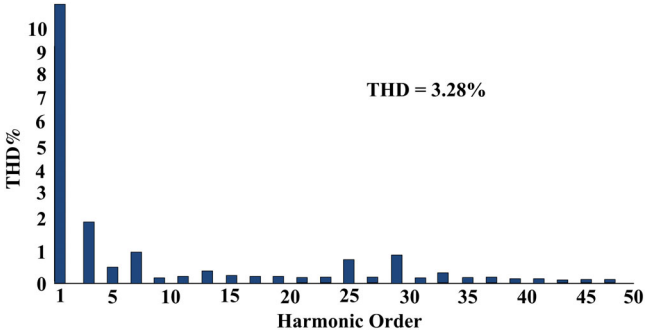

FIGURE 19 FFT spectrum of load current for T-type MLI DVR with Reduced carrier pulse width modulation (PWM)

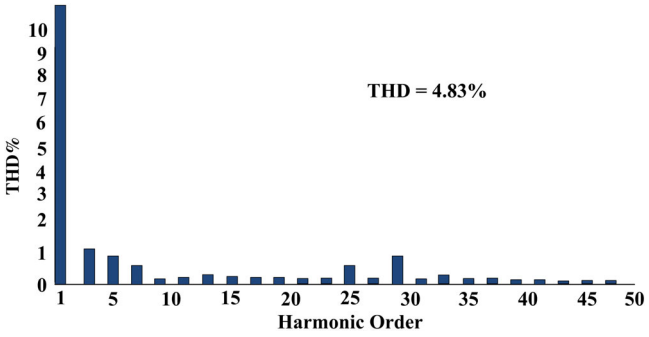

FIGURE 20 FFT spectrum of load voltage for T-type MLI DVR with LSPWM-POD

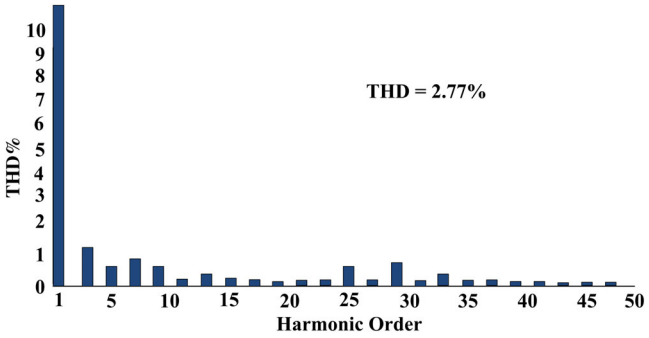

FIGURE 21 FFT spectrum of load voltage for T-type MLI DVR with reduced carrier pulse width modulation (PWM)

Inverter	Modulation Technique	THD %	
		Load Current	Load Voltage
T-type MLI	LSPWM-POD	3.76%	4.83%
	RCPWM	3.28%	2.77%

TABLE 6 THD comparison of LSPWM-POD and RCPWM techniques

improve THD in line voltages. The proposed DVR is able to keep the load current and voltage THD under the specified limits of IEEE-1159 standard. Also, the compensation capability of the proposed DVR is very fast in compensating the voltage sag and voltage swell.

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