Arabian Journal for Science and Engineering
https://doi.org/10.1007/s13369-019-03740-x

RESEARCH ARTICLE - ELECTRICAL ENGINEERING

One-Cycle Controlled Bridgeless SEPIC with Coupled Inductors for PAM Control-Based BLDC Drive

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Received: 9 August 2018 / Accepted: 1 February 2019

Abstract
This paper presents a novel approach for the speed control of BLDC motor for residential air conditioning application, using pulse amplitude modulation (PAM) control of voltage source inverter (VSI). PAM control of VSI is accomplished by using a bridgeless SEPIC converter embedded with coupled inductors at the front end and adopting one-cycle control (OCC) technique in the inner voltage control loop. The DC reference voltage required for inner voltage control loop is obtained using a PI controller in the outer speed control loop and speed feedback signal. The PAM control (DC supply voltage control) of VSI reduces switching losses by allowing the operation of VSI at fundamental frequency. Bridgeless SEPIC with coupled inductors is designed to enable PAM control for VSI and is operated in discontinuous conduction mode (DCM) for the complete range of DC link voltage. DCM operation simplifies power factor correction control scheme to a simple voltage follower approach, since it has inherent input current shaping feature. The introduction of coupled inductors in the bridgeless SEPIC converter lowers the overall count of components, allows better integration and lowers the requirement of inductance, compared to conventional bridgeless SEPIC. OCC which is a nonlinear control technique, used in the voltage control loop, enhances the performance with improved startup and transient state response. It also improves the quality of supply current drawn by reducing the distortion compared to PI control technique. The proposed BLDC motor drive is modelled and simulated using MATLAB/Simulink. The performance of proposed system is evaluated for a wide range of speed control. The experimental prototype for bridgeless SEPIC with coupled inductors is implemented. The inherent power factor correction for supply voltage variations is validated using the results. The bridgeless operation of the converter with coupled inductor configuration is also described with experimental waveforms at rated supply voltage of 220 V.

Keywords Pulse Amplitude Modulation · Bridgeless SEPIC · Coupled inductors · DCM · One-Cycle Control

1 Introduction

The demand for well-furnished and provisioned infrastructure and growing awareness on importance of indoor air quality have led to the growth of air conditioning systems. Conventional ON/OFF type control of compressor motors in air conditioners is replaced by adjustable speed drives with inverter technology [1]. Research in adjustable speed drives used for compressor is aimed at obtaining high power density, increased motor efficiency and better performance at a minimised cost. Owing to the advantages like high energy efficiency, high torque/inertia ratio, ruggedness and low maintenance, brushless DC motors are substituting conventional motors used in air conditioners [2]. Brushless DC motor is a permanent magnet synchronous motor having trapezoidal back emf. Three-phase winding is employed on the stator of this motor, and for rotor, permanent magnets are used. The motor is commutated electronically by energising stator windings with a three-phase VSI depending on rotor position information [3].

Conventionally, BLDC drive for compressor involves a VSI-fed BLDC motor supplied from single-phase mains through an uncontrolled bridge rectifier. In such an arrangement, generally the speed control of brushless DC motor is achieved by PWM control of VSI. It leads to high switching losses in VSI and requires motor current sensors. Conventional BLDC drive draws highly distorted current from the

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Published online: 19 February 2019

supply with large peak overshoot and low power factor. This results in violation of power quality standards specified by IEC 61000-3-2. The power quality issues related to traditional diode rectifier-fed BLDC motor drive invite the need for power factor correction (PFC) converter for input current shaping [4, 5]. A PFC converter with wide range of output voltage modulation allows speed control of BLDC motor by pulse amplitude modulation (PAM) control of three-phase VSI [6–9]. This method facilitates VSI to operate at the fundamental frequency and thereby lowers switching losses compared to PWM control. Also, it eliminates the need for motor current sensors.

The research works done in [6–9] explain the realisation of PAM control by controlling the input DC voltage of VSI for a wide range using a PFC converter capable of providing both lower and higher voltage than its input voltage. As discussed in the literature, the PFC converter configurations Cuk [6], buck–boost [7], single-ended primary-inductance converter (SEPIC) [8] and Zeta converter [9] converters supply wide range of output voltage, as they can be controlled to step-up and step-down their input voltage. In these converters, buck–boost and Cuk configurations have negative output voltage polarity which complicates the control implementation and Zeta has high EMI problem due to the switch in series with the supply [10]. So the best alternative is SEPIC, which provides an output voltage of positive polarity and undergoes lesser EMI issues.

The PFC converter can operate either in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM). DCM operation exhibits more stress on switching devices, but has inherent supply current shaping property. By operating PFC converter in DCM, control scheme simplifies to voltage mode control approach; therefore, the inner current loop can be eliminated. However, due to the switching stress, it is restricted to low and medium power applications [11].

Since diode rectifier involves more conduction losses, recent PFCs employ bridgeless topologies [12], where it includes only one slow diode in the conduction path. The conventional configuration of bridgeless SEPIC is presented for PAM control of BLDC motor in [13]. The topology consists of two DC–DC SEPIC converters, one to operate in the positive half cycle and another to operate during the negative half cycle of supply mains. Due to that, the conventional bridgeless topology of SEPIC converter has more number of components, increased size and weight.

In order to minimise the size and number of elements involved, some alternate bridgeless topologies have been developed for bridgeless SEPIC configuration. The bridgeless SEPIC topology developed in [14] has three inductors, and requirement of an additional gate drive circuitry. The structure becomes more complex due to increased number of capacitors. The reduced number of component topology for bridgeless SEPIC introduced by Mahdavi et al. in [15,16] also needs an additional driver circuitry for the switches. The topology presented in [17] has less number of components, and it has been presented for PAM control of BLDC drive in [18]. However, this topology has a limitation of high side gate drive requirement. This demands for a bridgeless SEPIC topology which can reduce size avoiding structure complexity and additional/high side gate drive requirement. Incorporating the coupled inductors for SEPIC converter reduces the size and weight, and it retains the advantage of possessing only one low side gate driver [19].

The generation of reference DC voltage, for DC bus voltage control, is achieved by multiplying reference speed with motor voltage constant [13,18]. The DC bus voltage for BLDC drive is also a function of load torque and motor winding parameters such as resistance and inductance [20]. The rate limiter is utilised in [21], which incorporates the effect of winding parameters. This limits the rate of rise of current drawn from dc link during transient state. The equation incorporating the effect of motor winding parameters and the dc link current equivalent to load torque is presented in [22] for generating the reference DC voltage. The research work in [23] uses a speed control loop which process the error in actual and desired speed to generate the reference DC voltage. In the proposed work, the speed feedback is utilised to generate the DC voltage using PI controller in the outer speed control loop. This approach provides better speed control as compared to the methods used to generate reference voltage without sensing the speed.

The conventional PI controller employed in the voltage control loop exhibits poor performance, causing transient oscillations and large peak overshoots under parameter variation, load disturbance, etc [24–27] and [28]. This demands for sophisticated control technique for DC link voltage control. A simple nonlinear control proposed by Smedley called as one-cycle control (OCC) can be employed for controlling the output of dc–dc converter [29]. Basically, OCC controls the duty cycle of the power switch in the dc–dc converter such a way that the average DC output voltage always matches the reference DC voltage. The OCC finds application in both PWM and quasi-resonant power converters. There is improvement in the steady-state and transient response characteristics of the converter with the application of OCC [30]. The OCC is realised using a resettable integrator which integrates the output voltage of the converter. The integrator output is continuously compared with the reference DC voltage. At the instant when both the quantities match, the power converter switch is turned off, and the integrator is reset to zero value. The power switches operate in constant switching frequency to conceptualise OCC method. The OCC finds application in power factor correction control schemes also [31, 32]. This control is proved as simple and efficient solution even for bridgeless topology of PFC con-

verters [33]. One-cycle control introduced for BLDC drive with PAM control performs the speed control efficiently [34].

In view of all the above, this paper presents bridgeless SEPIC with coupled inductors adopting one-cycle control technique for the PAM control-based BLDC drive used in residential air conditioning application. The OCC is applied to the inner voltage control loop in the proposed dual-loop control for the BLDC drive. The outer speed loop is realised using a PI controller. Coupled inductors reduce size and weight since a single core is used to wind the two inductors of a SEPIC converter. It also effects in reduction of self-inductance value, hence decreases the number of turns of windings. Thus, it reduces magnetic losses and improves efficiency. The generation of reference DC voltage for the voltage control loop, using outer speed control loop, assures the accurate reference voltage required for precise speed control using PAM method. One-cycle control adopted in DC voltage control loop obtains better control performance over a wide speed range, along with improving the quality of current drawn from the supply.

The continuation of this paper has the description of the proposed system in Sect. 2, which involves the operation of bridgeless SEPIC, the effect of coupled inductors in SEPIC topology and design of the proposed converter. Control of the proposed system is described in Sect. 3. Section 4 deals with the results obtained and the detailed discussions. Finally, conclusions obtained from the work are discussed in Sect. 5.

2 System Description of Proposed BLDC Drive with PAM Control of VSI

This work proposes bridgeless SEPIC with coupled inductors using one-cycle control for speed control of the BLDC motor. The block diagram of the overall system is shown in Fig. 1. The PAM control of VSI is done by controlling the duty ratio of the proposed SEPIC converter. The duty cycle of the SEPIC converter is controlled using OCC which forms the inner control loop so as to obtain wide range of voltage variation at the DC link.

The gating pulses for VSI are governed by rotor position signals (H_a, H_b, H_c) from BLDC motor. The electronic commutation logic provides switching signals for the VSI at the fundamental frequency. This rotor position sensor-based commutation reduces the high frequency switching losses in VSI.

The speed control of BLDC motor is realised using dual-loop controller with outer speed control loop and inner voltage control loop using OCC. The OCC controls the duty cycle of the SEPIC converter. The reference DC voltage (V_{dc}^*) needed in the OCC is obtained from the outer speed control loop. A PI controller is used in the outer loop to process the error (N_e) in the actual speed (N) and the reference speed (N^*). This ensures the precise generation of reference DC voltage corresponding to a reference speed for wide range of reference speed.

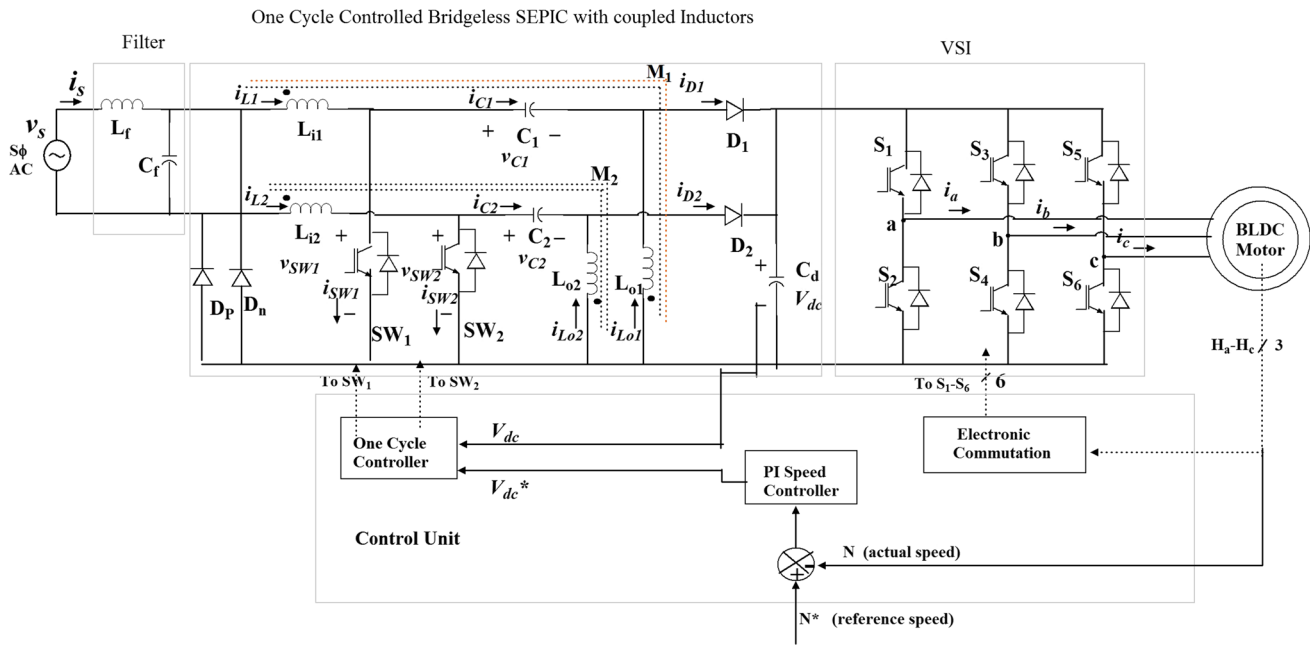


Fig. 1 Block diagram of BLDC drive with PAM control using bridgeless SEPIC with coupled inductors

2.1 Operation of the Proposed Bridgeless SEPIC with Coupled Inductors

In the bridgeless SEPIC with coupled inductors, one-cycle control technique is employed to control DC bus voltage (V_{dc}) over a wide range by modulating the duty ratio of switches.

From Fig. 1, it can be seen that the bridgeless configuration of SEPIC converter consists of two SEPIC converters, one converter to operate during positive half cycle duration of supply voltage and another to operate during negative half cycle of supply voltage. The SEPIC converter consisting of elements L_{i1}, L_{o1}, C_1, C_d, D_1, SW_1 operates for the positive half cycle of the supply. The rectifier diode D_p completes the path for the positive half cycle of the supply. For the negative half cycle, the components L_{i2}, L_{o2}, C_2, C_d, D_2, SW_2 operate along with rectifier diode D_n. The dotted line shows the magnetic coupling between the two inductors of SEPIC converter. Inductors L_{i1}, L_{o1} are coupled and have mutual inductance M_1, and similarly, inductors L_{i2}, L_{o2} are coupled and the mutual inductance of M_2 is developed between the windings.

Figure 2 shows the circuit diagram for operation of bridgeless SEPIC for positive half cycle of the supply mains. DCM operation of SEPIC constitutes of three intervals in each switching cycle. Figure 3 shows the circuit for three intervals of operation in a switching cycle, and Fig. 4 shows the corresponding waveforms for operation of the proposed drive for a switching cycle in positive half cycle duration of supply.

In interval I, where switch is ON, diode is OFF as shown in Fig. 3a and the input inductor (L_{i_1}) and output inductor (L_{o_1}) start charging. The intermediate capacitor (C_1) discharges via inductor (L_{o_1}) at the output side, and the voltage across it decreases. The diode (D_1) remains in the OFF state, and the capacitor (C_d) at DC link supplies the energy requirement of the load VSI-fed BLDC motor.

In interval II, where switch is OFF, and diode is ON as can be seen in Fig. 3b and the input inductor (L_{i_1}) and inductor (L_{o_1}) at output side start discharging via diode (D_1). The intermediate capacitor (C_1) charges in this interval of operation. The capacitor (C_d) at DC link also charges in this interval. Inductors transfer energy to the load.

In interval III, depicted in Fig. 3c, the switch is OFF, and the diode is also OFF. The inductors (L_{i_1}) and (L_{o_1}) are completely discharged. A nonzero remaining current will flow through inductors and intermediate capacitor. The energy required to the load VSI-fed BLDC motor is supplied by DC link capacitor (C_d).

The operation can be analysed in a similar way also for the negative half cycle of supply voltage .

2.2 Effect of Coupled Inductors in the SEPIC Topology

In order to analyse the effect of introducing the coupled inductors in SEPIC topology, the SEPIC converter operating in positive half cycle is considered and the circuit diagram is shown in Fig. 2.

The SEPIC converter consists of two inductors: inductor with self-inductance of L_{i1} at input side and inductor with self-inductance of L_{o1} at output side. Two inductors L_{i1}, L_{o1} are coupled magnetically. The coupling coefficient and the mutual inductance are k_{c1} and M_1, respectively.

The coupling coefficient k_{c1} in terms of self-inductance and mutual inductance is given by (1).

$$k_{c1} = \frac{M_1}{\sqrt{L_{i1} L_{o1}}} \tag{1}$$

The turns ratio of the two windings n_1 is given by (2)

$$n_1 = \frac{v_{Lo1}}{v_{Li1}} = \frac{N_{o1}}{N_{i1}} = \sqrt{\frac{L_{o1}}{L_{i1}}} \tag{2}$$

where $v_{L_{i1}}$, $v_{L_{o1}}$ are the voltages across the inductors $L_{i1}$and L_{o1}, respectively. N_{o1} and N_{i1} are number of turns of coupled inductors $L_{i1}$and L_{o1}, respectively. Voltage across coupled

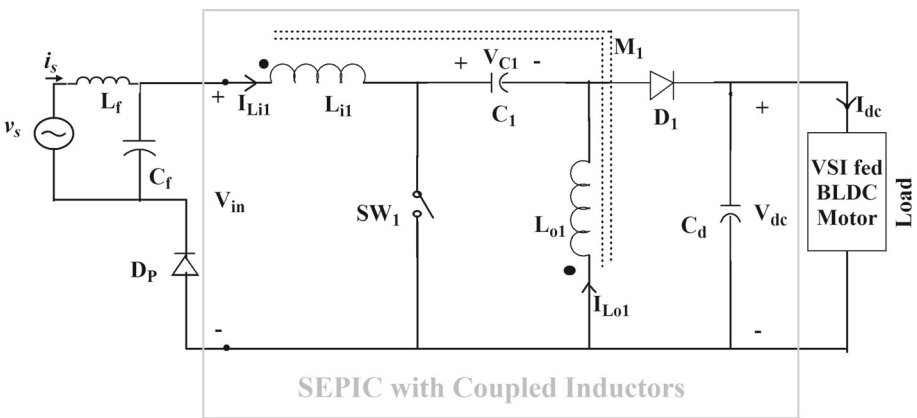


Fig. 2 Circuit diagram for positive half cycle operation of proposed bridgeless SEPIC

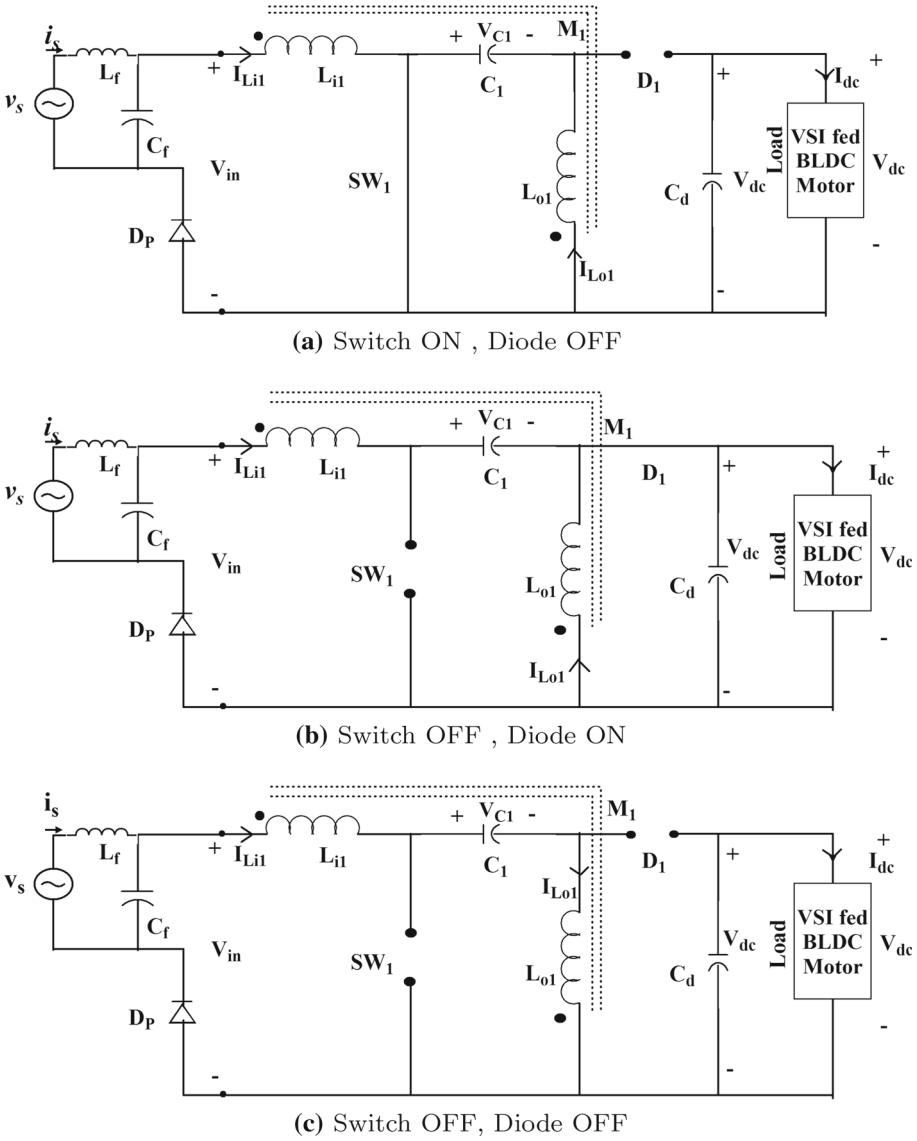


Fig. 3 Operation of proposed BLDC drive with PAM control for positive half cycle

inductor windings having self-inductances L_{i1} and L_{o1} is given by (3) and (4), respectively.

$$v_{L_{i1}} = L_{i1}\frac{di_{i1}}{dt} + M_1\frac{di_{o1}}{dt} \tag{3}$$

$$v_{L_{o1}} = M_1\frac{di_i}{dt} + L_{o1}\frac{di_{o1}}{dt} \tag{4}$$

From the circuit diagram in Fig. 2, it can be seen that the voltage across intermediate capacitor V_{c1} is equal to the input voltage V_{in} over a switching cycle, since the voltage across each inductor at steady state is zero. When switch SW_1 is ON, the voltage applied across inductor L_{i1} is input voltage V_{in}, and since L_{o1} is in parallel with C_1, the voltage applied across L_{o1} is also V_{in}. When the switch SW_1 is OFF, voltage applied across both the inductors is V_{dc}.

So the voltage across two inductors is same in every interval of a switching cycle, as given by (5)

$$v_{L_{i1}} = v_{L_{o1}} \tag{5}$$

The coupled inductors can attain zero ripple if it satisfies the relationship given by (6)

$$\frac{v_{L_{i1}}}{v_{L_{o1}}} = 1 = \frac{M_1}{L_{o1}} = k_{c1}\sqrt{\frac{L_{i1}}{L_{o1}}} \tag{6}$$

By substituting (5) into the mutual inductance model, (3) and (4) result in (7) and (8).

$$\frac{di_{L_{i1}}}{dt} = \frac{v_{L_{o1}}L_{o1} - v_{L_{i1}}M_1}{L_{i1} * L_{o1} - M_1^2} = \frac{v_{L_{i1}} - \frac{k_{c1} * v_{Lo1}}{n_1}}{L_{i1}(1-k_{c1}^2)} \tag{7}$$

$$\frac{di_{L_{o1}}}{dt} = \frac{v_{L_{i1}}L_{i1} - M_1 v_{L_{o1}}}{L_{i1} * L_{o1} - M_1^2} = \frac{v_{L_{o1}} - k_{c1} * n_1 * v_{Li1}}{L_{o1}(1-k_{c1}^2)} \tag{8}$$

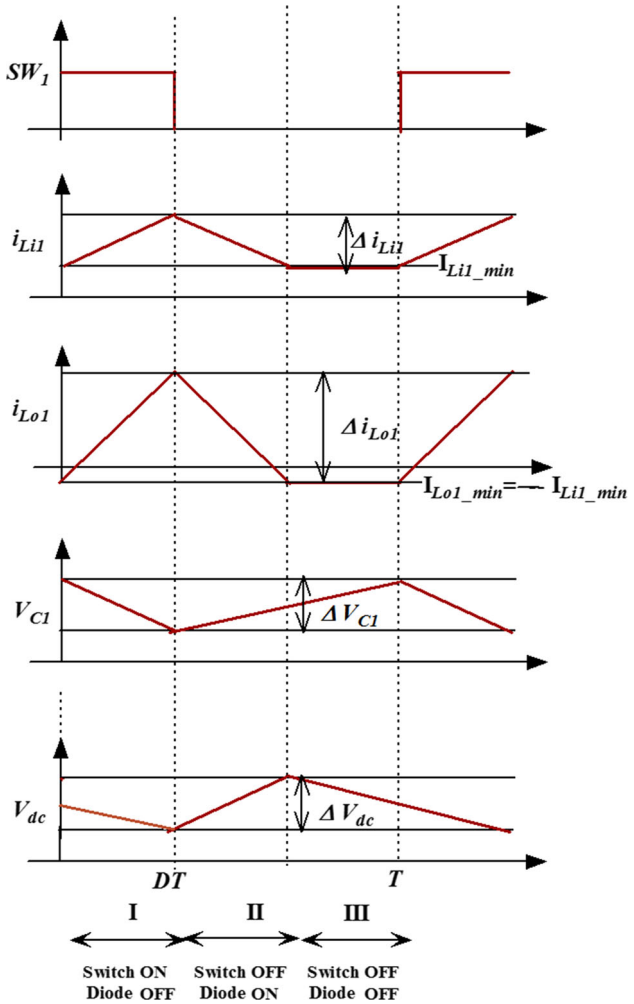


Fig. 4 Waveforms for operation of proposed BLDC drive with PAM control for positive half cycle

By comparing the ripple current formulae (7) and (8) with the corresponding equations obtained when there is no coupling between the two inductors, the model for equivalent inductance can be derived and is given by (9) and (10).

$$L_{\mathrm{i1eq}} = L_{\mathrm{i1}} \frac{1 - k_{\mathrm{c1}}^2}{1 - \frac{k_{\mathrm{c1}}}{n_1}} \tag{9}$$

$$L_{\mathrm{o1eq}} = L_{\mathrm{o1}} \frac{1 - k_{\mathrm{c1}}^2}{1 - k_{\mathrm{c1}} n_1} \tag{10}$$

where L_{i1eq} and L_{o1eq} are equivalent inductance values produced due to coupling effect.

Similarly, the equivalent inductance values produced as an effect of coupling L_{i2} and L_{o2} for converter operating in negative half cycle can be shown by (11) and (12)

$$L_{\mathrm{i2eq}} = L_{\mathrm{i2}} \frac{1 - k_{\mathrm{c2}}^2}{1 - \frac{k_{\mathrm{c2}}}{n_2}} \tag{11}$$

$$L_{\mathrm{o2eq}} = L_{\mathrm{o2}} \frac{1 - k_{\mathrm{c2}}^2}{1 - k_{\mathrm{c2}} n_2} \tag{12}$$

Above analysis shows that the equivalent inductance has effective value of self-inductance multiplied to a ratio determined by coupling coefficient and number of turns. Thus, for the same input current ripple, value of self-inductance of inductors in SEPIC converter can be reduced.

2.3 Design of Bridgeless SEPIC with Coupled Inductors for BLDC Drive

Bridgeless SEPIC with coupled inductors is designed for a wide range control of output voltage. Converter operation is ensured to be in DCM mode for the entire range of DC voltage. Hence, it achieves auto-shaping of supply current. The output DC voltage V_{dc} of the converter is a function of duty ratio (D), and it is given as (13)

$$V_{\mathrm{dc}} = \frac{D}{(1 - D)} V_{\mathrm{in}} \tag{13}$$

where V_{in} is the mean value of the input voltage to the SEPIC converter.

The input side inductors are designed for the ripple current of ΔI_{Lin} as given by (14)

$$L_{\mathrm{i1eq}} = L_{\mathrm{i2eq}} = \frac{V_{\mathrm{in}} * D}{\Delta I_{\mathrm{Lin}} * I_{\mathrm{in}} * f_s} \tag{14}$$

where $I_{\mathrm{in}} = \frac{P_{\mathrm{i}}}{V_{\mathrm{in}}}$. And $P_{\mathrm{i}} = \frac{P_{\mathrm{max}}}{V_{\mathrm{dcmax}}} * V_{\mathrm{dc}}$ is the input power for any value of DC voltage V_{dc}.

The output side inductor is expressed as (15)

$$L_{\mathrm{o1eq}} = L_{\mathrm{o2eq}} = \frac{V_s^2}{P_{\mathrm{i}}} \frac{V_{\mathrm{dc}} D}{2 V_{\mathrm{in}} f_s} \tag{15}$$

where V_{s} is the RMS value of supply voltage.

The self-inductances L_{i1}, L_{i2} of input side inductors of bridgeless SEPIC can be obtained from (9) and (11), and the self-inductances L_{o1}, L_{o2} of output side inductors are given by (10) and (12), respectively.

The intermediate capacitance with ripple voltage of ΔV_{c1} is obtained as (16)

$$C_{1,2} = \frac{P_{\mathrm{i}}}{\Delta V_{\mathrm{c1}} * f_s * (V_{\mathrm{in}} + V_{\mathrm{dc}})^2} \tag{16}$$

The DC link capacitor C_d, for the ripple voltage of δ, is obtained from (17)

$$C_d = \frac{P_{\mathrm{i}}}{2\omega\delta V_{\mathrm{dc}}^2} \tag{17}$$

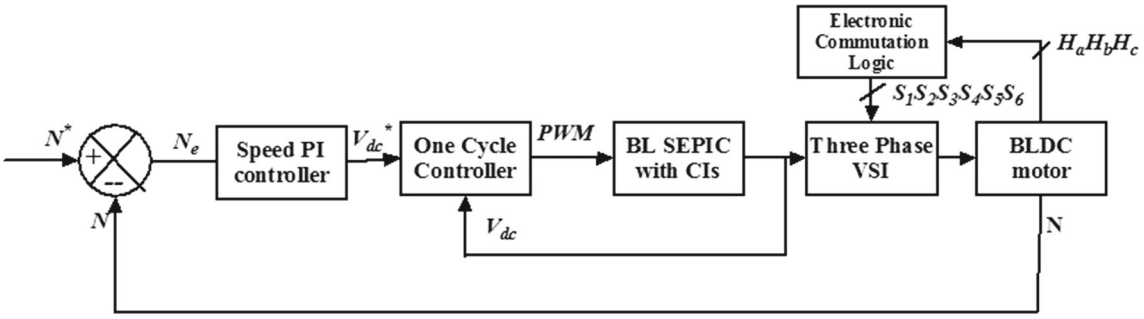


Fig. 5 Control flow schematic

Table 1 Energised phase voltages and corresponding switching sequences based on rotor position sensor signal

θ deg	Rotor position signal			Switching state						Phase voltages		
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6	V_{an}	V_{bn}	V_{cn}
NA	0	0	0	0	0	0	0	0	0	–	–	–
0–60	0	0	1	1	0	0	0	0	1	$V_{dc}/2$	0	$-V_{dc}/2$
60–120	0	1	0	0	1	1	0	0	0	$-V_{dc}/2$	$V_{dc}/2$	0
120–180	0	1	1	0	0	1	0	0	1	0	$V_{dc}/2$	$-V_{dc}/2$
180–240	1	0	0	0	0	0	1	1	0	0	$-V_{dc}/2$	$V_{dc}/2$
240–300	1	0	1	1	0	0	1	0	0	$V_{dc}/2$	$-V_{dc}/2$	0
300–360	1	1	0	0	1	0	0	1	0	$-V_{dc}/2$	0	$V_{dc}/2$
NA	1	1	1	0	0	0	0	0	0	–	–	–

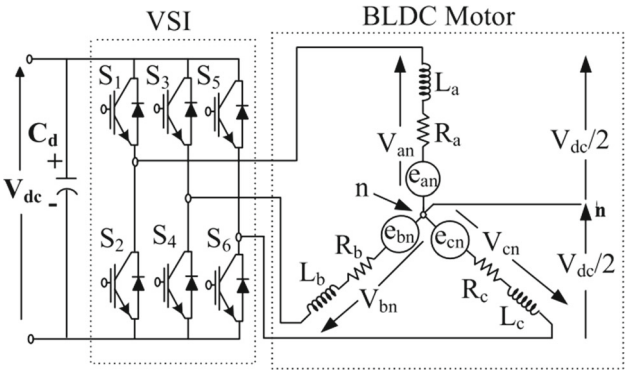


Fig. 6 A three-phase VSI-fed BLDC motor

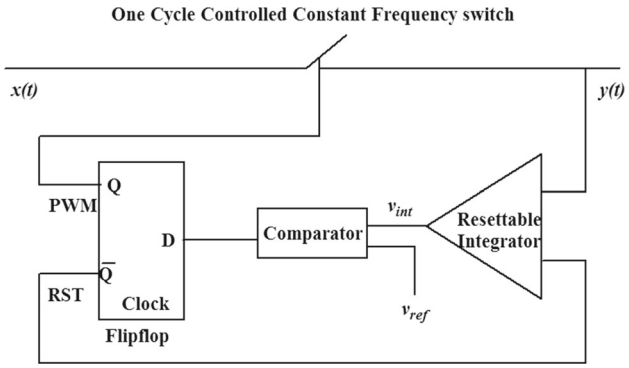


Fig. 7 One-cycle controlled constant frequency switch

The design of filter capacitance is done for its maximum value that is expressed by (18)

$$C_{\max} = \frac{I_m}{\omega V_m}\tan\theta \tag{18}$$

where θ is the phase angle between the output current and voltage of the filter.

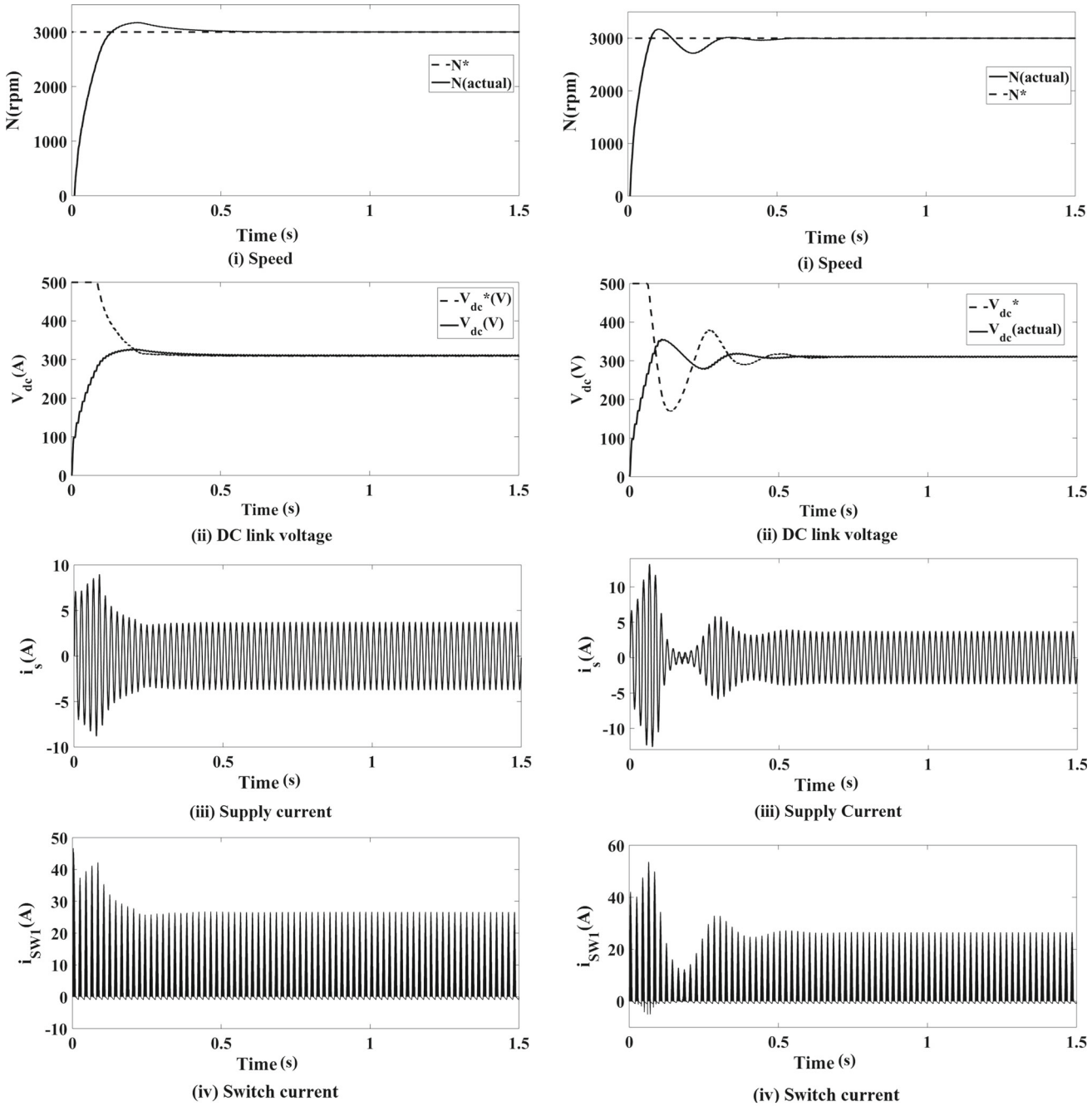
The design of filter inductance is evaluated for $f_c = f_s/10$, since $f_L < f_c < f_s$ using (19)

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} \tag{19}$$

3 Control of Proposed BLDC Drive

PAM control of three-phase VSI is used to achieve the speed control in the proposed BLDC motor drive. The control flow schematic of proposed drive is shown in Fig. 5. It consists of

- *Generation of switching logic for VSI*: The VSI is switched at fundamental frequency corresponding to rotor position signals obtained using hall sensors. Switching logic implemented for VSI is known as electronic commutation logic.
- *Outer speed control loop*: The actual speed is sensed and compared with reference speed. The reference DC volt-



(a) Performance of the drive with One Cycle Control **(b)** Performance of the drive with PI Control

Fig. 8 Performance of BLDC drive with PAM control using bridgeless SEPIC with coupled inductors for rated speed, under rated load and rated supply voltage conditions

age is generated by using a PI controller, whose input is the difference between actual speed and desired speed. The reference DC voltage so obtained is given as input to the inner voltage control loop (OCC).

– *Inner DC bus voltage control loop*: The one-cycle controller processes reference dc voltage and actual DC voltage to generate the required gating signals for bridgeless SEPIC. The OCC integrates the actual DC voltage. Whenever the integrator output and reference DC voltage match exactly, the switch is turned OFF and the integrator is reset.

3.1 Electronic Commutation Switching Logic for VSI

The logic for switching pulses of the voltage source inverter corresponding to rotor position signals is as shown in Table 1.

Table 2 Steady-state performance of proposed BLDC drive with PAM control at different speeds

N^*(rpm)	N(rpm)	V_{dc}^*(V)	V_{dc}(V)	I_s(A)	%THD		PF	
					OCC	PI	OCC	PI
300	300	72.5	72.5	0.6266	5.79	6.13	0.9951	0.9950
600	600	98.2	98.2	0.8287	5.26	5.27	0.9978	0.9965
900	900	124.5	124.5	1.0330	4.39	4.67	0.9986	0.9973
1200	1200	150.5	150.5	1.2395	4.26	4.28	0.9991	0.9989
1500	1500	176.8	176.8	1.4495	4.00	4.07	0.9992	0.9991
1800	1800	203	203	1.6630	3.42	3.80	0.9995	0.9992
2100	2100	230	230	1.879	3.22	3.62	0.9995	0.9994
2400	2400	257	257	2.0986	3.01	3.49	0.9994	0.9993
2700	2700	283	283	2.32	2.96	3.38	0.9992	0.9992
3000	3000	310	310	2.547	2.81	3.29	0.9992	0.9990

The switch-on and switch-off conditions of the switches are described as '1' or '0', respectively. From Fig. 6, the voltage of the phase 'a' of three-phase VSI, with respect to the point 'n', is given as:

$V_{an} = V_{dc}/2$ for $S_1 = 1$
$V_{an} = -V_{dc}/2$ for $S_2 = 1$
$V_{an} = 0$ for $S_1 = 0, S_2 = 0$

where '1' and '0' represent the 'on' and 'off' conditions of the switches, respectively.

Table 1 shows the voltages for the other two phases v_{bn}, v_{cn} of three-phase VSI and the corresponding switching pattern of other switches (i.e. S_3, S_4, S_5, S_6) obtained in a similar way.

3.2 Speed Loop with PI Controller for Generating Reference DC Bus Voltage

The speed control of BLDC motor is dependent on DC link voltage control, which in turn is obtained from the inner voltage control loop. In this work, the speed control is realised using dual-loop control, namely the inner voltage control loop and outer speed control loop.

The outer speed control loop consists of a PI controller, which is used to generate the reference DC voltage V_{dc}^* for the inner voltage control loop. This facilitates output voltage control of bridgeless SEPIC converter to achieve control of DC link voltage.

The outer loop has a comparator to produce the speed error N_e, by comparing actual speed N with reference speed N^*.

Speed error at kth instant is given by (20)

$$N_e(k) = N^* - N \tag{20}$$

This speed error is processed by PI controller, which generates reference voltage V_{dc}^* for the DC voltage controller as shown in (21)

$$V_{dc}^*(k) = V_{dc}^*(k-1) + k_p\{N_e(k) - N_e(k-1)\} + k_i N_e(k) \tag{21}$$

where k_p is proportional gain and k_i is integral gain of the speed PI controller.

3.3 One-Cycle Control Technique for DC Bus Voltage Control

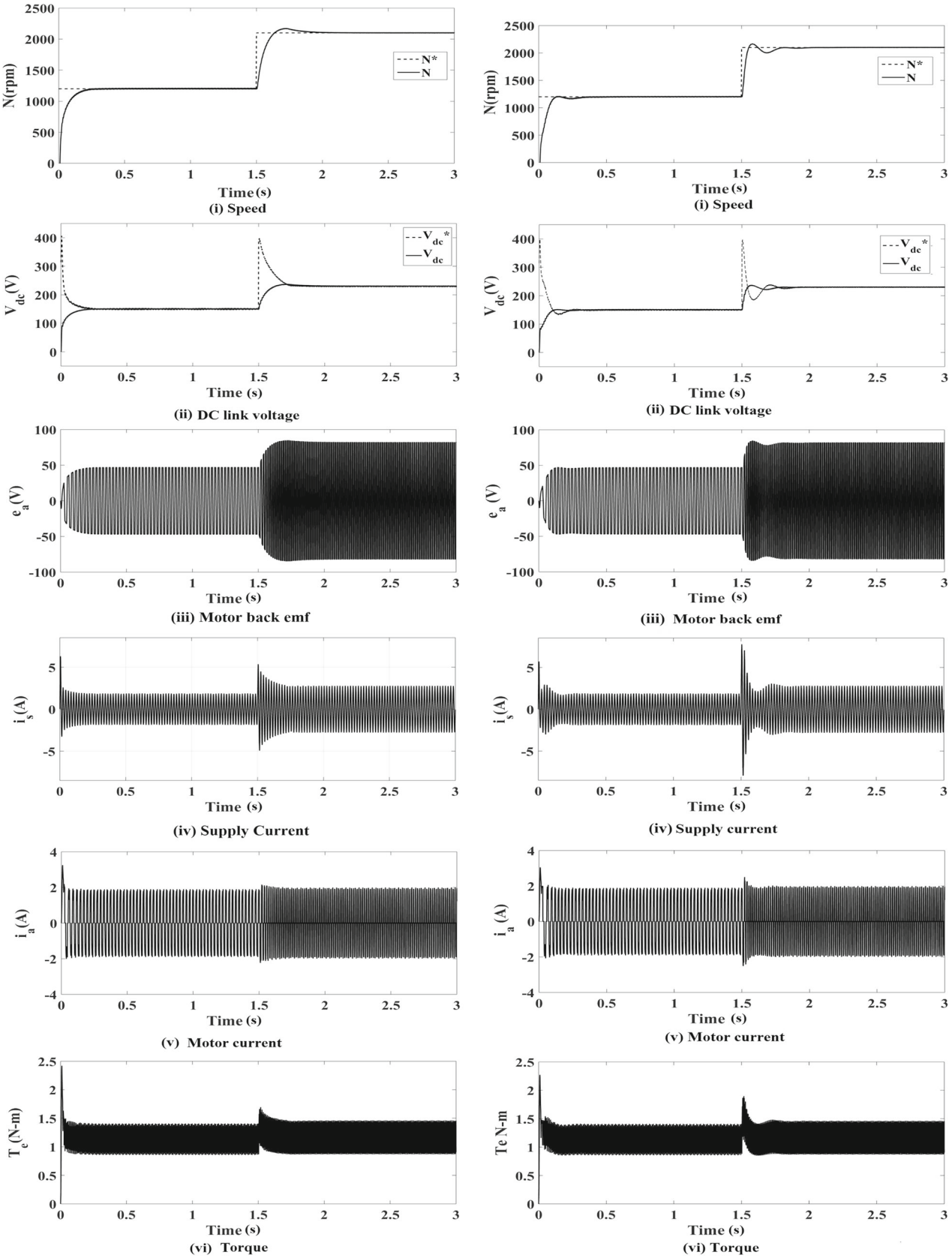
The inner loop voltage control to obtain DC bus voltage control is achieved by application of OCC technique to the bridgeless SEPIC.

The schematic diagram for implementation of one-cycle control technique is illustrated in Fig. 7. The main components are resettable integrator, a comparator and a D-flip flop. A clock of constant frequency ($f_s = 1/T_s$) for flip flop determines turning ON of the switch. The integrator starts operating immediately when the switch is turned ON. The sensed output voltage from the SEPIC converter is fed to the integrator. The integrator output is given to comparator, which compares it with the reference signal V_{dc}^*. The instant at which the output from the integrator matches the reference voltage V_{dc}^*, a high pulse is produced by the comparator which resets the flip flop. Immediately, the switching device turns OFF and the integrator is reset. Thus, it helps in maintaining the average value of the actual voltage to be equal to the reference voltage.

The operation of the switch in each cycle is determined by the switching function $d(t)$ at a frequency $f_s = \frac{1}{T_s}$, as shown in (22)

$$d(t) = \begin{cases} 1 & 0 \le t \le T_{ON} \\ 0 & T_{ON} \le t \le T_s \end{cases} \tag{22}$$

In this work, the $x(t)$ marked in Fig. 7 represents the input DC voltage $v_{in}(t)$ of the SEPIC converter and the output $y(t)$ represents the output voltage $V_{dc}(t)$ of SEPIC converter.



(a) Performance of the drive with One Cycle Control **(b)** Performance of the drive with PI Control

Fig. 9 Dynamic performance of the BLDC drive with PAM-control for step change in reference speed

Table 3 Control performance assessment indices

Performance index	$N = 3000$ rpm		$N = 2100$ rpm		$N = 1200$ rpm	
	OCC	PI	OCC	PI	OCC	PI
ISE	0.04129	0.04783	0.0348	0.0359	0.02162	0.02631
IAE	0.08384	0.101	0.07913	0.0828	0.06182	0.06569
ITSE	0.001828	0.003486	0.0015	0.0024	0.0007685	0.0009227
ITAE	0.01011	0.01454	0.01034	0.0192	0.01275	0.01431

Assuming the input to the switching converter as $x(t)$, the signal transmitted to the output of the converter is given by (23)

$$\begin{aligned} y(t) &= x(t) * d(t) \\ \text{i.e.} y(t) &= \frac{1}{T_s}\int_0^{T_{\text{ON}}} x(t)\mathrm{d}t \end{aligned} \tag{23}$$

If the duty ratio of the switch is adjusted such that integration of the output voltage over a switching cycle is exactly equal to the integration of the reference voltage as shown in (24)

$$\int_0^{T_{\text{ON}}} x(t)\mathrm{d}t = \int_0^{T_s} V_{\text{dc}}^*(t), \tag{24}$$

then the mean of the switch voltage becomes equal to the mean value of reference voltage in each cycle, as given in (25)

$$\begin{aligned} y(t) &= \frac{1}{T_s}\int_0^{T_{\text{ON}}} x(t)\mathrm{d}t = \frac{1}{T_s}\int_0^{T_s} v_{\text{ref}}(t) = V_{\text{dc}}^*(t) \\ y(t) &= \frac{1}{T_s}\int_0^{dT_s} x(t)\mathrm{d}t = V_{\text{dc}}^*(t) \end{aligned} \tag{25}$$

This operation is repeated for every switching cycle, and the output voltage is controlled to be equal to the reference voltage.

4 Results and Discussions

BLDC motor rated for speed of 3000 rpm, with rated power of 375 W and rated torque of 1.2 Nm, has been used in the proposed BLDC drive. The design of bridgeless SEPIC with coupled inductors is done for rated power of 500 W. The Simulink model of the proposed BLDC drive is developed and is tested for speed control performance under rated load torque and rated supply voltage (220 V) conditions. Performance of the drive is analysed for OCC and compared with conventional PI control technique.

4.1 Performance Comparison of Proposed BLDC Drive with PAM Control During Starting

Dual-loop control is used with an outer speed control loop and inner voltage control loop. PI controller is used in the outer speed control loop. The inner voltage control is implemented using PI and also OCC. The inner voltage control loop has faster response compared to the outer speed control loop. So the PI controller in inner voltage loop has to be tuned first. The MATLAB/Simulink auto-tuning algorithm is used to obtain the PI controller parameters for the inner voltage control loop. The output voltage to control transfer function $\frac{v_o(t)}{d(t)}$ of pulse-width modulated SEPIC in DCM is obtained as described in [35]. This linearised plant model is utilised in the controller design using auto-tuning method in MATLAB software. The controller is tuned such that, it gives optimal performance in terms of its response to a step voltage input. Also, THD of the supply current is checked to be within the specified limits given by IEC-61000-3-2. Similar procedure is adopted for tuning the outer speed control loop considering the speed to dc link voltage transfer function $\frac{N(t)}{V_{\text{dc}}(t)}$.

The PI controller in the speed control loop (outer loop) is designed to obtain a speed response with peak overshoot of 5.6% settling time of 0.6 s. The performance of BLDC drive is evaluated for one-cycle control and PI control in the DC bus voltage control loop (inner loop). Achievement of better transient state performance of the BLDC drive with one-cycle control in the inner loop is discussed.

Figure 8 shows the comparison of speed control performance of the drive with one-cycle control and PI control techniques for speed reference set to rated value of 3000 rpm, under rated supply voltage and load torque conditions.

Figure 8a shows the performance waveforms of (i) speed (N), (ii) DC link voltage (V_{dc}), (iii) supply current (i_{s}) and (iv) switch current (i_{sw1}) for PAM-BLDC drive with one-cycle control technique, and Fig. 8b depicts the respective performance waveforms of PAM-BLDC drive with PI control technique.

From Fig. 8, it can be seen that PI controller (Fig. 8b) has more oscillatory transients at the starting compared to one-cycle controller (Fig. 8a). It is evident from the speed response waveform (i) of Fig. 8b and this gets reflected in

the inner voltage control loop as depicted by DC link voltage waveform (ii). Further, the supply current shown in waveform (iii) of Fig. 8b and a has larger peak overshoot of 2.8 times the rated current with PI controller, and 1.5 times the rated value with one-cycle controller, respectively. Because of this, the current stress on switching devices is more in case of PI controller as shown in waveform (iv) of Fig.8b. One-cycle controller results in low stress on switching devices and similarly on other components of the circuit such as inductors and capacitors. Hence, the ratings of components of PAM-BLDC drive get reduced with one-cycle controller.

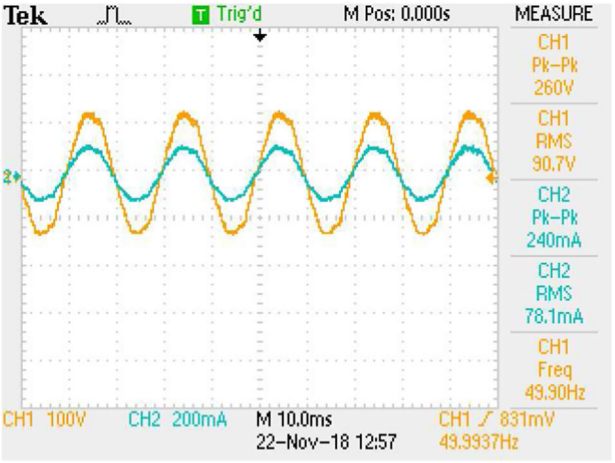
4.2 Performance Comparison of Proposed BLDC Drive with PAM Control at Steady State for Different Speeds

Comparison based on power quality indices like power factor and % THD is done at different speeds under steady state for the PAM-BLDC drive using one-cycle control and PI control techniques. The supply voltage and load torque are maintained at rated values. Speed reference is changed and performance is analysed; power quality indices are tabulated in Table 2 for different speeds. Inherent power factor correction with voltage mode control of bridgeless SEPIC with coupled inductors is evident from the results for the entire range of speed control (300–3000 rpm). One-cycle control enhances the performance of the system compared to the PI controller in regard to reduction in % THD of supply current and improvement in power factor.

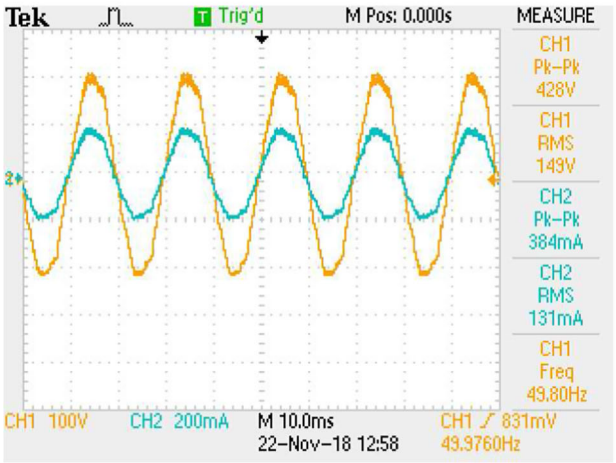
4.3 Performance Comparison of Proposed BLDC Drive with PAM Control for Dynamic Step Change in Reference Speed

The dynamic performance of proposed BLDC drive with PAM control is evaluated for a step change in the reference speed. This is achieved by giving a step change in the reference speed from 1200 to 2100 rpm at the time of 1.5 s, at rated torque and supply voltage conditions as shown in Fig. 9. Figure 9a presents the performance waveforms of (i) speed (N), (ii) DC link voltage (V_{dc}), (iii) motor back emf (e_a), (iv) supply current (i_s), (v) motor phase current (i_a) and (vi) motor torque (T_e) for PAM-BLDC drive with one-cycle control technique, and Fig. 9b shows the respective performance waveforms of PAM-BLDC drive with PI control technique for step change in speed.

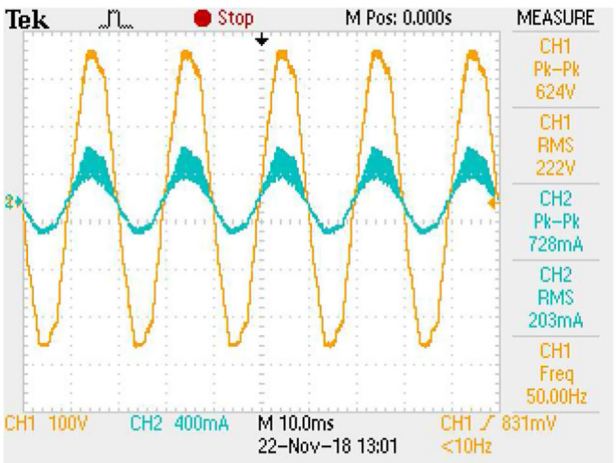
BLDC drive with PI controller has comparatively higher dynamic transient oscillations in the speed response at the step change instant of 1.5 s, as shown in waveform (i) of Fig. 9b. The change in DC bus voltage from 150 V to 230 V, corresponding to step change in speed reference from 1200 rpm to 2100 rpm, respectively, can be seen in the DC link voltage waveform (ii) of Fig. 9a and b. The larger transient oscillations in the DC link voltage of PI-controlled BLDC drive result in higher transients in the back emf as shown in waveform (iii) of Fig. 9b. The supply current waveform



(a) At supply voltage of 90 V

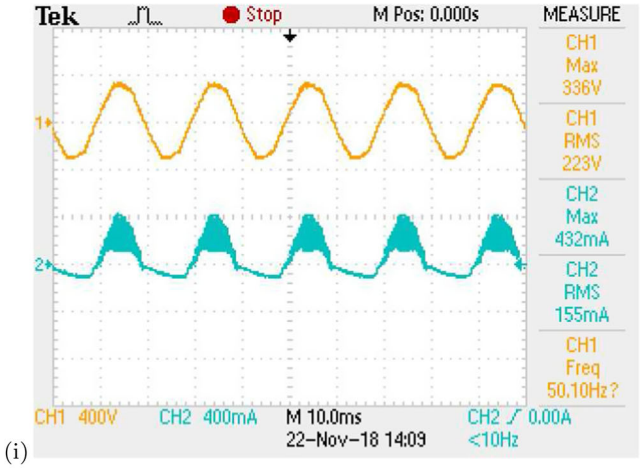


(b) At supply voltage of 150 V

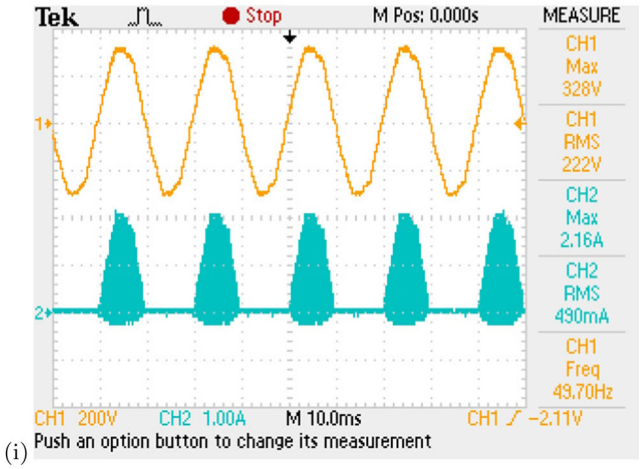


(c) At supply voltage of 220 V

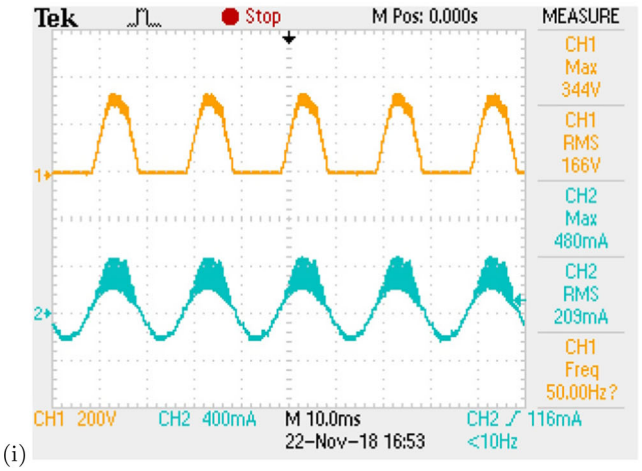
Fig. 10 Inherent power factor correction



(a) Input side inductor currents



(b) Output side inductor currents



(c) Intermediate Capacitor Voltages

Fig. 11 Bridgeless operation at supply voltage of 220 V

(iv) of Fig. 9b shows that the BLDC drive with PI controller has larger overshoot of 2.8 times the steady-state value at the instant of step change. The supply current transient at the step change effects in the motor current overshoot at step change instant which is shown in waveform (v) of Fig. 9b. This causes higher torque overshoot for the BLDC drive with PI control

as shown in waveform (vi) of Fig. 9b. Overall analysis shows the better performance by BLDC drive with one-cycle control for dynamic step change in reference speed.

4.4 Control Performance Assessment

The control performance for step response can be analysed using the significant performance indices like integral absolute error (IAE), integral square error (ISE), integral time absolute error (ITAE) and integral time square error (ITSE) per unit basis, where

integral absolute error is given by (26)

$$\mathrm{IAE} = \int |e| \mathrm{d}t \tag{26}$$

integral square error is given by (27)

$$\mathrm{ISE} = \int e^2 \mathrm{d}t \tag{27}$$

integral time absolute error is given by (28)

$$\mathrm{ITAE} = \int t|e| \mathrm{d}t \tag{28}$$

integral time square error is given by (29)

$$\mathrm{ITSE} = \int te^2 \mathrm{d}t \tag{29}$$

Control performance assessment indices is given in Table 3. The results are tabulated for reference speeds of 3000 rpm, 2100 rpm and 1200 rpm. It can be seen from Table 3 that the one-cycle control displays the improved values of performance indices compared to PI control, indicating the enhanced control performance.

4.5 Experimental Results

Experimental prototype for bridgeless SEPIC with coupled inductors rated power of 500 W is implemented. The self-inductance value for the proposed converter is reduced significantly compared to separate inductor converter. The input and output side inductors of individual (positive and negative half cycle) SEPIC converter are wound on single core with windings of reduced number of turns. This reduces cost and size of the SEPIC converter and hence the overall system.

The experiment is conducted in open loop for the different supply voltages of 90 V, 150 V and 220 V with a fixed resistive load. The results are shown in Fig. 10. It can be seen that bridgeless SEPIC with coupled inductors efficiently exhibits inherent power factor correction feature for universal supply voltage variations. The supply current in phase with supply voltage is shown in Fig. 10a, b and c for supply voltages of 90 V, 150 V and 220 V, respectively.

The designed coupled inductor configuration of SEPIC operates successfully in bridgeless topology as shown in Fig. 11. The part (i) of Fig. 11a, b and c depicts waveforms for current through input side inductor, current through output side inductor and the voltage across intermediate capacitor of SEPIC converter operating in positive half cycle of supply voltage. Similarly, the part (ii) of Fig. 11a, b and c shows the corresponding waveforms of SEPIC converter operation during negative half cycle for the supply voltage of 220 V.

5 Conclusion

One-cycle controlled bridgeless SEPIC embedded with coupled inductors is presented for BLDC drive using PAM control of VSI for a residential air conditioning application. The proposed bridgeless SEPIC converter employs lower self-inductance when compared to conventional bridgeless SEPIC topology by adopting coupled inductors in the structure. Hence, two inductor windings of converter with less number of turns, wound on a same core, result in reduction of size and cost. One-cycle control for controlling DC bus voltage enhances the performance of the BLDC drive compared to PI controller. The evaluation of power factor and THD at steady state shows better performance by one-cycle control with improved power factor and reduced source current THD over a wide speed range. The oscillatory transients in the speed response with PI controller at startup are reduced using one-cycle controller. This lowers the supply current overshoot and thereby reduces the stress on the switch. Dynamic response of the BLDC drive for the step change in reference speed is also better with one-cycle controller compared to PI controller. A lower supply current and reduced torque overshoot is observed at the instant of step change with the one-cycle controller. The control performance is assessed using IAE, ISE, ITAE and ITSE indices. Improved values of indices are obtained with one-cycle controller, for different speeds. Hence, OCC ensures the better performance of BLDC drive by improving the transient state. Experimental results are obtained to validate bridgeless operation of the proposed coupled inductor configuration for the SEPIC. The results obtained also show the inherent capability of DCM SEPIC to obtain the unity power factor for the variations in line voltage.

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