Dual Role CDSC-Based Dual Vector Control for Effective Operation of DVR With Harmonic Mitigation

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***Abstract*—For the effective operation of a dynamic voltage restorer (DVR), a control strategy plays a significant role. This paper presents an enhanced control strategy for DVR using dual role cascaded delay signal cancellation (CDSC)-based dual vector control (DVC) under unbalanced and distorted grid conditions. Based on the numerical analysis, it is found that the CDSC prefilter is a promising solution when grid voltage is distorted by symmetric, asymmetric harmonics, and unbalanced sag. Mainly, the CDSC prefilter extracts instantaneous symmetrical components of the grid voltage required for voltage sags detection and generation of fundamental component of reference voltage for the DVR. A CDSC-based DVC algorithm with inductor current and capacitor voltage feedback is implemented in a synchronous reference frame, which tracks the fundamental DVR reference voltages. An extractor based on the modified CDSC strategy is designed to extract harmonics from load voltage during distorted grid conditions. These extracted harmonic components (nonfundamental) are added in phase opposition with fundamental component and fed to pulse width modulation block to generate reference voltages. Experimental studies are conducted on scaled down (100 V, 0.5 kVA) laboratory prototype DVR to verify the effectiveness of the proposed control algorithm under unbalanced and distorted grid conditions.**

***Index Terms*—Cascaded delay signal cancellation (CDSC), double vector control, extractor, harmonics, medium-voltage dynamic voltage restorer (DVR), prefilter, symmetric and asymmetric voltage sags.**

Manuscript received October 26, 2017; revised February 1, 2018 and March 2, 2018; accepted April 2, 2018. Date of publication April 24, 2018; date of current version August 31, 2018. This work was supported in part by the administration of National Institute of Technology Karnataka, Surathkal, and in part by the Department of Science and Technology, India, under project Grant SB/FTB/ETA-0020/2014. *(Corresponding author: Anbalagan Karthikeyan.)*

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Digital Object Identifier 10.1109/TIE.2018.2829678

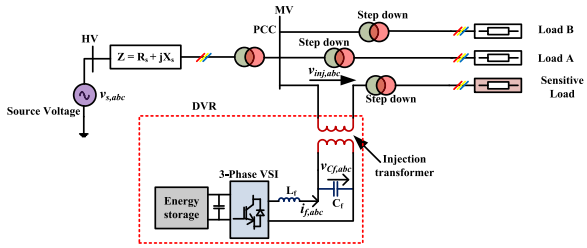

Fig. 1. Dynamic voltage restorer.

I. Introduction

POWER quality (PQ) has become a serious concern with deregulation of energy markets and increased use of power electronics-based loads. These types of loads are nonlinear in nature and its abundant usage results in injection of harmonics into the system thereby declining quality of power. To address these PQ issues, viz., voltage sags, swell, and harmonics, a dynamic voltage restorer (DVR) has been proposed [1], [2] as shown in Fig. 1. For effective utilization of the DVR, two major aspects play a significant role: reference generation and control. Reference generation algorithms based on synchronous reference frame (SRF) theory usually employ SRF-phase locked loop (PLL) for this purpose. The presence of negative sequence components and harmonics in grid voltage leads to sustained oscillations in the *dq*-voltages computed by a conventional SRF-PLL. PLLs are proposed in the literature with different in-loop and prefiltering techniques to eliminate these oscillations. However, for DVR application, moving average filter (MAF)-PLL [4], delayed signal cancellation (DSC)-PLL [5], and least error squares (LES) filter-based PLL [6], [7] are proposed for extraction of instantaneous symmetrical components (ISC) of the grid voltage. Even though MAF-PLL eliminates all even- and odd-order harmonics, it takes one cycle to block these harmonics [8]. The complexity of LES-PLL increases with the number of harmonics present in the grid voltage. DSC-PLL proposed in the literature is not effective when the grid voltage contains asymmetric odd-order harmonics (+5, –7 . . .), even though it can filter the fundamental negative sequence voltages and symmetric odd order harmonics (–5, +7 . . .). Hence, the *dq*-voltages of the grid v_{dq} estimated by DSC-PLL contains an oscillating

component which makes it difficult to enable and disable DVR. Double second-order generalized integrator (DSOGI)-PLL [9] can filter out these harmonics but it offers a tradeoff between speed and its filtering ability. Cascaded delay signal cancellation (CDSC)-PLL extends the concept of DSC by cascading multiple delay operators to eliminate both asymmetric odd- and even-order harmonics [10]–[12]. Unlike other filters, the CDSC filter can be customized by cascading different delay operators to eliminate specific group of harmonics and thus offers flexibility to eliminate harmonics of interest without effecting (compromising its dynamic response) its speed [14]. Also the CDSC operator can be placed as either a prefilter or in-loop filter. In this paper, $\text{CDSC}_{4,8,16,32}$ prefilter is implemented by cascading multiple delay operators DSC4, DSC8, DSC16, DSC32 to eliminate symmetric and asymmetric odd harmonics and separate the ISC of the grid voltage. In order to inject desired compensating voltage, the DVR should be operated by using a proper control strategy.

Several control methods have been proposed in the literature for the control of DVR [14]–[26]. Multiple reference frame-based controllers [23] with resonant filter, improved SRF controller with high-pass filter for harmonic elimination [24] are also proposed in the literature, but these algorithms are complex as they involve multiple reference frame transformations. Double vector control algorithm with resonant controllers [25] is proposed in the literature to improve the transient response of DVR and eliminate harmonics from load voltage, respectively. Though this scheme was tested for voltage harmonics, but for unbalanced voltage sags, the validation of this scheme is not shown. Modified double vector control is proposed in [5] to compensate for both balanced and unbalanced dips. Even though the grid voltage distortions were considered previously in the literature, no clear classification of symmetric and asymmetric voltage harmonics is defined, and no separate tests were carried out. These symmetric and asymmetric voltage harmonics become relevant if there is spike in the grid-connected single phase nonlinear loads. In this paper, a dual role CDSC-based dual vector control (DVC) is presented for DVR control and harmonics mitigation. The compensation voltage injected by DVR includes both fundamental and nonfundamental component. The proposed dual role CDSC has a feature of generating both components simultaneously. First, the prefilter extracts ISC of grid voltage and is given to the controller to generate fundamental component. Apart from that, to achieve the harmonic mitigation of load voltages, an extractor based on the modified CDSC strategy is designed which generates nonfundamental component of compensation voltage and added in 180° phase opposition to the DVC algorithm. Thereby, this paper eliminates the use of additional controllers for harmonic compensation such as resonant controllers proposed in the literature, because the single CDSC operator is performing the dual role as a prefilter and extractor. In this application, many authors have addressed the harmonic compensation during unbalanced grid conditions but here an attempt is made to classify harmonics into symmetric, asymmetric, and its compensation is achieved during distorted grid conditions.

The paper is organized as follows. Section II starts with the brief introduction of various harmonics that occur in grid voltage. Then, the role of CDSC as a prefilter and extractor is explained with respective mathematical equations and the frequency response of CDSC-PLL, DSOGI-PLL, DSC-PLL, and SRF-PLL under distorted grid conditions is studied. In Section III, the proposed CDSC-based DVC control scheme is discussed. In Section IV, the EMTDC/PSCAD simulation results of medium-voltage DVR for asymmetric and symmetric harmonics cases are presented. In Section V, experimental results of the proposed algorithm for different test cases are portrayed. Finally, conclusion is given in Section VI.

II. Proposed Dual Role CDSC

Usually the harmonic spectrum of grid voltage in a distribution system is dominated by the lower order odd harmonics because of nonlinear loads which are often connected to the grid. These harmonics of order h = –5, + 7 . . . etc., are termed as symmetric harmonics. But with the steep rise in the usage of single-phase nonlinear load causes unbalance and thereby leads to the occurrence of asymmetric harmonics of order h = +5, –7 . . . etc., along with triplen harmonics. In this case, if any grid disturbances occur, say voltage sag, then it affects the DVR control algorithm in detecting the sag and thereby chances of maloperation. Thus, an effective filter is necessary to eliminate these harmonics (h = +5, + 7. . .). In this paper, CDSC-based prefilter is adopted which extracts ISC of the grid voltage required for voltage sags detection and for the generation of fundamental component of reference voltage for DVR. Furthermore, when grid voltages are harmonically distorted and to regulate the load voltage harmonics, an extractor is designed based on the modified CDSC strategy. This extractor generates the nonfundamental component of reference voltage and is added in 180° phase opposition to fundamental component (from prefilter and controller). The following part of the section deals with the concept of the proposed dual role CDSC operator.

A. CDSC Prefilter

The harmonics present in the grid voltage retain their periodic nature even when they are transformed to SRF. DSC technique exploits this property so that it is possible to eliminate harmonic signal by summing it with half-cycle delayed version. The mathematical model of the DSC operator in the *dq* frame is given in (1), where *n* is a delay operator which delays signal by *T/n*. Single DSC operator is not able to eliminate all the harmonics, so multiple DSC operators are cascaded to form the CDSC operator, which accomplished the elimination process step-by-step. In this paper, the CDSC operator is implemented in the $\alpha\beta$ frame

$$dq\text{DSC}_n\left[v(t)\right] = \frac{1}{2}\left[v(t) + v(t - T/n)\right] \tag{1}$$

$$v_{dq}(t) = e^{-j\theta'}(v_{\alpha\beta}) \tag{2}$$

$$\text{v}_{dq}(t - T/n) = e^{-j(\theta - \frac{2\pi}{n})}(v_{\alpha\beta}). \tag{3}$$

By substituting (2) and (3) in (1), the DSC operator in the $\alpha\beta$ frame is given in the following equation:

$$\alpha\beta\text{DSC}_n\left(v_{\alpha\beta}(t)\right) = \frac{1}{2}\left[v_{\alpha\beta}(t) + e^{j\frac{2\pi}{n}}v_{\alpha\beta}(t - T/n)\right]. \tag{4}$$

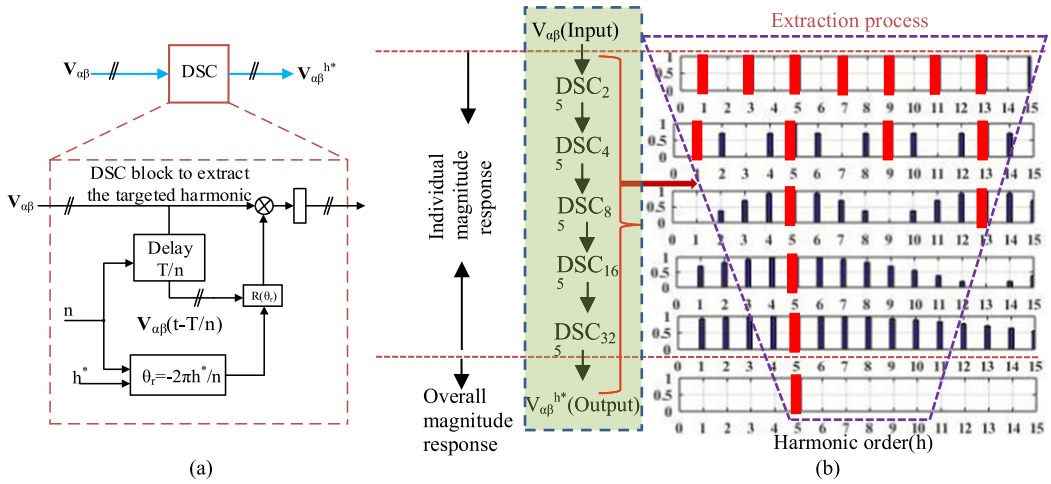

Fig. 2. Dual role CDSC. (a) Extractor. (b) Individual and overall magnitude response of CDSC^5 operator.

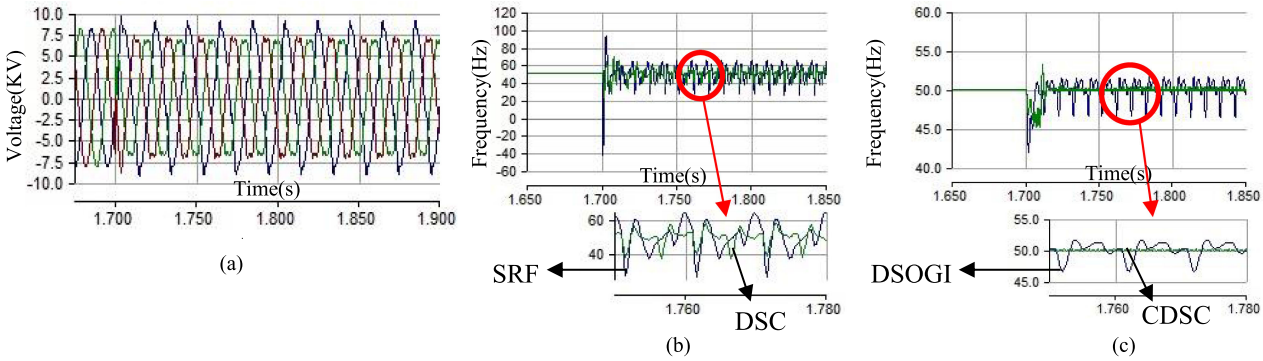

Fig. 3. Simulation results for asymmetric harmonics with 20% sag in two phases. (a) Source voltage. (b) Frequency response of SRF-PLL and DSC-PLL. (c) Frequency response of DSOGI-PLL and CDSC-PLL.

Delay operators $n = 2, 4, 8, 16, 32$ can eliminate all harmonics with $h = 0, \pm1, \pm2, \pm3, \pm4 \ldots \pm 30$ in the $\alpha\beta$ frame, i.e., the dc offset, all symmetrical and asymmetrical harmonics up to $h = \pm30$. But DSC_2 operator is used to filter out the even-order harmonics which are very small. Thus, in this paper, only DSC_4, DSC_8, DSC_{16}, DSC_{32} are cascaded to form $\text{CDSC}_{4,8,16,32}$ prefilter. Positive sequence voltages after application of a DSC_n operator are given in the following equation:

$$\begin{bmatrix} v^+_{\alpha n} \\ v^+_{\beta n} \end{bmatrix} = \begin{bmatrix} v_\alpha + v_\alpha\left(t-\frac{T}{n}\right)\cos\left(\frac{2\pi}{n}\right) + v_\beta\left(t-\frac{T}{n}\right)\sin\left(\frac{2\pi}{n}\right) \\ v_\beta + v_\beta\left(t-\frac{T}{n}\right)\cos\left(\frac{2\pi}{n}\right) - v_\alpha\left(t-\frac{T}{n}\right)\sin\left(\frac{2\pi}{n}\right) \end{bmatrix}. \quad (5)$$

B. Modified CDSC Extractor

The concept of harmonic extraction is based on harmonic gain, i.e., a zero gain of a DSC on a harmonic signal means the DSC can eliminate the harmonic signal and on the other side unity gain means the harmonic can pass through without attenuation. The modified CDSC extractor can eliminate the fundamental positive sequence signal as well to achieve the target harmonic extraction. The CDSC extractor is constructed as follows:

$$\text{DSC}_n\left[v_{\alpha\beta}(t)\right] = \frac{1}{2}\left[v_{\alpha\beta}(t) + R(\theta_r).v_{\alpha\beta}(t-T/n)\right] \quad (6)$$

where $R(\theta_r)$ is given as $\left[\begin{smallmatrix} \cos\theta_r & \sin\theta_r \\ -\sin\theta_r & \cos\theta_r \end{smallmatrix}\right]$ and rotation angle $\theta_r = -2\pi h^*/n$. Fig. 2(a) depicts the block diagram of (6).

For illustration purpose, let us consider a typical harmonic scenario, where the voltage source consists of $h = -1, \pm3, 5, \pm7, 9, \pm11, 17, \pm19 \ldots \pm 30$. Let the target harmonic to be extracted is $h^* = 5$, then the extractor should eliminate $h = \pm3, \pm7, 9, \pm11, 17, \pm19 \ldots \pm30$. To achieve this, five DSC blocks of $n = 2$ (even-order harmonics and dc components), $n = 4$(–29, –25, –21, –17, –13, –9, –5, –1, 3, 7, 11, 15, 19, 23, 27, 31), $n = 8$(–39, – 31, – 23, – 15, – 7, 1, 9, 17, 25, 33, 41) $n = 16$(–19, – 3, 13, 29), and $n = 32$(–11, 21) are cascaded to form the $\text{CDSC}^5_{2,4,8,16,32}$ extractor. Fig. 2(b) depicts that the constructed $\text{CDSC}^5_{2,4,8,16,32}$ operator eliminates all undesired harmonics by providing zero gain and extracts the fifth harmonic component by providing unity gain.

C. Asymmetric Harmonics

A dynamic model has been implemented in PSCAD in order to simulate the operation of different PLL's, i.e.,

CDSC-PLL, DSOGI-PLL, DSC-PLL, and SRF-PLL, and the results are presented in Fig. 3 under two-phase sag with asymmetric grid voltage harmonics. The operation of the aforementioned PLL's is demonstrated in Fig. 3(a)–(c), where it is noticed that the time taken to detect frequency and phase angle is different for all PLL's. The moment when sag is created, Fig. 3(b) shows that both SRF-PLL and DSC-PLL have an undershoot of more than 75%, respectively. The time taken by DSC-PLL to reach the tolerance band is 5 ms but SRF-PLL oscillates above the tolerance band. Similarly, Fig. 3(c) depicts DSOGI-PLL and CDSC-PLL, though both PLL's take less time to reach the tolerance band but possess an undershoot of 16% and 8%, respectively. Therefore, CDSC-PLL is the preferable solution as it is operating accurately during asymmetric voltage sags.

There are some considerations for the practical (digital) implementation of CDSC operator. Ideally, the delay time (*T/n*) of DSC should correspond to an integer number of delay samples ($N_n = N/n$) but in practical scenario N_n is hardly an integer. So, N_n should be rounded by taking the floor ($N_{nf} = \text{floor}(N_n)$) or the ceiling ($N_{nc} = \text{ceil}(N_n)$). The resulted delay buffer size becomes imprecise, and thereby causes small discretization error in the operation of DSC. Such error usually has limited effect (for small frequency variations, viz., nominal frequency (*f*) ± 0.3 and error $\approx 0.6\%$). However, if the system demands higher detection accuracy (if the aforementioned range exceeds), then the CDSC technique can be further improved by adopting the linear interpolation method [27]. In this paper, the results are focused on the mitigation of symmetric and asymmetric voltage sags and harmonics at constant frequency thus avoiding the discretization error (*N* corresponds to samples f_s (sampling frequency) /*f* (nominal frequency).

III. DVR Control

The schematic of dual role CDSC-based DVC algorithm for DVR is shown in Fig. 4. At first, the CDSC prefilter extracts ISC of the fundamental grid voltage in stationary frame. The extracted ISC is transformed to the *dq* frame and fed to the controller which generates fundamental component of compensation voltage. On the other hand, an extractor based on the modified CDSC strategy is designed which extracts the desired harmonic components from load voltages. The harmonic extraction block generates nonfundamental component of compensation voltage and added 180° phase opposition with fundamental component. Finally, the resultant is fed to pulsewidth modulation block to produce reference voltage for compensation. It has been considered that a sufficient battery energy storage system supports the real power required by the dc-link capacitor of DVR. The DVC implemented in this paper is a multiloop with a capacitor voltage and inductor current as feedback signals designed in the SRF. It consists of positive and negative sequence controllers (PSC and NSC) to compensate for balanced and unbalanced voltage sags. The voltage and current feedback loops of DVC employ proportional controllers to track the reference voltages accurately. Equations of the positive controllers are given in the following equations:

$$i^*_{Ldp} = i_{\text{load\_}dp} - \left(\frac{\omega c_f}{2}\right)\left(v^*_{cqp} + v_{cqp}\right) + K_u\left(v^*_{cdp} - v_{cdp}\right) \tag{7}$$

$$i^*_{Lqp} = i_{\text{load\_}qp} + \left(\frac{\omega c_f}{2}\right)\left(v^*_{cdp} + v_{cdp}\right) + K_u\left(v^*_{cqp} - v_{cqp}\right) \tag{8}$$

$$v^*_{iqp} = v^*_{cqp} + R_f i_{Lqp} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Ldp} + i_{Ldp}\right) + K_p\left(i^*_{Lqp} - i_{Lqp}\right) \tag{9}$$

$$v^*_{idp} = v^*_{cdp} + R_f i_{Ldp} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Lqp} + i_{Lqp}\right) + K_p\left(i^*_{Ldp} - i_{Ldp}\right) \tag{10}$$

where K_p and K_u are proportional gains of current and voltage loops, respectively, of the DVC. The PSC and NSC are shown in Fig. 4(a).

A. Design of Controller Parameters

The objective of tuning the controller is to find the coefficients of the proposed CDSC-based DVC controller. The DVC implemented in this paper is a multiloop with a capacitor voltage and inductor current as feedback signals designed in the SRF. It consists of PSC and NSC to compensate for balanced and unbalanced voltage sags. The voltage and current feedback loops of DVC employ proportional controllers to track the reference voltages accurately. Both PSC and NSC constitutes of eight controllers (four with respect to PSC and four with respect to NSC). In this section, the tuning of two controller gains K_v and K_c among the four controllers of PSC is discussed. K_v refers to the outer loop voltage controller gain, and K_c refers to the inner loop current controller gain (PSC). An extended root locus design (RLD) [28] method is adopted to tune the controller coefficients. Fig. 4(b) and (c) shows the extended RLD for tuning the coefficients of P controller. First, to tune the value of *Kc*, the root locus for K_c is drawn as shown in Fig. 4(c) for all the values of K_v varied stepwise from its minimum stable value to maximum stable value obtained by Routh Hurwitz stability criterion. Based on the maximum relative stability, the optimal value of K_c is obtained. From the obtained value of K_c [see Fig. 4(c)], the root locus is plotted for transfer function having gain K_v as shown in Fig. 4(b) and its value is calculated based on relative stability. To design the controller with high robustness, relative stability is considered for optimum tuning of controller parameters. It is essential that load voltage tracking accuracy should be sustained during voltage sags. Thus, the controller parameters are tuned to address all the above requirements. The same procedure is followed to tune the other controller gains.

IV. Simulation Results

A PSCAD/EMTDC model of a three-phase DVR with the proposed control scheme is built and its performance is validated

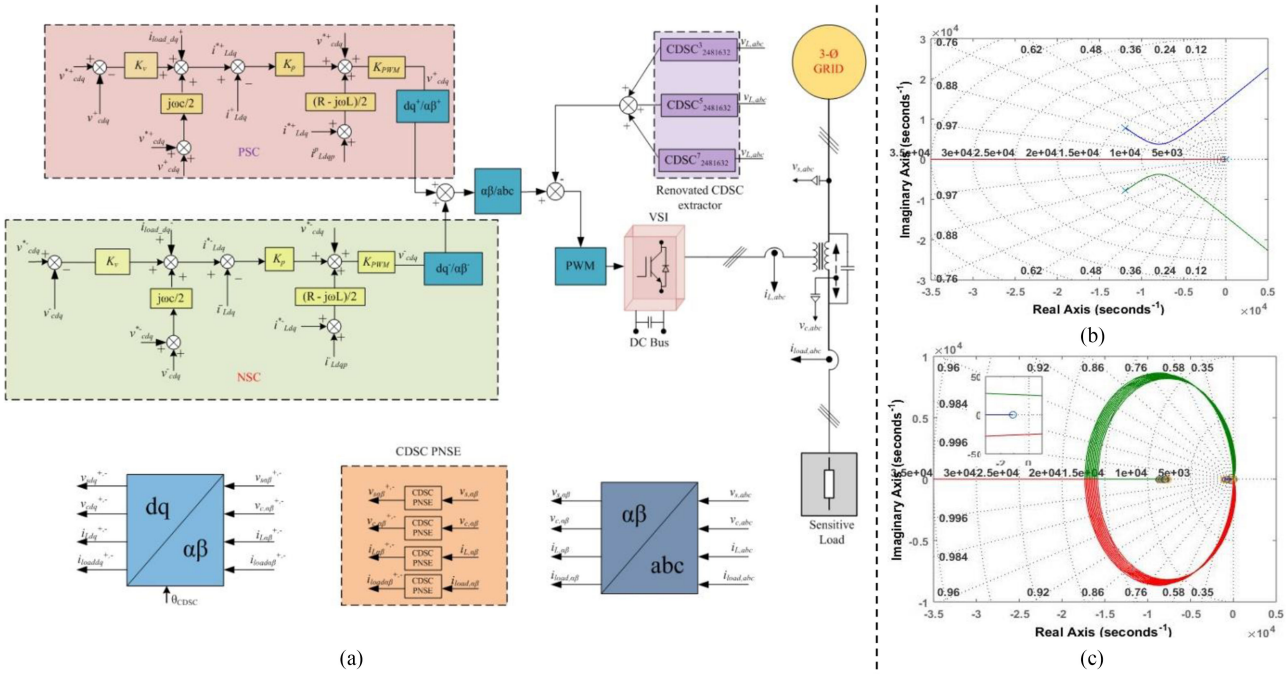

Fig. 4. Control scheme for DVR. (a) Block diagram. (b) and (c) Root loci of P controller.

for asymmetric and symmetric voltage sags and harmonics, but results are presented for harmonics case. The parameters of the 10 kV distribution system with DVR installed between the source and load which are considered for simulation studies are provided in the Appendix [3].

A. Performance of DVR Under Asymmetric and Symmetric Harmonics Condition

The use of single-phase nonlinear loads could generate asymmetric odd voltage harmonics such as $n = +5, -7 \ldots$. Hence, by connecting unbalanced nonlinear loads, asymmetric odd harmonics are generated at the PCC. Under such nonlinear loads, phase-a voltage contains third harmonic of 5.53%, fifth harmonic of 7.23% as shown in Fig. 5(e). Furthermore, the terminal voltages have a total harmonic distortion of 13.07%. Fig. 5(a) depicts the supply voltages with a two-phase voltage dip of 20%. CDSC prefilter extracts the ISC accurately even under asymmetric harmonics. Positive and negative sequence controllers compensate for the voltage sag and restore the fundamental of load voltage to nominal value as shown in Fig. 5(c). The effectiveness of the modified CDSC-based extractor under asymmetric harmonics can be verified from the load THD waveform from Fig. 5(e), where it is observed that the third and fifth harmonics are restricted to 0.99% and 1.45%, respectively. After harmonic compensation by dual role CDSC-based DVC, the load voltages have a THD of 3.7%. The DVR injected voltages are shown in Fig. 5(b) and the zoomed view of source, DVR injected, and load voltages are presented in Fig. 5(d). Fig. 5(f)–(j) shows the DVR performance during the presence of symmetric harmonics in source voltage. The THD waveform shows the efficacy of control algorithm where load voltage THD is reduced to 3.89% from source voltage THD of 21.4% as depicted in Fig. 5(j). Fig. 5(i) represents the zoomed part of source, DVR, and load voltages under symmetric harmonics case.

V. Experimental Results

A 100 V, 0.5 kVA scaled down DVR prototype is developed in the laboratory to conduct experimental studies. Hardware configuration of the DVR prototype consists of a SEMIKRON-made voltage source inverter (VSI), Fluke 435 PQ analyzer, and a resistive load as shown in Fig. 7(a). The dc link of the VSI is powered by an auxiliary supply as shown in Fig. 7(a). The control platform is based on Altera cyclone-II field programmable gate array (FPGA) controller using Quartus GUI. The FPGA board is interfaced with EEPROM (configuration device), physical interfacing devices, viz., ADC, DAC, Digital I/O's, USB device, and synchronous Dual-PORT SRAM (CY7C09389V). Analog signals are converted to digital form using 12-bit 4-channel bipolar ADCs(AD7864) and the signals are interfaced to FPGA. The scaling circuits provide necessary scaling of measured values to interface with the FPGA board. The system parameters are listed in Table II in the Appendix. The experimental studies are conducted for symmetrical and asymmetrical voltage sags, harmonics, respectively, and their results are presented.

A. Performance of CDSC-PLL Under Distorted Grid Conditions

In simulation studies, it is found that CDSC prefilter performs better during the distorted grid conditions. Hence, CDSC-PLL algorithm is implemented in the FPGA board. It is tested for two phase sag, symmetric and asymmetric grid voltage harmonics.

1) Performance of CDSC-PLL Under Two-Phase Sag: The CDSC-PLL algorithm is subjected to two-phase sag to test

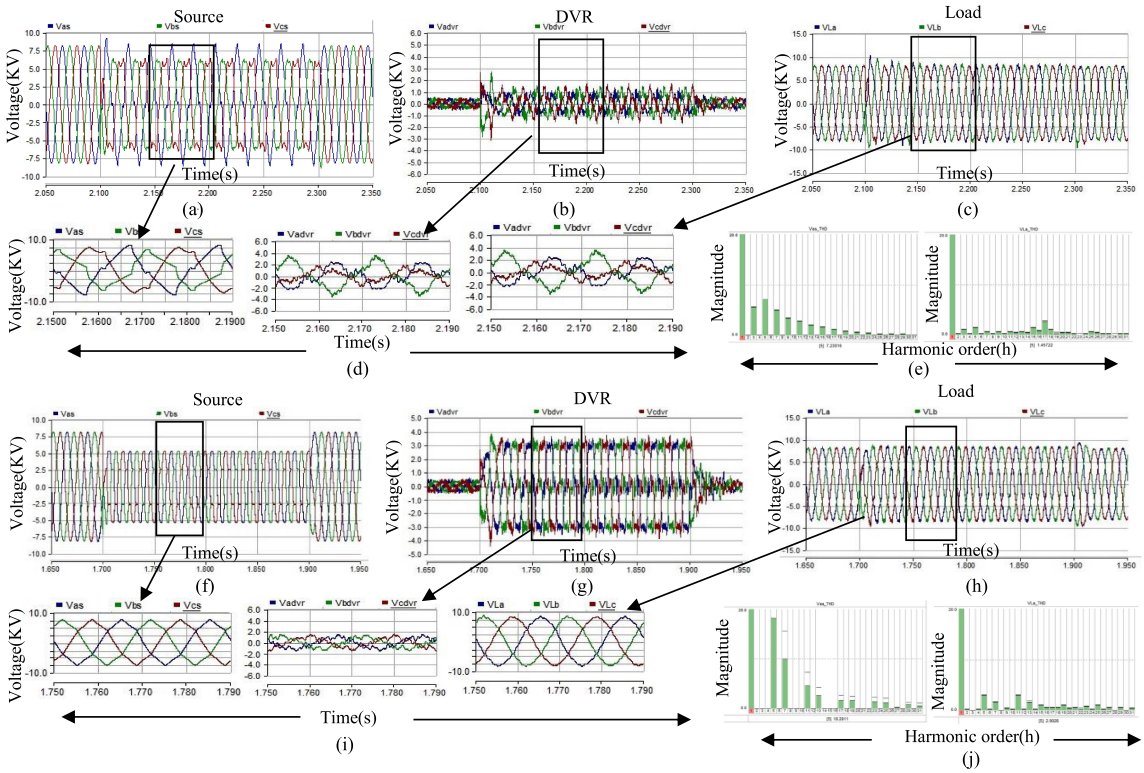

Fig. 5. Testing of DVR response during (a)–(c) two-phase sag with asymmetric odd order harmonics. (d) and (e) Zoomed view and harmonic spectra under asymmetric harmonics. (f)–(h) Three-phase balanced sag with symmetric odd order harmonics. (i) and (j) Zoomed view and harmonic spectra under symmetric harmonics.

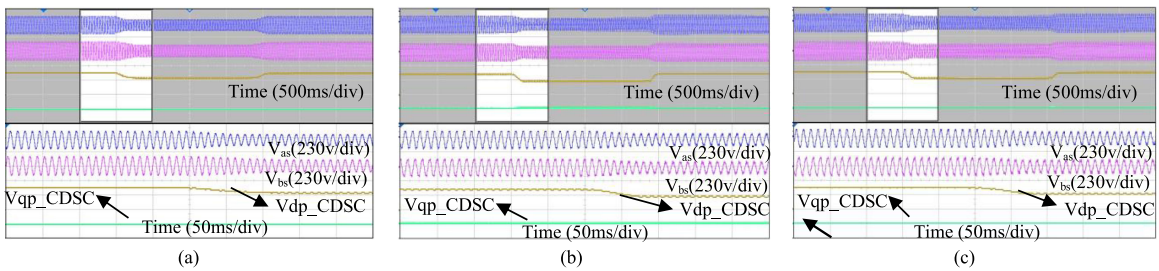

Fig. 6. Source voltages and its estimated dq_{sp}- voltages of CDSC-PLL under different test conditions. (a) Two-phase sag. (b) Balanced sag with symmetric harmonics. (c) Balanced sag under asymmetric harmonics.

its ability in eliminating negative sequence voltages. During sag condition, the negative sequence components present in the grid voltage leads to oscillating double frequency components in the *dq* frame but Fig. 6(a) shows that the CDSC prefilter cancels out the oscillating component to keep V_{sdq} ripple free.

2) Performance of CDSC-PLL Under Asymmetric and Symmetric harmonics: A balanced dip of 30% is generated in phase-a and phase-b of the supply voltage with symmetric and asymmetric harmonics, respectively. The absence of ripple in V_{sdq} of CDSC-PLL, shown in Fig. 6(b) and (c), indicates the effectiveness of its prefilter in eliminating harmonics.

B. Balanced Sag

The laboratory prototype DVR is connected to a load of 0.5 kW for the following experimental cases. A three-phase voltage dip of 30% is initiated by using a three-phase auto transformer for a duration of 840 ms, which can be observed from supply voltage waveform shown in Fig. 7(b) and (c). DVR mitigates the voltage sag and restores the load voltage to a constant value as shown in Fig. 7(d). DVR injected voltages can be observed in Fig. 7(b)

C. Two-Phase Sag

Three single-phase transformers are employed to create unbalanced voltage sag by reducing the voltage in phase-a and phase-b, respectively, by 30% as shown in Fig. 8(a) and (c). DVR compensates for both negative and positive sequence voltage and maintains a constant voltage waveform of phase-a and phase-b as depicted in Fig. 8(a) and (d). DVR injected voltages are shown in Fig. 8(a).

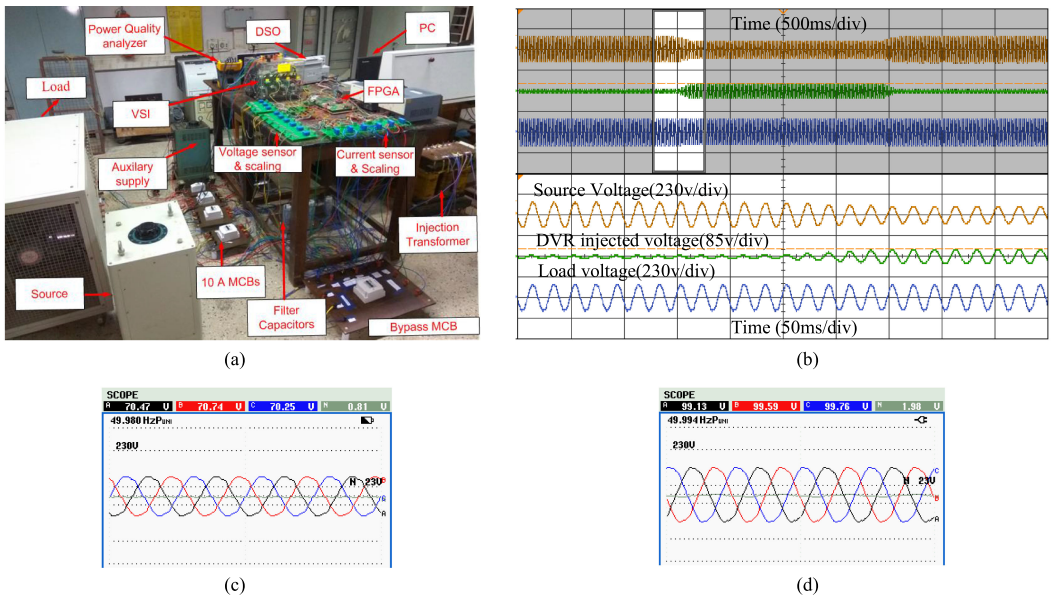

Fig. 7. Experimental results. (a) Experimental setup of laboratory prototype. (b) Dynamic response of DVR under symmetric sag (192 v/div). (c) and (d) Steady-state voltage waveform of source and load under symmetric sag.

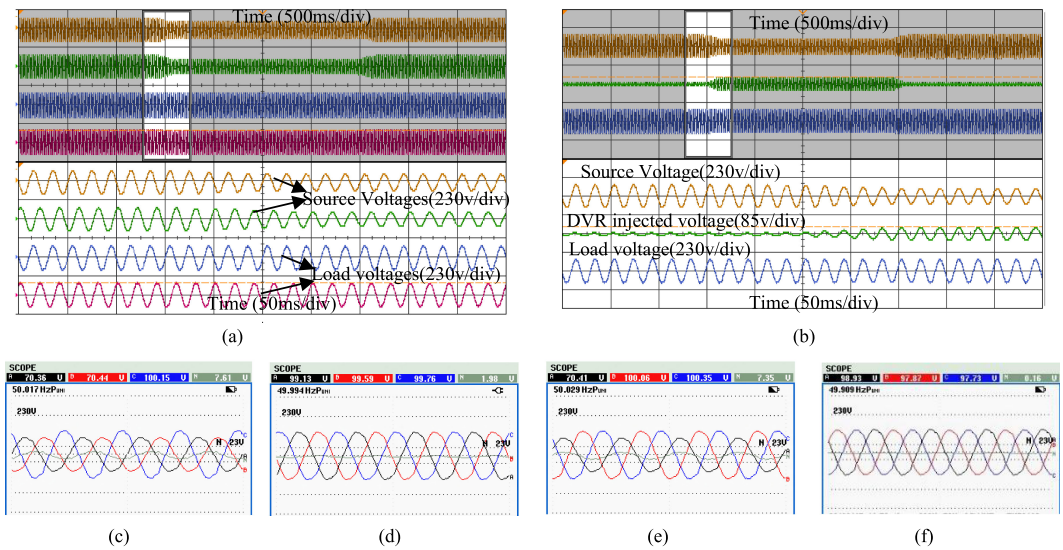

Fig. 8. Experimental results. (a) and (b) Dynamic response of DVR under two-phase and single-phase sag (192 v/div). (c) and (d) Steady-state voltage waveform of source and load under two-phase sag. (e) and (f) Steady-state voltage waveform of source and load under single-phase sag.

D. Single-Phase Sag

The dynamic response of a DVR for a 30% dip in phase-a is portrayed in Fig. 8(b). The supply voltage drops to 70 V in phase-a as shown in Fig. 8(e). The control algorithm responds immediately after the detection of sag and injects voltage as shown in Fig. 8(b) and (f) to keep the load voltage unchanged.

E. Asymmetric Harmonics

To evaluate the performance of DVR with harmonics in voltage source, a nonlinear load of diode rectifier type is connected in parallel feeder line as shown in Fig. 1. The steady-state grid voltage is distorted by harmonics due to the addition of nonlinear loads and is shown in Fig. 9(a) and (c). Along with odd harmonics, a balanced voltage dip of 30% is also generated to test the performance of control algorithm. In this case, the CDSC prefilter and controller (PSC and NSC) tracks the fundamental component of reference voltages and the modified CDSC extractor extracts the respective harmonics present in the load voltage and generates a nonfundamental component which is added in 180° phase opposition with the fundamental component. It can be seen from Fig. 9(a) that the zoomed part of the rectangular portion clearly shows the load voltage is maintained constant during sag and also harmonics are mitigated. The reduction in

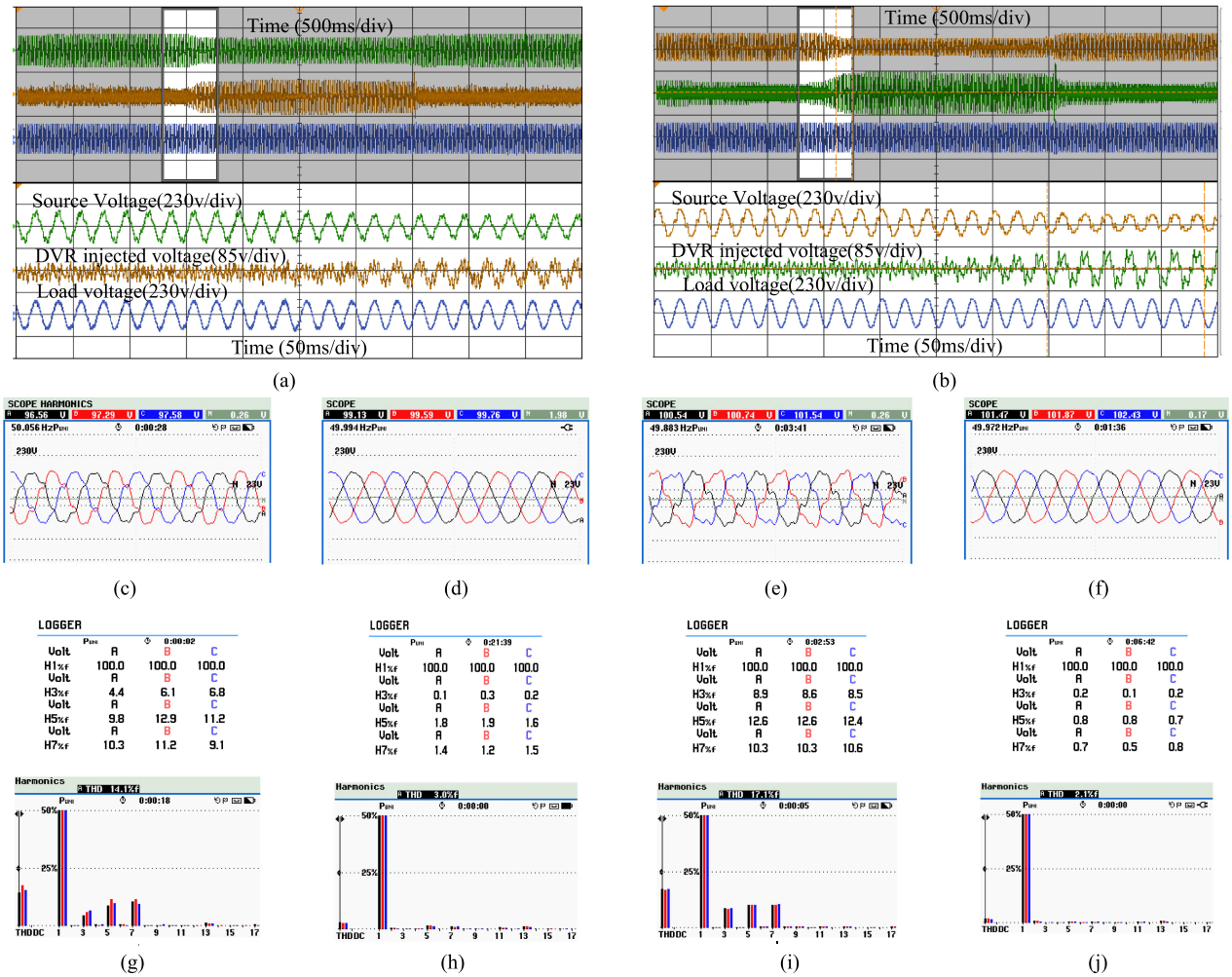

Fig. 9. Experimental results. (a) and (b) Dynamic response of DVR under balanced sag with asymmetric and symmetric harmonics (192 v/div). (c)–(f) Steady-state voltage waveform of source and load under asymmetric and symmetric harmonics. (g) and (h) Harmonic spectrum of source and load voltages during asymmetric harmonics. (i) and (j) Harmonic spectrum of source and load voltages during symmetric harmonics.

THD is reflected from Fig. 9(g) and (h), where THD of source voltage is 14.1% and respective load voltage is 3.0%.

F. Symmetric Harmonics

In this case, the performance of dual role CDSC-based DVC is tested by connecting unbalanced nonlinear loads at the PCC to generate odd symmetric harmonics. The harmonic contents introduce a THD of 17.1% in grid voltage as shown in Fig. 9(i) along with a balanced voltage dip of 30% which can be observed from Fig. 9(b). CDSC prefilter extracts the ISC accurately even under symmetric harmonics. DVC algorithm compensates for the voltage sag and restores fundamental of load voltage to the nominal value as shown in Fig. 9(b) and (f). The THD of the total voltage is reduced to 2.1% which is evident from Fig. 9(j).

VI. Conclusion

This paper presented the flexible control strategy for the effective control of DVR. It is based on the CDSC operator which plays a dual role as a prefilter and as an extractor. Therefore, the main contribution of this paper was the development of dual role CDSC-based DVC algorithm for compensating voltage sags and simultaneously mitigating the harmonics from load voltage. First, the ISC of the grid voltages were obtained using a CDSC prefilter, which is customized to filter out symmetric and asymmetric voltage harmonics. Then, the CDSC-based DVC algorithm with positive and negative sequence controllers was implemented in the *dq* frame to track the DVR reference voltages. Furthermore, the load voltage THD was reduced to 3.0% (from 14.1%) in asymmetric harmonic case and to 2.1% (from 17.1%) in symmetric harmonics case by adding an extractor based on the modified CDSC strategy to the control algorithm which is designed to extract the dominant lower order harmonics from the load voltage. In summary, based on the simulation studies and experimental results, the proposed algorithm operates effectively even when the grid voltage is distorted with variations such as balanced, unbalanced sags, and during the presence of asymmetric and symmetric voltage harmonics.

APPENDIX

TABLE I
EXPERIMENTAL SETUP—SYSTEM PARAMETERS

Device	Description	Value
Source	AC voltage (phase voltage rms)	100 V
	Frequency	50 Hz
Load (Star)	Resistance	0-400 Ω ,5A
Inverter	Switching frequency	5 kHz
	DC link Voltage	200 V
Filter	Capacitance	70 μF
Injection Transformer	Inductance, Turns ratio	720 μH, 1:1
	Primary and secondary voltage	230 V

TABLE II
SIMULATION STUDIES—SYSTEM PARAMETERS

Device	Description	Value
Supply	AC voltage (LL rms)	10 KV
	Frequency	50 Hz
	Supply impedance (Z_s)	2.6 Ω, 0.006048 mH
Load (Delta)		45KW/6670Ω
Inverter	Switching frequency	5 KHz
	DC link Voltage	600V
Filter	Inductance (L_f)	260 μH
	Capacitance (C_f)	120 μF
Injection Transformer (per phase)	Rated Power (S_{tra})	67 KVA
	Primary Voltage (V_1) (LL)	2900V
	Secondary voltage(V_2)	290V

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